LATTICE SEMICONDUCTOR

THE LOW POWER LEADER

Exhibit 99.1
Forward Looking Statements
We may make projections or other forward-looking statements regarding future events during our presentation today. We caution you that such statements are predictions based on information that is currently available and that actual results may differ materially. We refer you to the documents that the company has filed with the SEC, including our 10-K, 10-Qs and 8-Ks. These documents identify important risk factors that could cause actual results to differ materially from those contained in our projections or forward-looking statements.

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Solid Progress Over the Past Year

FOCUSED STRATEGY
100% Focus on FPGA

RE-ENERGIZED TEAM
New Leadership Team; Revitalized Culture

SOLUTION INNOVATION
Application Focused Innovation

PROFIT EXPANSION
2x Growth in Profit
5x Growth in Cash Flow

INCREASED INVESTMENT
Increasing Investment in New Devices and Solutions

STRONGER ROADMAP
Faster Cadence; High Fidelity Execution

Note: Net profit and cash flow expansion based on non-GAAP results from Q1 thru Q3 2019 compared to Q1 thru Q3 2018
New Products Over the Next 12 Months

- **sensAI 2.0**
  - New AI Capabilities
  - **LAUNCH DATE MAY 20, 2019**

- **MachXO3D**
  - Robust Platform Security
  - **LAUNCH DATE MAY 20, 2019**

- **CrossLinkPlus**
  - Enhanced Video Bridging
  - Sampling in H2 2019

- **Next Generation**
  - Next Generation FPGA Platform
  - Sampling early 2020

- **Q3 2019**

- **Today**
Our Mission

The Low Power Programmable Leader
Lattice’s Focus: Low Power, Small Size

**OTHER FPGA COMPANIES**
Focused on Large, High Power Devices for Data Center Compute

~200 W With Heat Sink

**Focused on Low Power, Smaller Form Factors**

~1 W (Small)

~1 mW (Smallest)

Addressing Applications Where Power Efficiency & Small Size are Important
Solving Problems at the Edge

AI Inferencing at the Edge

VIDEO

Embedded Vision

SECURITY

Hardware Platform Security

5G INFRASTRUCTURE

Control & Management

AUTOMATION

Precision Robotic Motor Control

~1 W (Small)

~1 mW (Smallest)
Introducing Our New Low Power FPGA Platform

LATTICE NEXUS
Introducing Our New Low Power FPGA Platform

LATTICE INNOVATION

SOLUTIONS

ARCHITECTURE

Hardened D-PHY
Fast Programmable I/O

Logic Cells
Embedded Memory

DSP Blocks

Ultra Fast Boot

Enhanced PLLs

Hardened PCIe

CIRCUIT

LATTICE NEXUS
Lattice Nexus is Changing the Landscape

**POWER**
- Operating Power Consumption
  - Up to 75% Lower power

**PERFORMANCE**
- Video Connectivity
  - Up to 2x Faster speed

**RELIABILITY**
- Soft Error Rates
  - Up to 100x Lower SER

Note: comparing similar class competitive devices
Bringing Lattice Nexus Across All our Key End Markets

COMMUNICATIONS

- 5G Wireless
- Switches/Routers

COMPUTE

- Servers
- Client

INDUSTRIAL

- Industrial IoT
- Factory Automation

AUTOMOTIVE

- ADAS
- Infotainment

CONSUMER

- Smart Home
- Wearables

$3B Lattice Market Opportunity
LATTICE NEXUS

- Low power leadership
- Edge computing ready
- Robust and reliable
- Smallest form factor
- Faster innovation cadence
Steve Douglass
Corporate Vice President, R&D
Introducing Our New Low Power FPGA Platform

ARCHITECTURE

Logic Cells
Embedded Memory
DSP Blocks
Hardened PHY
Fast Programmable I/O
Ultra-Fast Boot
Enhanced PLLs
Hardened PCIe

SOLUTIONS

LATTICE INNOVATION

CIRCUIT

LATTICE NEXUS
Greatly reduces transistor leakage and susceptibility to soft errors
FDSOI leverages bulk CMOS process and has fewer processing steps
In high volume production today
Circuit Innovation

SOLUTIONS

ARCHITECTURE

CIRCUIT

POWER

Static Power

Half
The Power

RELIABILITY

Soft Error Rate

100x
Lower SER

Bulk
FDSOI

Bulk
FDSOI

Hardened D-PHY
Fast Programmable I/O
Logic Cells
Embedded Memory
DSP Blocks
Enhanced PLLs
Hardened PCIe

Industry Leading SER

Ultra Fast Boot

Circuit Innovation
Circuit Innovation

PROGRAMMABLE BODY BIAS

Allows customers to optimize for both:

- **HIGHER PERFORMANCE**
- **LOWER POWER**

**ARCHITECTURE**

- Hardened D-PHY
- Fast Programmable I/O
- Industry-Leading SER
- Enhanced PLLs
- Hardened PCIe
- Logic Cells
- Embedded Memory
- DSP Blocks
- Ultra Fast Boot
- Hardened PCIe

**CIRCUIT**

- Logic Cells
- Embedded Memory
- DSP Blocks
- Hardened PCIe
- Ultra Fast Boot
- Enhanced PLLs
- Hardened D-PHY

**SOLUTIONS**

- Logic Cells
- Embedded Memory
- DSP Blocks
- Hardened PCIe
- Ultra Fast Boot
- Enhanced PLLs
- Hardened D-PHY
Architecture Innovation

OPTIMIZED FOR POWER EFFICIENT COMPUTING

ARCHITECTURE

- Hardened D-PHY
- Fast Programmable I/O
- Logic Cells
- Embedded Memory
- DSP Blocks
- Enhanced PLLs
- Hardened PCIe

CIRCUIT

- Hardened D-PHY
- Fast Programmable I/O
- Logic Cells
- Embedded Memory
- DSP Blocks
- Enhanced PLLs
- Hardened PCIe

SOLUTIONS

- Logic Cells
- Embedded Memory
- DSP Blocks
- Hardened D-PHY
- Fast Programmable I/O
- Enhanced PLLs
- Hardened PCIe
Architecture Innovation

OPTIMIZED FOR POWER EFFICIENT COMPUTING

2x Faster Performance
Half The Power

Note: Performance and power relative to Lattice prior generation devices
What You Are Seeing
Human presence detection with bounding box around upper body implemented with our first Lattice Nexus based device.

Why It Matters
Human presence detection is a common AI use case in many Edge applications including security cameras, client compute, factory automation, and automotive.
Solutions Innovation

ARCHITECTURE

- Hardened D-PHY
- Fast Programmable I/O
- Enhanced PLLs
- Hardened PCIe
- Logic Cells
- Embedded Memory
- DSP Blocks
- Ultra Fast Boot

CIRCUIT

- Industry Leading SER
- Enhanced PLLs
- Hardened PCIe
- CIRCUIT

APPLICATION FOCUSED SOLUTIONS

EMBEDDED VISION

- SENSOR BRIDGING
- SENSOR AGGREGATION

- SubLVDS
- D-PHY
- MACHINE VISION PROCESSOR
- IMAGE SENSORS
- D-PHY
- LATTICE

IMAGE PROCESSING

- D-PHY
- LATTICE

LATTICE TECHNOLOGIES

Logic Cells
Embedded Memory
DSP Blocks
Hardened D-PHY
Fast Programmable I/O
Enhanced PLLs
Hardened PCIe
Ultra Fast Boot

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Solutions Innovation

ARCHITECTURE

- Hardened D-PHY
- Fast Programmable I/O
- Industry Leading SER
- Enhanced PLLs
- Hardened PCIe
- Logic Cells
- Embedded Memory
- DSP Blocks
- Ultra Fast Boot

CIRCUIT

APPLICATION FOCUSED SOLUTIONS

EMBEDDED VISION

SENSOR BRIDGING

Sub-LVDS → LATTICE → D-PHY → MACHINE VISION PROCESSOR

SENSOR AGGREGATION

IMAGE SENSORS → D-PHY → LATTICE

IMAGE PROCESSING

D-PHY → LATTICE → D-PHY → MOBILE PROCESSOR
Camera Aggregation Demo

What You Are Seeing
MIPI CSI-2 data streams from 4 cameras are aggregated into a single data stream, bridged to parallel data and displayed in a single HDMI output.

Why It Matters
Number of sensors are increasing, and the application processors have limited MIPI inputs.

Number of screen sizes and resolutions are increasing.

Need solution that can aggregate data streams for multiple image sensors in applications such as ADAS, drones, AR/VR, robots etc.

KEY APPLICATIONS
AR / VR  Drones  ADAS  Robotics

OVERVIEW
Introducing Our New Low Power FPGA Platform
Introducing Lattice CrossLink-NX
Introducing Lattice CrossLink-NX

- Hardened MIPI D-PHY
- Fast Programmable I/O
- Programmable Logic
- Embedded Memory
- DSP Blocks
- Industry Leading SER
- Enhanced PLLs
- Ultra Fast Boot
- Hardened PCIe
A Closer Look at CrossLink-NX

**Programmable Logic Core**
- Low power mode
- High performance mode
- High embedded memory count
- Optimized DSP blocks

**Fast Programmable I/O**
- Up to 12 MIPI D-PHY interfaces @ 1.5 Gbps
- LVDS, subLVDS, SGMII
- DDR3 @ 1066 Mbps
- Up to 192 total I/O

**Dedicated Interfaces**
- 8 D-PHY lanes @ 2.5 Gbps
- One lane PCIe @ 5 Gbps

**Instant-On**
- 3 ms I/O configuration
- 14 ms device configuration

**Enhanced for Customer Needs: Power Efficiency, Performance, Reliability**
Esam Elashmawi
Chief Marketing & Strategy Officer
Customer Engagement

LOW POWER

PERFORMANCE

HIGH RELIABILITY
Solving the Power Challenge

**POWER IS KEY TO SOLVE**

**PORTABLE & AUTONOMOUS CHALLENGES**

**SYSTEM & OPERATING COSTS**

**LOWEST POWER FPGA …**

Up to **75%** lower power compared to competition

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Operating Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Xilinx</td>
<td>High</td>
</tr>
<tr>
<td>Spartan 7</td>
<td>Medium</td>
</tr>
<tr>
<td>Intel</td>
<td>Low</td>
</tr>
<tr>
<td>Cyclone 10</td>
<td>Very Low</td>
</tr>
<tr>
<td>Lattice</td>
<td>Lowest</td>
</tr>
<tr>
<td>CrossLink-NX</td>
<td>Lowest</td>
</tr>
</tbody>
</table>

Note: comparing similar class competitive devices

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CrossLink-NX Low Power Demo

OVERVIEW

What You Are Seeing
Power consumption for Lattice CrossLink-NX-40 running a typical design compared with Xilinx Spartan 7 (XC7S50) and Intel Cyclone 10LP (10CL025).

Why It Matters
- Simplifies thermal management
- Improves operating costs
- Extends battery life

KEY APPLICATIONS
- Industrial
- Robots
- Drones
- Medical
- Factory Automation
- Servers
- 5G
Solving the Performance Challenge

LOW POWER

PERFORMANCE

HIGH RELIABILITY

PERFORMANCE IS KEY TO SOLVE

USER EXPERIENCE

PERFORMANCE FOR AI

ENHANCED PERFORMANCE FEATURES

Fastest display connection

Optimized for power efficient computing

Note: comparing similar class competitive devices
sensAI Application Example: Retail Security Camera

### ALWAYS-ON HUMAN COUNTING

![Image of a security camera monitoring people]

**Lattice CrossLink-NX**

- **SRAM** (weights / activations)
- **Sensor Interface**
- **Neural Network Accelerators**

Data → Sensors → MCU

Results → Sensors 

**PERFORMANCE**

- 10x FASTER
- 1 fps
- 10 fps

**POWER**

- 600 mW
- 3x LOWER
- 200 mW

**CrossLink- NX-40K**

- SensAI Application Example: Retail Security Camera

- CrossLink- NX
- 40K
- 10 fps
- 100 mW
- 200 mW
- 3x LOWER
PERFORMANCE IS KEY TO SOLVE

INCREASED DEMAND FOR INSTANT-ON APPLICATIONS

UP TO 50X FASTER

I/O wake up time

- Intel Cyclone 10LP
- Xilinx Spartan 7
- Lattice CrossLink-NX

Note: comparing similar class competitive devices
**CrossLink-NX Instant-on Demo**

**OVERVIEW**

**What You Are Seeing**
Time for device to self configure I/O to a user defined state for Lattice CrossLink-NX-40 compared with Xilinx Spartan 7 (XCS7-50) and Intel Cyclone 10LP (10LP025).

**Why It Matters**
“Instant-on” I/O configuration is important for applications such as LED drivers, motor control and board housekeeping.

Reduces complexity, cost, and power dissipation of customer systems.

**KEY APPLICATIONS**

- **Motor Control**
- **Human Machine Interfaces**
- **ADAS**

Note: based on competition’s evaluation boards running at similar frequencies
Solving the Reliability Challenge

RELIABILITY IS KEY TO SOLVE

CRITICAL SAFETY & RUGGEDIZED

SYSTEM UP TIME

MOST RELIABLE FPGA FOR RUGGEDIZED APPS

Temperature Ranges

-40°C  125°C

Soft Error Rates (FIT)

Xilinx*
Spartan 7

Lattice
CrossLink-NX

Up to 100x Lower SER

FIT (Failure In Time) (1B device hours)
* Based on Xilinx published data

Suitable for:
OUTDOOR | AUTOMOTIVE | INDUSTRIAL | AVIONICS
Small Size Matters

CrossLink-NX
LIFCL-40-7MG121C

Logic Cells
40K

Xilinx Spartan 7
XC7S50-1GCSGA324C

15 mm
19 mm

Intel Cyclone 10LP
10CL040YU484C6

50K
40K
Engaged with > 65 customers

Early Access Program with 30+ customers

Solutions available today
Jim Anderson
President, Chief Executive Officer
The Lowest Power FPGA Platform

ARCHITECTURE
- Logic Cells
- Embedded Memory
- DSP Blocks
- Hardened PHY
- Fast Programmable I/O
- Ultra Fast Boot
- Industry Leading SER
- Enhanced PLLs
- Hardened PCIe

CIRCUIT

SOLUTIONS

LOW POWER

PERFORMANCE

HIGH RELIABILITY

LATTICE NEXUS

Product 2
Product 3
Product N

CrossLink-NX
Faster Cadence of New Devices and Solutions

- **H1 2019**
  - Lattice sensAI 2.0

- **H2 2019**
  - Lattice Radiant 2.0

- **H1 2020**
  - Embedded Vision Stack

- **H2 2020**
  - Security Stack

**Devices**

- MachXO3D
- CrossLinkPlus
- CrossLink-NX
- Nexus Product #2
- Nexus Product #3
DEMO SIGNAGE
Human Presence Detection & Counting

**OVERVIEW**

**What You Are Seeing**
Human presence detection and counting with bounding box around upper body implemented with Lattice CrossLink-NX

**Why It Matters**
Human presence detection is a common AI use case in many Edge applications including security cameras, client compute, factory automation, and automotive.

**The Lattice Advantage**
Lattice CrossLink-NX supports detection at 2x frame rate and 0.5x the power of prior generation

Lattice CrossLink-NX supports detection at 10x higher frame rate and 0.3x power compared to MCUs

Integrated D-PHY to reduce power and BOM cost

FPGA flexibility for additional pre/post processing compared to fixed function ASICs

**KEY APPLICATIONS**

- **Security cameras**
- **Client compute**
- **Smart doorbells**
- **Smart appliances**
Camera Aggregation

**OVERVIEW**

**What You Are Seeing**
4 cameras, each providing a separate MIPI CSI-2 data stream aggregated into a single data stream, bridged to parallel data and displayed in a single HDMI output.

**Why It Matters**
Application processors with limited MIPI D-PHY inputs cannot interface to multiple image sensors in applications such as ADAS, drones, AR/VR, robots etc.

**The Lattice Advantage**
- Only FPGA with up to 8 hard D-PHY lanes @ 2.5 Gbps
- Scalable to support up to 14 MIPI D-PHY interfaces
- Low power consumption ~300 mW
- Up to 40K LUTs for customization and additional image processing

**KEY APPLICATIONS**
- AR / VR
- Drones
- ADAS
- Robotics
CrossLink-NX Delivering Up to 75% Lower Power

**OPERATING POWER (mW) @ 2 MHz and 200 MHz**

<table>
<thead>
<tr>
<th>Device</th>
<th>Power Consumption (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CrossLink-NX LIFCL-40</td>
<td>100</td>
</tr>
<tr>
<td>Spartan 7 XC7S50</td>
<td>200</td>
</tr>
<tr>
<td>Cyclone 10 LP 10CL025</td>
<td>300</td>
</tr>
</tbody>
</table>

**What You Are Seeing**

Power consumption for Lattice CrossLink-NX-40 running a typical design compared with Xilinx Spartan 7 (XC7S50) and Intel Cyclone 10LP (10CL025) running at a variety of frequencies.

**Why It Matters**

Low power consumption simplifies thermal management, improves operating costs and where applicable extends battery life.

**The Lattice Advantage**

Up to 75% lower power than Xilinx Spartan 7 and Intel Cyclone 10LP.

- Programmable back bias for per device performance / static power optimization.
- 28 nm FD-SOI technology provides best in class dynamic power.
- HP and LP user modes.

**KEY APPLICATIONS**

- Industrial Robots
- Drones
- Medical
- Factory Automation
- Servers
- 5G
CrossLink-NX Enabling Up to 50x Faster I/O Wake Up Time

What You Are Seeing
The I/O self configuration time of the Lattice CrossLink-NX-40 running on the Lattice development board compared with Xilinx Spartan 7 (XCS7-50) and Intel Cyclone 10LP (10LP025) configured for the fastest possible configuration times on their associated development boards.

Why It Matters
“Instant-on” I/O configuration is important for applications such as LED drivers, motor control and board housekeeping.

Reduces complexity, cost, and power dissipation of customer systems

The Lattice Advantage
Smart monitor of SPI configuration memory avoids delay timers

150 MHz Quad SPI configuration interface for high speed configuration data transfer

Early I/O configuration ensures outputs stable as soon as possible