Lattice Announces ispLEVER 7.2 Service Pack 1 FPGA Design Tool Suite

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Tool Suite Includes Support for the New LatticeECP3 FPGA Family

HILLSBORO, OR - FEBRUARY 23, 2009 - Lattice Semiconductor Corporation (NASDAQ: LSCC) today announced the immediate availability of Service Pack 1 for Version 7.2 of its ispLEVER® FPGA design tool suite. The release adds support for the new LatticeECP3™ FPGA family, also announced today, and the latest release of Synopsys' Synplify Pro® advanced FPGA synthesis for all operating systems supported and Aldec's Active-HDL™ Lattice Edition simulator for Windows.

"This release extends the benefits of the ispLEVER 7.2 design tool suite to the new LatticeECP3 FPGA family, including advanced place and route algorithms to reduce runtime on large designs and a clock boosting flow to increase performance," said Mike Kendrick, Lattice's Manager of Software Product Planning. "Additional support for the LatticeECP3 family also is provided by the many other industry leading features of the ispLEVER tool, such as the fast and accurate Power Calculator, bank and pin based Simultaneous Switching Output (SSO) Analyzer, and LatticeMico32™ System design tools for the open source LatticeMico32 soft microprocessor."

LatticeECP3 FPGA Family Support in ispLEVER 7.2 Service Pack 1

The ispLEVER 7.2 Service Pack 1 release includes complete implementation and verification support for the LatticeECP3 FPGA family. Designers with applications targeting the LatticeECP3 family for its low power consumption can plan with confidence using Power Calculator, the FPGA industry's leading tool for power estimation and calculation. Power Calculator measures not only typical power consumption but also worst case power consumption based on actual silicon measurements. "What-if" analysis is virtually effortless as Power Calculator quickly recalculates power consumption under different environmental conditions such as temperature, voltage and activity factors. The SSO Analyzer enables users to see whether their planned pin layout has enough noise margin to operate reliably. Using the SSO Analyzer, "what-if" analysis of different environmental conditions, such as the noise added by the board layout, can estimate results without first building the board, avoiding costly re-spins. In addition, ispLEVER tools such as the Lattice Reveal™ RTL-based hardware debugger and the LatticeMico32 System used to implement the open source LatticeMico32 soft microprocessor now also support the LatticeECP3 family. For more comprehensive information regarding the new and expanded features found in ispLEVER 7.2 Service Pack 1, please visit http://www.latticesemi.com/products/designsoftware/isplever/isplever/whatsnewinisplever.cfm

About the ispLEVER Design Tool Suite

The ispLEVER design tool suite is the flagship design environment for the latest Lattice FPGA products. It provides a complete set of powerful tools for all design tasks, including project management, IP integration, design planning, place and route, in-system logic analysis and more. The ispLEVER tool suite is provided on CD-ROM and DVD for Windows, UNIX or Linux platforms. Synopsys' Synplify Pro advanced FPGA synthesis is included for all operating systems supported, and Aldec's Active-HDL Lattice Edition simulator is included for Windows.

Pricing and Availability

The ispLEVER 7.2 Service Pack 1 tool suite for Windows, LINUX and UNIX users is available immediately without charge for customers with active design tool maintenance. The full ispLEVER design tool suite starts at $1,295 for the Windows version.

About Lattice Semiconductor

Lattice is the source for innovative FPGA, PLD and Mixed Signal programmable logic solutions. For more information, visit www.latticesemi.com

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For more information contact:
Brian Kiernan, Corporate Communications Manager
Lattice Semiconductor Corporation
brian.kiernan@latticesemi.com
voice: (503) 268-8739
fax: (503) 268-8193