Lattice Launches Industry's Lowest Power, Highest value FPGA Devices

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SERDES-Capable LatticeECP3 Family Consumes Half the Power and is Half the Price of Competitive Devices

HILLSBORO, OR - FEBRUARY 23, 2009 - Lattice Semiconductor Corporation (NASDAQ: LSCC) today announced its third generation high value FPGAs, the mid-range 65nm LatticeECP3™ family, which offers the industry's lowest power consumption and price of any SERDES-capable FPGA device. The LatticeECP3 FPGA family offers multi-protocol 3.2G SERDES with XAUI jitter compliance, DDR3 memory interfaces, powerful DSP capabilities, high density on-chip memory and up to 149K LUTS, all with half the power consumption and half the price of competitive SERDES-capable FPGAs. The entire LatticeECP3 family is manufactured using Fujitsu's advanced low power process technology, and is the only 65nm mid-range, high value FPGA family in the industry.

"Like our award winning LatticeECP2M™ devices before it, our LatticeECP3 family once again redefines mid-range, value-based FPGAs, not only by further reducing costs, but also by reducing static power consumption by 80% and total power consumption by over 50% for typical designs, compared to competitive SERDES-capable FPGAs. By making careful design choices and minimizing die size, we are able to offer designers the benefits of high speed serial I/O and processing capabilities, without the power and cost premiums typically associated with these types of devices," said Sean Riley, Corporate Vice President and General Manager of High Density Solutions.

"Early Access" LatticeECP3 Customers React Enthusiastically

"…unprecedented power and performance results."

"...the only FPGA that was able to meet our technical requirements…."

While the LatticeECP3 family is being formally announced today, for several months many Early Access Lattice customers have been experiencing first hand the low power and high value benefits that are the hallmarks of these new FPGA devices.

Shane Flint, Managing Director of Affarii, a provider of wireless transmitter and linearization solutions, said, "Implementation of our 4G transceiver design with Crest Factor Reduction and Predistortion functions in the LatticeECP3 FPGA has yielded unprecedented power and performance results. With sample rates up to 180Msps, LatticeECP3 performance exceeds that of commercially available ASSP offerings, and power consumption is 50% lower than previous Remote Radio Head designs using high-end FPGAs. Add to this the integrated SERDES supporting CPRI, OBSAI and Gigabit Ethernet, and we can offer a single chip processing solution that greatly reduces real estate, power consumption and implementation cost for wireless basestation vendors."

Philippe Wetzel, CEO of Vitec Multimedia, a pioneer and worldwide leader in the digital video domain, said, "Vitec selected the LatticeECP3 in the summer of 2008 to support a technically demanding new product design. It was the only FPGA that was able to meet our technical requirements for 3G-SDI broadcast video, PCIe x4 and DDR3 at 800MHz, all on a low cost FPGA platform."

Five LatticeECP3 Family Members

The five devices that comprise the low power LatticeECP3 FPGA family all offer standards-compliant multi-protocol 3G SERDES, the industry's only DDR3 memory interface for low cost FPGAs and high performance, cascadable DSP slices that are ideal for high performance RF, baseband and image signal processing. Toggling at 1Gbps, the LatticeECP3 FPGAs also feature the fastest LVDS I/O available in a mid-range FPGA family, as well as embedded memory of up to 6.8 Mbits. Logic density varies from 17K LUTs to 149K LUTs with up to 586 user I/O. The LatticeECP3 FPGA family's high performance features include:

- 3.2Gbps SERDES with 10GbE XAUI jitter compliance and the ability to mix and match multiple protocols on each SERDES quad. This includes PCI Express, CPRI, OBSAI, XAUI, Serial RapidIO and Gigabit Ethernet.
- The SERDES/PCS blocks have been designed specifically to enable the design of the low latency variation CPRI links that are found in wireless basestations with Remote Radio Head connectivity.
- Compliance to the SMPTE Serial Digital Interface standard, with the unprecedented ability to support 3G, HD and SD video broadcast signals independently on each SERDES channel. The triple rate support is performed without any oversampling technique, consuming the least possible amount of power.
- DSP blocks allowing up to 36x36 Multiply and Accumulate functions running at 500MHz. The DSP slices also feature innovative cascadability for implementing wide ALU and adder tree functions without the performance bottlenecks of FPGA logic.
- 800Mbps DDR3 memory interfaces, with built-in read and write leveling.
- 1Gbps LVDS I/O, with Input Delay blocks, allows interfacing to high performance ADC and DACs.

With these features, the LatticeECP3 FPGA family is ideally suited for deployment in high volume cost- and power-sensitive wireless infrastructure and wireline access equipment, as well as video and imaging, applications.

Design Tool Support

The LatticeECP3 FPGA family is supported by the ispLEVER® design tool suite, version 7.2 Service Pack 1, which also has been announced today. The ispLEVER design tool suite is the flagship design environment for the latest Lattice FPGA products. It provides a complete set of powerful tools for all design tasks, including project management, IP integration, design planning, place and route, in-system logic analysis and more. The ispLEVER software is provided on CD-ROM and DVD for Windows, UNIX or Linux platforms. The ispLEVER design tool suite includes Synopsys' Synplify Pro® synthesis for all operating systems supported and Aldec's Active-HDL™ Lattice Edition simulator for Windows.

Pricing and Availability

Production devices are available now. In 25K unit volume and the FN484 wirebond package, the LatticeECP3-70 is priced as low as $35 and the LatticeECP3-95 is priced as low as $50.

For more information about the new LatticeECP3 FPGA family, please visit http://www.latticesemi.com/products/fpga/ecp3

About Lattice Semiconductor

Lattice is the source for innovative FPGA, PLD and Mixed Signal programmable logic solutions. For more information, visit www.latticesemi.com

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