SPI4.2 MACO Cores for LatticeSCM FPGAs Win Coveted Product of the Year Award

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EN-Genius Network Also Recognizes LatticeECP2M Development Kit

HILLSBORO, OR - JANUARY 19, 2009 - Lattice Semiconductor (NASDAQ: LSCC) today announced that its LatticeSCM™ FPGA SPI4.2 MACO™ Cores with Enhanced Buffer Management have been recognized as "Product of the Year, Best System Interconnect Element" by the EN-Genius Network. In addition, the LatticeECP2M™ FPGA Development Kit for PCI Express captured an "Honorable Mention" award.

"We started this process nearly a decade ago, and it is very undemocratic," said Editor-in-Chief Paul McGoldrick. "We never involve the vendors or allow (or demand, as other publications do) some kind of essay with the technical and business information as to why their products should win. At EN-Genius we always call the winners (and the occasional losers) as we see them, as we do with every review we write." McGoldrick went on to note that he and editorial colleagues Lee Goldberg and Alex Mendelsohn believe the products selected "will make significant bottom line numbers for the companies involved" because of their strong technical merit, design innovation and marketability.

Regarding the LatticeSCM FPGA SPI4.2 MACO Cores, EN-Genius observed, "The enhanced queuing and scheduling capabilities offered by the LatticeSCM family's SPI 4.2 logic could go a long way to offloading a network processor from some lower-level traffic management tasks or providing some very intelligent buffering between system elements."

"We continue to enhance our SPI4.2 solution portfolio by integrating sophisticated system-level features, while maintaining the low cost and power targets that have made Lattice a leading SPI4.2 programmable gasket solution provider," said Shakeel Peera, Lattice Director of Strategic Marketing for SRAM FPGAs. "Designers working on 10G Carrier Ethernet and Packet over SONET platforms will find these features useful as they architect systems designed around determinism and Service Level Agreement (SLA) guarantees."

Also recognizing the LatticeECP2M FPGA Development Kit for PCI Express, the editors noted that, "Honorable Mentions go to products that very nearly made it to a full Award category, but did not fit into our Award general criteria." Editor Lee Goldberg said, "This well-provisioned kit provides a quick, easy way for designers to get comfortable with using their SERDES-equipped LatticeECP2M family in many of the high volume PCI Express applications where these devices' low cost makes them extremely attractive. A couple of years ago Lattice shook up the FPGA world with the introduction of its SERDES-equipped LatticeECPM2 product line that put PCI Express capabilities on a $23 device. The LatticeECP2M series delivers the basic functionality to nicely satisfy the requirements of many PCIe applications."

About LatticeECP2M and LatticeSC/M FPGAs

LatticeECP2M FPGAs are an innovative response to the broad range of customers who have been clamoring for low-cost SERDES capability for chip-to-chip and small form-factor backplane applications. The LatticeECP2M family maintains all of the compelling features of the 90nm LatticeECP2™ family that are required for high-volume, cost-sensitive applications, while dramatically increasing memory capacity (ranging from 1.2 Mbits to 5.3 Mbits) and DSP resources (ranging from 24 to 168 multipliers). The SERDES integrated into the LatticeECP2M devices has been engineered as a quad-based architecture with 1 to 4 quads, depending on the size of the device. Each quad features four SERDES channels (four complete TX and RX channels), with each channel featuring power consumption as low as 100mW and supporting data rates from 270 Mbps to 3.125 Gbps. A flexible PCS layer that includes 8b/10b encoding, an Ethernet link state machine and rate matching circuitry also are built onto the chip. The SERDES/PCS combination is designed to support today's most common packet-based protocols, including PCI Express, Gigabit Ethernet, Serial RapidIO and wireless interface standards (OBSAI and CPRI).

The LatticeSC/M Extreme Performance™ FPGAs deliver the industry's most extensive portfolio of high performance IP. LatticeSC devices combine up to 32 3.8 Gbps SERDES channels with an innovative Physical Coding Sublayer (PCS) to provide a breadth of support for interface protocols including PCI Express, Serial RapidIO, Ethernet, Fiber Channel, XAUI and SONET/SDH. Source synchronous I/O standards such as RapidIO, HyperTransport, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX and memory standards such as SDR, DDR1, DDR2, QDR2 and RLDRAM are implemented with dedicated PURESPEED I/O logic, which delivers up to 2 Gbps parallel I/O performance. LatticeSCM devices also include exclusive MACO (Masked Array for Cost Optimization) pre-engineered IP in structured ASIC blocks for low-cost and low-power system-level integration.

About Lattice Semiconductor

Lattice is the source for innovative FPGA, PLD and Mixed Signal programmable logic solutions. For more information, visit www.latticesemi.com.

Statements in this news release looking forward in time are made pursuant to the safe harbor provisions of the Private Securities Litigation Reform Act of 1995. Investors are cautioned that forward-looking statements involve risks and uncertainties including market acceptance and demand for our new products, our dependencies on our third party software suppliers, the impact of competitive products and pricing, technological and product development risks and other risk factors detailed in the Company's Securities and Exchange Commission filings. Actual results may differ materially from forward-looking statements.

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