



## Lattice Announces PCI Express Solutions for LatticeECP2M and LatticeSCM FPGAs

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### -- Successfully Tested Against PCI Express Version 1.0a Specifications, Solutions Enable Single-Chip, Programmable PCI Express Endpoints --

**HILLSBORO, OR - October 30, 2006** -Lattice Semiconductor (NASDAQ: LSCC) today announced the availability of new PCI Express Intellectual Property (IP) cores in its ispLeverCORE™ portfolio. A new PCI Express core optimized for the newly announced LatticeECP2M™ low-cost FPGA family implements a single-chip PCI Express x1 endpoint solution with integrated SERDES that is ideal for high-volume, low-cost and limited form-factor applications. New PCI Express x1 and x4 cores also are available for the LatticeSCM™ FPGA family, which are suitable for system applications requiring the highest integration and performance. The IP cores are available within the IPexpress™ flow supported by Lattice's ispLEVER® 6.0 Service Pack 1, or later, design tool suite.

Lattice's PCI Express solutions include not only new IP cores but new evaluation boards, demo software and drivers as well. LatticeECP2M and LatticeSCM evaluation boards are both available in the PCI Express mechanical form-factor compatible with standard motherboards. The demo software utilizes the evaluation boards to demonstrate PCI express endpoint operation, including configuration, memory/register access and simple tests. Demo drivers and API also are available for users who wish to extend the demo capabilities. The Lattice PCI Express IP cores and evaluation boards have successfully passed testing against PCI Express version 1.0a specifications at the recent October 2006 PCI-SIG workshop, ensuring that Lattice's solutions are interoperable with existing PCI Express-supported systems.

"With this announcement, Lattice is the only FPGA vendor to offer single-chip PCI Express solutions with on-board SERDES in both low-cost (LatticeECP2M) and high-end (LatticeSCM) FPGAs, further illustrating our Lattice 'More of the Best' philosophy," said Stan Kopec, corporate vice president of marketing. "By providing an expanded range of solutions with 2.5 Gbps SERDES channels and embedded PHYs, Lattice is uniquely positioned to enable its customers to better optimize the price and performance of their PCI Express-based products. These devices, along with our new PCI Express IP cores, evaluation boards, demos and easy-to-use ispLEVER design flow, combine to deliver complete solutions that support rapid prototyping of single-chip PCI Express designs."

As the successor to the pervasive PCI standard, PCI Express inherits a rich legacy of installed software and applications. PCI Express continues to gain momentum and is poised for widespread deployment across a wide range of applications, including PCs, servers, routers, switches, industrial automation, robotics, medical, graphics/image processing and video capture. With this announcement, Lattice is poised to capitalize on the rapid expansion of the PCI Express market with SERDES-based solutions that address a range of system cost needs.

As the centerpieces of Lattice's PCI Express solutions, the LatticeECP2M and LatticeSCM IP cores offer different approaches to implementing the PCI Express protocol. The LatticeECP2M core implements the transaction, data link and most of the physical layer in soft IP. The remainder of the physical layer – including clock tolerance compensation, 8b/10b encoding and link synchronization – is completely embedded in the new low-cost LatticeECP2M Physical Coding Sublayer (PCS), which fully supports 2.5 Gbps operation. As a result, with the LatticeECP2M core, customers benefit from high-performance and a fully integrated PCI Express solution combined with low-cost PCS/SERDES: a compelling value for high-volume applications.

On the other hand, the LatticeSCM family offers a high-performance FPGA fabric, feature rich SERDES and PCS, as well as pre-engineered hard IP, or MACO™ (Masked Array for Cost Optimization), blocks implemented in ASIC gates that are ideal for high-throughput systems. For PCI Express, the LatticeSCM device utilizes its unique flexiMAC™ block to implement the PCI Express PHY and data link specifications. A separate MACO block also is dedicated to the complex LTSSM (Link Training and Status State Machine), leaving only the transaction layer implemented in FPGA gates. This pre-engineered solution implemented in ASIC gates minimizes cost and power consumption for customers who want to use a high-performance FPGA for their PCI Express design.

Both the LatticeECP2M and LatticeSCM device families offer additional capabilities that enable single-chip PCI Express solutions. On-board Phase Lock Loops (PLLs) support Spread Spectrum Clocking (SSC) for the system-supplied 100 MHz PCI Express clock and enable direct conversion to the 250 MHz reference clock, while the device remains within the PCI Express version 1.0a jitter specifications. This eliminates the need for any external PHY, clock conversion or attenuation chips, driving system cost lower. The combination of lower system cost and single-chip capabilities makes the LatticeECP2M and LatticeSCM devices attractive alternatives to the difficulties posed by other PCI Express offerings, such as competitive FPGAs that require external chips to implement clocking, or off-the-shelf ASSP chips that offer no programmability.

### Pricing and Availability

The LatticeECP2M and LatticeSCM PCI Express solutions are available immediately. The PCI Express IP cores are supported in Lattice's ispLEVER Design Tool Suite Version 6.0 Service Pack 1 or later. The LatticeECP2M PCI Express core can be downloaded from the Lattice website and is available for a no charge time-limited evaluation within the IPexpress flow of the ispLEVER design tool. The LatticeECP2M device evaluation board is available with a x1 PCI Express connector; for the LatticeSCM device, two evaluation boards are available with x1 and x8 PCI Express connectors,

respectively. Information about the cores, design tools, boards, demos and drivers can be found on the Lattice website at [www.latticesemi.com](http://www.latticesemi.com)

### **About LatticeECP2M FPGAs**

LatticeECP2M FPGAs are an innovative response to the broad range of customers who have been clamoring for low-cost SERDES capability for chip-to-chip and small form-factor backplane applications. The LatticeECP2M family maintains all of the compelling features of the 90nm LatticeECP2™ family that are required for high-volume, cost-sensitive applications, while dramatically increasing memory capacity (ranging from 1.2 Mbits to 5.3 Mbits) and DSP resources (ranging from 24 to 168 multipliers). The SERDES integrated into the LatticeECP2M devices has been engineered as a quad-based architecture with 1 to 4 quads, depending on the size of the device. Each quad features 4 SERDES channels (4 complete TX and RX channels), with each channel featuring power consumption as low as 100mW and supporting data rates from 270 Mbps to 3.125 Gbps. A flexible PCS layer that includes 8b/10b encoding, an Ethernet link state machine and rate matching circuitry also are built onto the chip. The SERDES/PCS combination is designed to support today's most common packet-based protocols, including PCI Express, Gigabit Ethernet, Serial RapidIO and wireless interface standards (OBSAI and CPRI).

The LatticeECP2M family will include five devices ranging in density from 20K to 95K Look-Up Tables (LUTs). Samples of the first member of the LatticeECP2M family, the LatticeECP2M-35, in both 484 and 672 ball fpBGA packages are available now. Lattice plans to bring the remaining members of the LatticeECP2M family to the market during the first half of 2007.

### **About LatticeSC Extreme Performance FPGAs**

LatticeSC™ Extreme Performance™ FPGAs deliver the highest performance and most robust feature set of any programmable logic product in the industry. The LatticeSC FPGA combines up to thirty-two 3.8 Gbps SERDES channels with an innovative Physical Coding Sublayer (PCS) to provide a breadth of support for interface protocols including Serial RapidIO, PCI Express, Ethernet, Fiber Channel, XAUI and SONET/SDH. Source synchronous I/O standards such as RapidIO, HyperTransport, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX, and memory standards including SDR, DDR1, DDR2, QDR2 and RLDRAM are implemented with dedicated PURESPEED™ I/O logic that delivers up to 2 Gbps parallel I/O performance, the fastest in the industry. The LatticeSCM devices also include exclusive MACO (Masked Array for Cost Optimization) pre-engineered IP in structured ASIC blocks for low-cost and low-power system-level integration.

LatticeSC device sizes range from 15,000 to 115,000 LUTs, with up to 7.8 Megabits of block RAM on a single chip. A variety of family members are currently available, including the LatticeSC15, LatticeSC25 and LatticeSC80.

### **About Lattice Semiconductor**

Lattice Semiconductor Corporation provides the industry's broadest range of [Programmable Logic Devices \(PLD\)](#), including [Field Programmable Gate Arrays \(FPGA\)](#), [Complex Programmable Logic Devices \(CPLD\)](#), [Mixed-Signal Power Management](#) and [Clock Generation Devices](#), and industry-leading [SERDES](#) products.

Lattice continues to deliver "More of the Best" to its customers with comprehensive solutions for system design, including an unequalled portfolio of [high performance, non-volatile](#) and [low cost](#) FPGAs.

Lattice products are sold worldwide through an extensive network of independent sales representatives and distributors, primarily to OEM customers in communications, computing, industrial, consumer, automotive, medical and military end markets. For more information, visit <http://www.latticesemi.com>

Statements in this news release looking forward in time are made pursuant to the safe harbor provisions of the Private Securities Litigation Reform Act of 1995. Investors are cautioned that forward-looking statements involve risks and uncertainties including market acceptance and demand for our new products, our dependencies on our third party silicon suppliers, the impact of competitive products and pricing, technological and product development risks and other risk factors detailed in the Company's Securities and Exchange Commission filings. Actual results may differ materially from forward-looking statements.

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