Lattice Expands Market for Low Cost FPGAs with 90nm LatticeECP2 Family

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-- Second Generation EConomy Plus Devices Expand Concept By Reducing Prices 50% and Doubling Available Density --

HILLSBORO, OR - FEBRUARY 8, 2006 - Lattice Semiconductor Corporation (NASDAQ: LSCC) today introduced its second-generation EConomy Plus Field Programmable Gate Array (FPGA) devices, the LatticeECP2™ family. Developed on 90nm Fujitsu CMOS technology utilizing 300mm wafers, this family cuts FPGA prices to under $0.50 per 1,000 Look-up Tables (LUTs) in high volume. Compared to Lattice's first-generation 130nm LatticeECP™ FPGAs, the new family also increases available logic density to 70K LUTs, increases the number of 18x18 multipliers to 88, boosts I/O performance over 50% and enhances configuration capabilities. Capabilities added for the first time to this class of FPGAs include pre-engineered 400Mbps DDR2 memory interface support, configuration bitstream encryption and dual-boot configuration support. Lattice's low cost LatticeECP2 devices are being announced today simultaneously with its high-end LatticeSC™ System Chip FPGAs, fabricated on the same technologyPlease see LatticeSC Family press release also dated today.

"Lattice customers have enthusiastically welcomed the Economy Plus concept that Lattice pioneered with its first-generation LatticeECP family," said Stan Kopec, Lattice corporate vice president of marketing. "The enhancements that LatticeECP2 brings in the areas of logic and memory capacity, I/O performance and configuration flexibility allow this new family to capture many new designs that would otherwise need to be targeted at higher cost, full-featured FPGAs."

Cost Optimized Architecture Provides Rich Feature Set

Throughout their development, the LatticeECP2 devices have been optimized to deliver the features and cost structure required by designers for high-volume applications. Key points include:

Optimized Logic and Routing Fabric: The logic block and routing have been optimized to tailor features such as distributed memory (provided on 12.5% of LUTs) and registers (provided on 75% of LUTs) to the typical application set. The resulting logic fabric allows easy high performance logic implementation.

Pre-engineered 840Mbps Parallel I/O: The rise of DDR memories and other similar standards leaves many designers grappling with the challenge of implementing high performance parallel I/O interfaces within FPGAs. To meet this need designers have historically had to utilize high cost FPGA solutions. The ECP2 devices provide DDR mux/de-mux, precision delay and gearbox logic elements. These can be combined to implement pre-engineered DDR2 (400Mbps) and other source synchronous interfaces operating at up to 840Mbps for applications such as SPI4.2 and ADC/DAC interfaces.

Full Feature sysDSP™ Blocks: To support low cost DSP applications, the ECP2 devices embed sysDSP blocks capable of implementing multiply, accumulate, summation and pipelining functions. The devices can implement DSP functions up to 28,600 Million Multiply Accumulates per second (MMACs) at prices below $.001 per MMAC.

Easy Field Logic Update: In order to accommodate bug fixes, respond to standard changes and support the addition of new features and services, an increasing number of FPGA designs require FPGA logic update in the field. The LatticeECP2 provides dual-boot support and Transparent Field Reconfiguration (TransFR™) I/O to simplify field updates. The devices also support the storage of two or more configurations in industry standard Serial Peripheral Interface (SPI) PROMs. TransFR I/O capability allows designers to precisely control I/O states while a new configuration is loaded into the FPGA, a significant improvement over the more conventional practice of tri-stating I/Os during reconfiguration.

Bitstream Encryption for Enhanced Design Security: To address increasing design piracy concerns, the LatticeECP2 devices have on chip non-volatile key storage and decryption circuitry to allow the decryption of 128-bit AES encrypted bitstreams based on a unique user key. This brings the concept of bitstream encryption to low-cost SRAM FPGA products for the first time, again reducing the need for higher cost FPGAs in many designs.

The LatticeECP2 family will be offered in two versions, the standard LatticeECP2 and a memory enhanced (LatticeECP2M™) version to be announced later in 2006. The LatticeECP2M devices will increase density to 100K LUTS and enhance memory capacity to over 5million bits of RAM. In all, 6 device densities from 6K to 70K LUTs are planned for the LatticeECP2 family plus additional members of the LatticeECP2M family. The LatticeECP2 devices will provide between 55K and 1Mbit of embedded memory through sysMEM™ Embedded Block RAM (EBR), twelve to eighty-eight 18x18 multipliers and 95 to 628 I/O pins. In addition, each device provides two Delay Locked Loops (DLLs) and from 2 to 6 Phase Locked Loops (PLLs) for timing control. The parts will be available in a variety of low-cost TQFP, PQFP and fine pitch BGA (fpBGA) packages and operate from 1.2volt power supplies.

Design Tools and Intellectual Property Support

Design support for the LatticeECP2 devices is provided by the latest version of the ispLEVER tool suite, Version 5.1 using Service Pack 2. These ispLEVER design tools provide designers with access, in one software package, to all Lattice digital devices and include synthesis support from Mentor Graphics and Synplicity.

An extensive range of IP (Intellectual Property) cores, particularly suited for high volume applications, will be available from both Lattice and its IP partners. Additional details of IP support will be announced during 2006.

Availability and Pricing

Samples of the first member of the LatticeECP2 family, the ECP2-50, will be made available during Q1 2006. The LatticeECP2-50 will be offered in 484 and 672 ball fpBGA package options. Lattice plans to introduce the entire LatticeECP2 family during 2006. The ECP2-50 will be priced as low as $23.95 in 100,000 unit quantities for delivery in 2007.

About Lattice Semiconductor

Lattice Semiconductor Corporation provides the industry's broadest range of Field Programmable Gate Arrays (FPGA) and Programmable Logic Devices (PLD), including Field Programmable System Chips (FPSC), Complex Programmable Logic Devices (CPLD), Programmable Mixed-Signal Products (ispPAC®) and Programmable Digital Interconnect Devices (ispGDX®). Lattice also offers industry leading SERDES products.

Lattice is "Bringing the Best Together" with comprehensive solutions for system design, including an unequaled portfolio of non-volatile programmable devices that deliver instant-on operation, security and "single chip solution" space savings.

Lattice products are sold worldwide through an extensive network of independent sales representatives and distributors, primarily to OEM customers in communications, computing, industrial, consumer, automotive, medical and military end markets. Company headquarters are located at 5555 NE Moore Court, Hillsboro, Oregon 97124-6421, USA; telephone 503-268-8000, fax 503-268-8037. For more information about Lattice Semiconductor Corporation, visit http://www.latticesemi.com

This release contains forward-looking statements that involve estimates, assumptions, risks and uncertainties. Many factors could cause actual results to differ materially from those expressed in such statements. With regard to statements herein concerning the timing of the introduction of new products, product features and product support, the release of such products will depend on a number of technical factors including timely and efficient completion of product design and software, timely and efficient implementation of wafer manufacturing and assembly processes for our new products and effective cooperation with our wafer suppliers and assembly contractors. With regard to statements herein concerning product pricing, the semiconductor industry is characterized by intense competition. The pricing of Lattice's products depends on a number of factors, including actions taken by our competitors, market acceptance of, and demand for, our products, product performance and manufacturing yields. In addition to the foregoing, other key factors that could cause our actual results to differ materially from the forward-looking statements herein are detailed in the Company's periodic reports filed with the Securities and Exchange Commission. Actual results may differ materially from forward-looking statements.

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