HDR Video Camera Development Kit and Evaluation Reference Design Now Available for LatticeECP3 FPGA Family

February 22, 2011

Production-Ready Kit and FPGA Reference Design Accelerate Time-to-Market and Enable Full HD HDR Camera Designs at Lowest System Cost

HILLSBORO, OR, Feb 22, 2011 (MARKETWIRE via COMTEX) --

Lattice Semiconductor Corporation (NASDAQ: LSCC) today announced the release of the Lattice HDR-60 Video Camera Development Kit, a production-ready High Definition (HD) video camera development system based on the LatticeECP3(TM) FPGA family. Pre-loaded with a plug and play evaluation Image Signal Processing (ISP) pipeline based on Intellectual Property (IP) Cores from Lattice partner Helion GmbH, the Kit works right out of the box. The IP is capable of delivering 1080p performance at 60 frames per second with 2D noise reduction and High Dynamic Range (HDR). Designed with a form factor to fit into commercially available camera housings and capable of supporting two sensors simultaneously, the Kit enables rapid evaluation and prototyping of high-definition HDR video cameras for security and surveillance, traffic control, video conferencing and automotive applications. Schematics and layout files are available free to all purchasers, further accelerating time to market. The Lattice HDR-60 Video Camera Development Kit is priced at $399.

A video demonstration of the HDR Video Camera Development Kit can be viewed here: English - www.latticesemi.com/hdr60videoen Chinese - www.latticesemi.com/hdr60videocn Japanese - www.latticesemi.com/hdr60videojp

Images of the HDR Video Camera Development Kit can be viewed and downloaded here: www.latticesemi.com/hdr60images.

About the Lattice HDR-60 Video Camera Development Kit The Lattice HDR-60 Video Camera Development Kit has been designed using a LatticeECP3-70 FPGA; however, the ISP IP pipeline needed to implement a complete 1080p60 HDR camera requires only a 33K LUT LatticeECP3-35 device. The Development Kit offers camera manufacturers several unique benefits, including a fully integrated HDR image signal processing pipeline from sensor to HDMI/DVI display. Equipped with an Aptina 720p HDR sensor, with a 1080p HDR sensor planned in Q2 2011, the Kit also offers the industry's fastest auto-exposure, greater than 120dB system dynamic range, a highly efficient Auto White Balance algorithm and 2D noise reduction -- all in streaming mode through the FPGA without the need for an external frame buffer, enabling extremely low latency and further reducing system cost. On-board DDR2 memory also enables applications such as 3D noise reduction, image stitching from multiple sensors, image rotation and de-warping.

In addition to two USB ports, the Kit features a RJ45 Ethernet port, a Broadcom Broadreach(TM) PHY and a built-in BNC connector, offering support for Ethernet over RG6 coaxial cable for distances up to 700 meters at 100Mbps for customers incorporating compression encoders into their designs. The Development Kit also supports easy programming over standard low-cost USB cable.

"The Lattice HDR-60 Video Camera Development Kit enables us to accelerate our camera design cycles and gives us significant advantages in time to market," said Tian Guang, Chief Technical Officer of BOCOM Digital Technology, a leading innovative products and solution provider in urban surveillance, ITS and telematics systems in China. "The image quality and HDR performance offered by the IP are of a very high order, while its small footprint, fitting inside a LatticeECP3-35, allows us to offer our customers high quality, truly differentiated HD cameras with HDR at very low system cost." For more information about BOCOM, please visit www.bocom.cn.

The pre-loaded, production ready evaluation camera reference design included with the Kit is future-proof, containing IP capable of being parameterized to support sensors up to 16 megapixels to protect the customer's investment. In addition to the on-board HDR ISP pipeline reference design, the Kit is supported by a comprehensive ISP library. The ISP IP is available for licensing either standalone or bundled with devices from the award-winning, low-power LatticeECP3 FPGA family, depending on customer requirements.

"Our goal with the Lattice HDR-60 Video Camera Development Kit is to enable camera manufacturers to jump start their FPGA-based high definition camera programs by providing a high quality HDR Video Camera reference design engineered to minimize system BOM, while addressing both legacy infrastructure and future-proofing the customer's investment," said Niladri Roy, Senior Manager of product marketing at Lattice Semiconductor. "With full 1080p60 support and the ability to scale up to 16MP sensors, as well as support for Ethernet over coaxial cable, the Lattice HDR-60 Development Kit offers nearly twice the functionality at less than half the price of any comparable kit currently available."

For more information and how to order, visit: www.latticesemi.com/hdr60.

About the LatticeECP3 FPGA Family The LatticeECP3 FPGA family is comprised of the lowest power, SERDES-enabled FPGAs in the market today. The family's five FPGAs offer standards-compliant, multi-protocol 3.2G SERDES, DDR1/2/3 memory interfaces and high performance, cascadable DSP slices that are ideal for RF, baseband and image signal processing. Toggling at 1Gbps, the LatticeECP3 FPGAs also feature fast LVDS I/O as well as embedded memory of up to 6.8 Mbits. Logic density varies from 17K LUTs to 149K LUTs with up to 586 user I/O. The LatticeECP3 FPGA family is ideally suited for deployment in high volume cost- and power-sensitive video camera and display, wireline and wireless infrastructure

applications.

About Lattice Semiconductor Lattice is the source for innovative FPGA, PLD, programmable Power Management and Clock Management solutions. For more information, visit www.latticesemi.com. Follow Lattice via Facebook, RSS and Twitter.

EDITORIAL/READER CONTACT:
Brian Kiernan
Corporate Communications Manager
Lattice Semiconductor Corporation
503-268-8739 voice
503-268-8193 fax
brian.kiernan@latticesemi.com

SOURCE: Lattice Semiconductor Corporation

mailto:brian.kiernan@latticesemi.com