



New Release of Lattice Diamond Design Software Accelerates FPGA Design Optimization for Low Power and Cost Sensitive Applications

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HILLSBORO, OR, Dec 12, 2011 (MARKETWIRE via COMTEX) -- Lattice Semiconductor Corporation (NASDAQ: LSCC) today announced release 1.4 of its Lattice Diamond(R) design software, the design environment for Lattice FPGA products. Users of Lattice Diamond 1.4 software will benefit from several usability enhancements that make FPGA design exploration easier and reduce time to market.

In addition, Lattice Diamond 1.4 software enhances support for the MachXO2(TM) PLD family by providing final production timing, power models and bitstreams for the entire family, including the latest wafer-level chip scale packaged version of the LCMXO2-2000U and LCMXO2-1200U devices that are ideal for very high volume, cost- and power-sensitive applications. Also, using the Lattice Diamond 1.4 software, select customers can begin designing with the newly announced low cost, low power mid-range LatticeECP4(TM) FPGA family.

"Achieving timing closure in the shortest amount of time can be a significant challenge as users try to pack more and more functionality into a single FPGA. Lattice Diamond 1.4 software offers the right combination of FPGA tools with enhanced usability to rapidly close the timing of design critical paths, which is especially important for low power and cost-sensitive FPGA applications," said Mike Kendrick, Lattice's Director of Software Marketing.

Final Data Support for the MachXO2 PLD Family The Lattice Diamond design environment enables users to easily explore design alternatives as they target cost-sensitive, low power, high volume applications -- the type of applications ideally suited for the MachXO2 PLD family. Lattice Diamond 1.4 software now includes final data for timing, power, package and bitstream based on the actual silicon characterization of all the MachXO2 devices. The final simultaneous switching output (SSO) data is available for all packages (except the wafer-level chip scale package of the LCMXO2-2000U, which will be made available later). With Lattice Diamond 1.4 software, users can now design and analyze using the most current data when targeting MachXO2 devices.

Early Access to the New LatticeECP4 FPGA Family Announced on November 28th, the LatticeECP4 FPGA family redefines the low cost, low power mid-range FPGA market for cost and power-sensitive wireless, wireline, video and computing markets. Select customers will be able to use Lattice Diamond 1.4 software to design with these new devices. Lattice Diamond 1.4 provides a complete set of powerful tools specifically targeted to the LatticeECP4 family's unique logic fabric and its built-in hardened IP blocks to enable lower cost and lower power applications. In particular, a new System Planner tool aids optimizing resource usage, and multiple improvements have been made to the generation of DSP blocks.

Design Exploration Improves Time to Market Lattice Diamond 1.4 software now provides a report of device resources used by level of design hierarchy following either the synthesis or the map step (a process that maps the synthesis output to the device resources). Device resources can therefore be reported out as both logical (registers) and physical (slices) elements. This feature helps users quickly understand what parts of their design are using scarce device resources so that they can optimize the design for the targeted device. This information can be exported to a text or a CSV file to enable analysis in other tools.

To improve timing closure productivity, users can now set up the multi-PAR placement and routing tool to stop after either trying a maximum number of seeds (or starting points) or when the last seed run has resulted in timing closure -- whichever comes first. In order to perform design exploration even faster, these multi-PAR tasks can now be distributed to run in parallel on computers with a multi-core CPU.

In addition, users can employ the Run Manager tool to process multiple implementations (or design structures) in parallel and accelerate timing and utilization results for these multiple implementations. Users can individually control the maximum number of implementations and multi-PAR processes that can be run simultaneously. With Lattice Diamond 1.4, users can also compare run reports of multiple implementations side by side and easily determine the best implementation for their design.

Lattice Diamond 1.4 software also aids users who want to migrate their designs later to a lower cost device within the same device family while preserving the existing board layout. This capability has now been extended to all the Lattice device families supported by Lattice Diamond software.

Improved Ease of Use Lattice Diamond software is an intuitive user design environment that enables users to complete their design more quickly. With Lattice Diamond 1.4 software, the pin assignment Design Rule Check (DRC) engine has been redesigned and implemented for the LatticeECP3(TM), MachXO2 and LatticeSC(TM) device families to provide real-time as well as on-demand DRC during pin assignment and configuration, and a user-friendly report that helps identify and correct pin usage issues.

In addition, users of the Lattice Synthesis Engine (LSE) tool can now create and edit Synopsys Design Compiler (SDC) synthesis constraints in the new Lattice Design Constraints graphical editor. This editor automatically populates design clock, port and net names and provides real time syntax and semantic checks. It generates an SDC file that can be used with LSE.

Included with this release is the new Diamond Deployment Tool. It uses an intuitive wizard approach to create the appropriate device programming file in the format required by the user's deployment method. Along with Diamond Programmer, introduced with Lattice Diamond version 1.3, these two tools now include the most popular features of ispVM(TM) System software, but with a more intuitive workflow. The ispVM System software is the

comprehensive stand-alone device programming manager currently offered by Lattice. The Diamond Deployment Tool is a standalone tool available as an accessory in the Lattice Diamond environment.

Third Party Tool Support Lattice Diamond software incorporates Synopsys' Synplify Pro advanced FPGA synthesis for Windows and Linux. Aldec's Active-HDL Lattice Edition II simulator is also included for Windows.

In addition to the tool support for Lattice devices provided by the OEM versions of Synplify Pro and Active-HDL, Lattice devices are also available in the full versions of Synopsys Synplify Pro and Aldec Active-HDL. Mentor Graphics ModelSim SE and Precision RTL synthesis also support Lattice devices.

Pricing and Availability Lattice Diamond 1.4 software is available now for download from the Lattice website at <http://www.latticesemi.com/latticediamond/downloads/> for both Windows and Linux. Once downloaded and installed, the software can be used with either the Lattice Diamond free license or the Lattice Diamond subscription license. The Lattice Diamond free license can be immediately generated upon request from the Lattice website and provides no cost access to many popular Lattice devices such as the MachXO2 and MachXO(TM) device families, the LatticeXP2(TM) and LatticeECP2(TM) FPGA families as well as the Platform Manager(TM) devices. The Lattice Diamond free license enables Synopsys Synplify Pro for Lattice synthesis as well as the Aldec Lattice Edition II mixed language simulator.

Purchase of the Lattice Diamond subscription license enables all the features of the free license and adds support for all Lattice FPGAs, including the LatticeECP3 devices. Select customers are provided early access to LatticeECP4 device support. The Lattice Diamond subscription license price is \$895 per year.

About Lattice Semiconductor

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