Lattice Breaks the Rules With ECP5 FPGA Family for High-Volume Small-Cell, Microserver, Broadband Access & Video Applications

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New Family Combines 40% Lower-Cost, 30% Lower Power and 2X Functional Density in the Smallest Package to Meet the Unique Needs of Fast Growing High-Volume Markets

HILLSBORO, OR -- (Marketwired) -- 04/10/14 -- Lattice Semiconductor Corp. (NASDAQ: LSCC) today announced its ECP5™ family for small-cell, microserver, broadband access, industrial video and other high-volume applications where the lowest-possible cost, lowest-possible-power, and smallest-possible form-factor are crucial. The ECP5 Family 'breaks the rules' of conventional FPGA approaches to deliver a SERDES-based solution for designers to rapidly add features and functions to complement those delivered by ASICs and ASSPs, reducing development risk and quickly overcoming time-to-market challenges.

Lattice optimized the ECP5 family's architecture with the goal of delivering the best value below 100k LUTs for performing critical functions as a companion chip to ASICs and ASSPs. Achieving 40% lower cost than competing solutions, optimizations include small LUT4 based logic slices with enhanced routing architecture, dual-channel SERDES to save silicon real estate, and enhanced DSP blocks for up to 4x resource improvements.

"The ECP5 family breaks the rule that FPGAs should be the highest density, power hungry and expensive," said Lattice Semiconductor President and CEO Darin Billerbeck. "Lattice's newest family serves to provide customers with an ASIC/ASSP companion chip as the quickest path for removing development obstacles at a time when mobility and mobile infrastructure are driving the need for small size and low power in practically every facet of the electronics industry."

The global deployment of next generation telecommunications systems is driving small-cells into high-volume, access and networking equipment is becoming commoditized and video display technologies continue to advance. For each of these applications, FPGA capabilities in a tiny, low-cost form-factor burning just milli watts of power can eliminate many roadblocks for pursuing opportunities that would otherwise be ruled out due to ASIC development costs and schedules, or ASSP inflexibility and availability.

"The ECP5 family is everything we hoped it would be for enabling the connectivity solutions we need for a number of our upcoming products," said Product Director, Peter Lyhne Uhrenholt at TRIAX A/S, a global maker of products for the reception, processing and distribution of analogue and digital radio and television signals. "For these products, we are dealing with extremely tight design environments in terms of size, power and cost. The ECP5 family gives us the flexibility we need with the functionality required."

In wireless and wireline applications, the ECP5 family delivers an FPGA solution for enabling implementation of data path bridging and interfacing in a small, low-cost package. ECP5 FPGAs provide the flexible connectivity required in outdoor small-cells, at extremely low-cost. They can also enable a smart SFP (small form-factor pluggable) transceiver solution for broadband access equipment, including integrated operation and maintenance, in a compact 10mm x 10mm package.

Outside of communications, ECP5 devices offer low cost, low power PCI Express side-band connectivity for microservers. For industrial video cameras, ECP5 FPGAs can implement the entire image processing functionality in a device that consumes under 2W.

The ECP5 family is the only FPGA portfolio in the industry that enables 85k LUTs and SERDES in 10mm x 10mm packages, amounting to 2X the functional density of competing solutions. Smart ball depopulation further simplifies package integration with existing PCB technology and reducing overall system cost.

Enhancements leading to 30% lower total power than other FPGA solutions include stand-by mode operation of the individual blocks including SERDES, dynamic IO bank controllers and reduced operating voltage. This enables single channel 3.25Gpbs SERDES functions starting below 0.25W, and quad channel SERDES functions starting below 0.5W for supporting a broad range of interface standards, including DDR3, LPDDR3, XGMII and 7:1 LVDS, PCI Express, Ethernet (XAUI, GbE, SGMII) and CPRI.

To watch videos, see applications and learn more about the ECP5 family's capabilities, please visit www.latticesemi.com/ecp5.

Availability

The ECP5 FPGA family is supported today in the Lattice Diamond® Software Tool. Devices are available immediately with production-qualification scheduled for August 2014. For details, please visit www.latticesemi.com/ecp5.

About Lattice Semiconductor

Lattice Semiconductor (NASDAQ: LSCC) is the world's leading provider of ultra-low-power programmable IC solutions for makers of smartphones, mobile handheld devices, small-cell networking equipment, industrial control, automotive infotainment, and much more. With more than 1 billion units sold over the past 10 years, Lattice ships more FPGAs, CPLDs and Power Management solutions than any other programmable solutions vendor. For more information, visit www.latticesemi.com. You can also follow us via Twitter, Facebook, or RSS.

Source: Lattice Semiconductor Corporation