SECURITIES AND EXCHANGE COMMISSION
WASHINGTON, D.C 20549
FORM 10-K

COMMISSION FILE NUMBER: 0-18032

/X/ Annual report pursuant to Section 13 or 15(d) of the Securities Exchange Act of 1934 for the fiscal year ended April 1, 1995 or

/ / Transition report pursuant to Section 13 or 15(d) of the Securities Exchange Act of 1934
For the transition period from _____ to _____

LATTICE SEMICONDUCTOR CORPORATION

(Exact name of Registrant as specified in its Charter)

DELAWARE	93-0835214
(State of Incorporation)	(I.R.S Employer Identification No.)
5555 NE MOORE COURT, HILLSBORO, OREGON	97124-6421
(Address of principal executive offices)	(Zip Code)

Registrant's telephone number, including area code: (503) 681-0118

SECURITIES REGISTERED PURSUANT TO SECTION 12(b) OF THE ACT: NONE
SECURITIES REGISTERED PURSUANT TO SECTION 12(g) OF THE ACT:

Title of Class	Name of Exchange
Common Stock, $.01 par value	NASDAQ
Preferred Share Purchase Rights	None

Indicate by check mark whether the Registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the Registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days.

Yes X No

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of the Registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K.

Yes X No

As of May 26, 1995, the aggregate market value of the shares of voting stock of the Registrant held by non-affiliates was approximately $496 million. Shares of Common Stock held by each officer and director and by each person who owns 5% or more of the outstanding Common Stock have been excluded in that such persons may be deemed affiliates. This determination of affiliate status is not necessarily a conclusive determination for other purposes.

As of May 26, 1995, 19,111,517 shares of the Registrant's common stock were outstanding.

DOCUMENTS INCORPORATED BY REFERENCE

1. Portions of the Annual Report to Stockholders for the fiscal year ended April 1, 1995 are incorporated by reference in Part II hereof.

2. Portions of the definitive proxy statement of the Registrant to be filed pursuant to Regulation 14A for the 1995 Annual Meeting of Stockholders to be held on August 14, 1995 are incorporated by reference in Part III hereof.

LATTICE SEMICONDUCTOR CORPORATION
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PART I

ITEM 1. BUSINESS

GENERAL

Lattice Semiconductor Corporation ("Lattice" or "the Company") is the world's leading supplier of in-system programmable ("ISP-TM-") logic devices and pioneered the application of electrically erasable CMOS ("E(2)CMOS-Registered Trademark- ") technology to programmable logic. The Company designs, develops and markets both high- and low-density, high performance E(2)CMOS programmable logic devices ("PLDs") and related development system software. PLDs are standard semiconductor components which can be custom configured by the customer (typically an electronic system manufacturer) to perform specific logic functions. PLDs enable the customer to shorten design cycle times and reduce development costs. Lattice was founded in 1983 and is based in Hillsboro, Oregon.

PLD MARKET BACKGROUND

Three principal types of digital integrated circuits are used in most electronic systems: microprocessors, memory and logic. Microprocessors are used for control and computing tasks, memory stores programming instructions and data, and logic is employed to manage the interchange and manipulation of digital signals within a system. Logic circuits contain interconnected groupings of simple logical "AND" and logical "OR" functions, commonly described as "gates". Typically, complex combinations of individual gates are required to implement the specialized logic circuits required for systems applications. Unlike the microprocessor and memory markets, which are dominated by a relatively small number of standard circuit designs, the logic market is highly fragmented. As such, the logic design of an electronic system often provides a key opportunity for end product differentiation.

Logic circuits are found in a wide range of today's electronic systems including data processing, telecommunications, data communications, computer peripherals, instrumentation, industrial control and military systems. According to Dataquest Incorporated, logic accounted for approximately 31% of the estimated $79 billion worldwide digital integrated circuit market in 1994. The logic market encompasses, among other segments, standard transistor-transistor logic ("TTL"), custom-designed application specific integrated circuits ("ASICs", which include conventional gate-arrays, standard cells and full custom logic circuits), and PLDs. Logic circuits are often classified by the number of gates per circuit with TTL circuits typically containing up to 100 gates, PLDs offering up to 20,000 gates, conventional gate arrays reaching up to 100,000 gates and custom logic circuits reaching up to millions of gates.

Manufacturers of electronic systems are increasingly faced with the challenge of developing highly differentiated products that can be brought to market rapidly. Historically, these two objectives have been incompatible, as the improved performance and cost reductions facilitated by ASICs have been accompanied by long, expensive and risky ASIC development cycles. Manufacturers with a need to reach market quickly were often forced to use low gate capacity standard TTL circuits, which limited system performance and increased system size and cost.

Programmable logic addresses this inherent dilemma. PLDs are standard products, purchased by systems manufacturers in a "blank" state, that can be custom configured into a virtually unlimited number of specific logic circuits by programming the device with an electrical signal. Incorporation of PLDs into standard design methodologies gives system designers the ability to quickly create their own custom logic circuits, satisfying the dual goals of product differentiation and rapid time to market. Certain PLD products, including Lattice's, are reprogrammable, which means that the logic configuration can be modified, if needed, after the initial logic programming. This gives the system designer the valuable additional benefit of last minute design flexibility, further reducing risk and accelerating design cycle time. Currently, PLDs are used by the majority of electronic systems manufacturers for prototyping, pilot production and to a lesser extent, volume production applications.

Several common PLD device types currently coexist in the marketplace, each offering customers a particular set of benefits. These include low-density PLDs (less than 1,000 gates) and high-density PLDs (greater than 1,000 gates), which include both complex PLDs ("CPLDs", up to 15,000 gates) and field programmable gate arrays ("FPGAs", up to 20,000 gates).

Low-density devices are typically based on industry standard architectures and include the GAL-Registered Trademark- (Generic Array Logic) product family developed by Lattice. These architectures are familiar to most experienced system designers and are supported by simple, non-proprietary, widely available development tools. Offering the highest absolute performance and lowest cost per device, these products are the most effective PLD solution to support simple logic functions in all systems and complex logic functions in systems with fast clock rates, such as those supporting state-of-the-art microprocessors.

High-density devices are typically based on proprietary architectures and require support from sophisticated CAE (computer aided engineering) development tools. Due to their higher levels of logic integration, absolute performance levels typically lag those of state-of-the-art low-density PLDs by one or more technology generations. However, for implementation of complex logic functions that would otherwise require many low-density devices, high-density PLDs can provide system performance enhancement and power, cost and circuit board area savings to sophisticated customers who have made the requisite investment in CAE tools.

Depending on the desired specific logic function, either a CPLD or a FPGA will be the most efficient high-density architecture from a price/performance perspective. CPLDs are characterized by a regular building block structure of wide-input logic cells, termed macrocells, and use a centralized logic interconnect scheme. CPLDs are optimal for control logic applications, such as state machines, bus arbitration, encoders and decoders and sequencers. FPGAs are characterized by a narrow-input logic cell and use a distributed interconnect scheme. FPGAs are optimal for register intensive and data path logic applications such as interface logic and arithmetic functions. Lattice believes that the majority of high-density PLD customers utilize both CPLD and FPGA architectures within a single system design, partitioning logic functions across multiple devices to optimize overall system performance and cost.

Lattice currently participates in both the low-density PLD and high-density CPLD markets, offering broad product lines across each segment.

BUSINESS STRATEGY

Lattice's strategy is to offer a broad line of cost effective standard programmable devices based on innovative architectures which offer high performance, superior functionality and design flexibility through reprogrammable and in-system programmable technologies. The Company supports its programmable devices with low cost, high functionality, software development tools that are easily adopted and fully integrated with common third party CAE software development systems and platforms. Lattice believes that the delivery of superior product quality and customer service, as well as access to state-of-the-art technology and manufacturing capacity through strategic partnerships are critical factors in the successful execution of its strategy.

The Company believes that due to its current market share leadership in low-density CMOS PLDs, it has been successful in executing its strategy in the low-density PLD market. Lattice is applying a similar business strategy to the high-density PLD market which it entered in March 1992.

TECHNOLOGY

Lattice's PLD products incorporate several types of internal architectures, which, when combined with Lattice's advanced, proprietary process technology, provide performance, design flexibility and testability advantages for the customer.

PROCESS TECHNOLOGY: Lattice's current high- and low-density PLD offerings are based on the Company's proprietary E(2)CMOS manufacturing process technology, termed UltraMOS-Registered Trademark-. The Company's current mainstream processes, UltraMOS IV and UltraMOS V, are advanced sub-micron CMOS technologies. Lattice is currently in the process of developing on UltraMOS VI, an advanced sub-micron process technology designed to enhance product performance and densities.

The Company believes that E(2)CMOS is the preferred programmable technology for both high- and low- density PLDs due to its inherent performance, reprogrammablity and testability benefits.

In comparison to bipolar technology, historically the dominant technology for low-density PLDs, CMOS technology consumes less power and generates less heat while operating at comparable speed. Additionally, in contrast to one-time-programmable bipolar PLDs, CMOS PLDs are fully erasable and reprogrammable, providing significantly greater design flexibility and allowing the PLD manufacturer to fully test all programmable elements in a device prior to shipment. An alternative CMOS technology, EPROM (Erasable Read Only Memory), provides the same power usage benefits as E(2)CMOS, but requires ultraviolet light exposure for erasure, necessitating expensive quartz windowed packages and limiting testability. Antifuse and SRAM (Static Random Access Memory) technology, used primarily in the manufacture of high density FPGAs, offer certain advantages for very dense logic devices, but also have significant drawbacks when compared with E(2)CMOS. Antifuse technology is non-erasable, non-reprogrammable and subject to lengthy initial programming times that can hinder usage in volume production applications. SRAM technology is volatile (erases when electrical current is removed), and as such programmable SRAM products require additional memory circuitry, typically on a separate chip, to store programming code. This adds cost and printed circuit board area to a design, and results in the devices not being completely functional at initial system power-up.

IN-SYSTEM PROGRAMMABILITY: Lattice has also developed and patented a unique programming technology called in-system programmability ("ISP-TM-"). ISP, a proprietary circuit programming interface and algorithm, allows Lattice's PLDs to be programmed while on a printed circuit board, or "in-system", with a standard 5-volt electrical signal. Traditional non-volatile programmable logic technologies require a 12-volt signal and therefore must be removed from the printed circuit board and programmed using stand-alone, specialized programming hardware. In-system programming of logic provides significant customer value through increased design, manufacturing and product field support flexibility. Lattice customers use ISP technology to reduce the manufacturing and development costs associated with PLD programming, while also significantly reducing design, prototype and manufacturing cycle times. All of Lattice's high-density PLDs are available with ISP capability and the Company also offers its most popular low-density architecture, the GAL22V10, with ISP technology.

PRODUCTS

LOW DENSITY: Lattice offers a full line of low-density PLDs based on its 16 families of GAL products offered in over 150 speed, power, package and temperature range combinations. The majority of the Company's revenue is derived from these product families. GAL devices range in complexity from approximately 200 to 1,000 logic gates and are typically assembled in 20-, 24- and 28-pin standard dual in-line packages ("DIP") and in 20- and 28-pin standard plastic leaded chip carrier ("PLCC") packages. Lattice offers the industry standard GAL16V8, GAL20V8, GAL22V10, GAL20RA10 and GAL20XV10 architectures in a variety of speed grades, ranging up to an industry leading 5 nanosecond logic delay. Lattice also offers several innovative proprietary extension architectures, the GAL26CV12, GAL18V10, GAL16VP8, GAL20VP8, GAL6001/2, GAL16V8Z, GAL20V8Z and the ispGAL22V10, each of which is optimized for specific applications. These product families offer industry leading performance levels, typically up to 7.5 nanoseconds.

During fiscal 1995, the Company extended its GAL line by introducing a family of 3.3 volt industry standard architectures, the GAL16LV8, GAL20LV8 and GAL22LV10 in a variety of speed grades, ranging up to an industry leading 7.5 nanosecond performance. Offered with a range of power consumption specifications, these devices are targeted towards emerging low voltage system applications. The Company plans to continue to maintain a broad offering of performance leadership, standard and extension architecture low-density CMOS PLDs.

Lattice's GAL products are supported by industry standard software and hardware development tools marketed by independent manufacturers specifically for PLD applications.

HIGH DENSITY: In fiscal 1993, Lattice entered the high-density PLD market by releasing to production its ispLSI-Registered Trademark- 1000 product family. The ispLSI 1000 product family, based on an innovative proprietary CPLD architecture incorporating familiar GAL-like logic building blocks, offers performance of up to 110 MHz (10 nanoseconds), densities of 2,000 to 8,000 gates, and is available in surface mount packages ranging from 44- to 120-pins. The Company is currently shipping over 60 speed, package and temperature range combinations of the ispLSI 1000 family.

In fiscal 1994, the Company introduced two new ispLSI families, the 2000 and 3000 series. The ispLSI 2000 family, containing eight devices, targets CPLD performance leadership, providing speeds up to 154 MHz (5.5 nanoseconds), densities of 1,000 to 4,000 gates, and 44- to 128-pin standard surface mount packages. It is the first high-density PLD architecture capable of supporting advanced microprocessors operating at clock speeds over 75 MHz. The ispLSI 3000 family, initially containing six devices, incorporates a modified logic architecture to target CPLD density leadership while retaining high performance. It offers 8,000 to 14,000 gates with performance up to 110 MHz (10 nanoseconds). Available in 128- to 208-pin surface mount packages, the 3000 family also incorporates boundary scan test, an attractive feature that provides enhanced testing capabilities important for higher density circuits. The Company is currently shipping over 30 speed, package and temperature range combinations of the ispLSI 2000 and 3000 families. The Company plans to continue to introduce new families of high density products, as well as improving the performance of existing product families, to meet market needs.

All of Lattice's high-density products are supported by the Company's pDS-Registered Trademark- (programmable development system) and pDS+-TM- software development tools. First introduced in fiscal 1992, pDS software allows a customer to enter and verify a logic design, perform logic minimization, assign I/O ("input/output") pins and critical speed paths, and execute automatic place and route tasks. Designed to be a low cost, fully integrated development tool, pDS runs under the Microsoft Windows-TM-(1) operating system on a personal computer. First introduced in fiscal year 1994, pDS+ software supports most popular third party CAE development tool environments running on the PC, SUN and HP workstation platforms. Designed to provide a low cost method to incorporate Lattice's PLD products into standard development environments, pDS+ software (referred to as "fitters") leverage a customer's existing investment in third-party CAE tools. Lattice also provides ispCODE-TM- software, a product that supports programming of the Company's ISP devices.

During fiscal 1995, Lattice released new versions of all its existing pDS and pDS+ software development tools to enhance performance, functionality and ease of use. The Company introduced new pDS+ products supporting the Cadence, Data I/O Synario, Mentor Graphics, Minc, Orcad, and Synopsys third party CAE design tool environments. Lattice also enhanced its ISP support by releasing ispTEST-TM- software, a product that enables ISP to be integrated into automatic test equipment ("ATE") on the manufacturing floor. Currently ispTEST supports equipment from Genrad, Hewlett Packard, and Teradyne.

Lattice plans to continue to enhance and expand its development tool offerings during fiscal year 1996.

OTHER PRODUCTS: During fiscal 1994, the Company began shipments of the ispGDS-TM- (in-system programmable Generic Digital Switch), a family of in-system programmable switching matrices targeted toward mechanical dip switch replacement and connectivity applications. Lattice plans to continue to selectively leverage its programmable process technology and product architecture expertise to design and develop new in-system programmable products as opportunities arise.

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(1)Windows is a registered trademark of Microsoft Corporation.

PRODUCT DEVELOPMENT

Lattice places great emphasis on product development and believes that continued investment in the development of new products that exploit market trends is required to maintain its competitive position. If the Company were unable to successfully define, develop and introduce competitive new products in a timely manner its future operating results would be adversely affected. The Company's product development activities emphasize refinement of its E(2)CMOS process and ISP programming technology, performance enhancement and cost reduction of existing products, development of new products and variants of existing products, and extension and enhancement of its software development tools. Product development activities occur in Lattice's Hillsboro, Oregon headquarters, its Milpitas, California design center, and its Shanghai, China design center.

Research and development expenses were $22.9 million, $20.6 million and $16.5 million in fiscal years 1995, 1994 and 1993 respectively. Lattice expects to continue to make significant investments in research and development in the future.

OPERATIONS

Lattice does not directly manufacture its silicon wafers. The Company has historically maintained strategic relationships with larger semiconductor manufacturers in order to source its wafer fabrication, allowing Lattice to focus its internal resources on product, process and market development. The Company believes that these partners can continue to produce wafers at lower costs due to their advanced production facilities and manufacturing economies of scale. Assembly is also performed for Lattice by outside suppliers. Lattice performs most test operations and all reliability and quality assurance processes internally, as the Company believes it can add significant customer value in these areas. In fiscal 1994, Lattice became the first domestic PLD company to achieve ISO 9001 quality registration, an indication of the Company's high internal operational standards.

WAFER FABRICATION: Lattice's wafer requirements are being supplied by Seiko Epson Corporation ("Seiko") in Japan pursuant to an agreement with S-MOS Systems Inc. ("S-MOS"), a U.S. affiliate of Seiko. See "Licenses and Agreements-Seiko Epson/S-MOS" following for a description of contractual arrangements with Seiko and S-MOS. Daniel S. Hauer, a member of the Company's Board of Directors is Chairman of the Board of S-MOS. The Company also has a wafer supply agreement with Chartered Semiconductor Pte. Ltd. ("Chartered") in Singapore. See "Licenses and Agreements - Chartered". Wafer volumes, prices and terms are determined through periodic negotiations.

Due to the complexity of the manufacturing process and the extremely low defect tolerances associated with the manufacture of complex integrated circuits, Lattice considers the relationship with its wafer supplier to be critical to its success. State-of-the-art semiconductor manufacturing processes are sensitive to a wide variety of factors, including the level of contaminants in the manufacturing environment, impurities in the raw materials and the performance of the personnel and equipment employed. Through fiscal 1995, the Company has been successful in obtaining adequate wafer capacity commitments and has not experienced any material difficulties or delays in the supply of wafers. Presently, demand on wafer suppliers is growing and existing capacity commitments may not be sufficient to satisfy the Company's continued growth. Moreover, all of the Company's wafer requirements are currently supplied by Seiko Epson Corporation. Although the Company has existing wafer supply commitments from such supplier which it believes will be adequate through the second quarter of fiscal 1996, such supplier has recently indicated that it does not presently intend to supply wafers at increased levels. In the event the Company is unable to obtain additional wafers from an alternate supplier and Seiko continues to be unable to increase wafer supplies to the Company, the Company's ability to increase sales of its products would be adversely affected. In addition, there can be no assurance such supplier will not reduce its allocation of wafers to the Company in future periods or that any such reduction could be offset from alternative sources of supply. If such supplier were to reduce its wafer allocations to the Company and the Company were unable to replace such capacity through alternative sources of supply, sales of the Company's products would be materially adversely affected. Lattice also expects that, as is customary in the semiconductor business, it will in the future seek to convert its fabrication process arrangements to larger wafer sizes, to more advanced process technologies, or to new or additional suppliers in order to maintain or enhance its competitive position. Such conversions entail inherent technological risks that could adversely affect yields and delivery times, and have a material adverse impact on the Company's operating results.

ASSEMBLY: After wafer fabrication and initial testing, Lattice ships wafers to independent subcontractors for assembly. During assembly, wafers are separated into individual die and encapsulated in plastic or ceramic packages. Presently, the Company has qualified long term assembly partners in the United States, Hong Kong, the Philippines and South Korea. Although Lattice has not to date experienced significant problems or interruptions in supply from its assembly contractors, any prolonged work stoppages or other inability of the contractors to supply assembled products would have a serious adverse effect on the Company's operating results.

TESTING: Testing is performed after both wafer fabrication and assembly. Lattice electrically tests the die on each wafer prior to shipment for assembly. Following assembly, prior to customer shipment, each product undergoes final testing using sophisticated test equipment techniques and quality assurance procedures developed by the Company. Final testing on some products is performed at independent contractors in the United States, the Philippines and South Korea.

MARKETING, SALES, CUSTOMERS

Lattice sells its products directly to customers through a network of independent sales representatives and indirectly through a network of distributors. The Company utilizes a direct sales management and field applications engineering organization in combination with manufacturer's representatives and distributors to reach a broad base of potential customers. Lattice's customers are primarily original equipment manufacturers ("OEMs") in the fields of data processing, telecommunications, data communications, computer peripherals,

instrumentation, industrial controls and military systems. The Company believes its distribution channel is a cost effective means of reaching small and medium sized customers.

On April 1, 1995, the Company had 18 sales representatives and five distributors in the United States and Canada. In North America, Arrow/Schweber Electronics, Inc. ("Arrow"), Hamilton Hallmark, Insight Electronics, Inc. and Marshall Industries ("Marshall") provide nationwide distribution, while Future Electronics provides regional distribution coverage in Canada. Lattice has established sales channels in 25 foreign countries through a network of 29 sales representatives and distributors. Approximately one-half of Lattice's North American sales and most of its foreign sales are made through distributors.

Lattice protects each of its North American distributors and some of its foreign distributors against reductions in published prices, and expects to continue this policy in the foreseeable future. The Company also allows returns from distributors of unsold products under certain conditions. For these reasons, the Company does not recognize revenue until products are resold by these distributors.

Lattice provides technical and marketing assistance to its customers and sales force with engineering staff based in the Company's offices in Oregon, California and selected field sales offices. The Company maintains 16 domestic and international sales offices where Lattice's field sales managers and applications engineers are based. These offices are located in the metropolitan areas of Atlanta, Boston, Chicago, Dallas, Los Angeles, Minneapolis, New York, Orlando, Portland, Rochester, San Jose, Hong Kong, London, Munich, Paris, and Tokyo.

Foreign sales, including those to Canada, accounted for 47%, 43% and 45% of Lattice's total revenue in fiscal 1995, 1994 and 1993, respectively. Sales to Europe were $24.5 million, $16.1 million and $13.1 million, and to Asia were $40.6 million, $34.3 million and $32.7 million, in fiscal 1995, 1994 and 1993, respectively. Both foreign and domestic sales are generally invoiced in U.S. dollars with the exception of sales in Japan which are invoiced in yen. The Company's export sales are subject to risks common to all export activities, including governmental regulation and possible imposition of tariffs and other trade barriers. To date, Lattice has not experienced material difficulties because of foreign or domestic trade restrictions, however there can be no assurance that such restrictions will not adversely affect future operations.

Lattice's products are sold to a large and diverse group of customers. Two distributors accounted for approximately 12% and 11% of revenue in fiscal 1995, approximately 12% and 10% in fiscal 1994 and approximately 11% each in fiscal 1993. No individual customer accounted for more than 5% of revenue in fiscal 1995.

The Company's sales are primarily executed against purchase orders for standard products. Customers frequently revise quantities and delivery schedules, without penalty. Lattice therefore does not believe that backlog as of any given date is indicative of future revenue.

COMPETITION

The semiconductor industry overall is intensely competitive and is characterized by rapid technological change, rapid rates of product obsolescence and price erosion. Lattice's current and potential competitors include a broad range of semiconductor companies, ranging from very large, established companies to emerging companies, many of which have greater financial, technical, manufacturing and marketing resources than Lattice.

The principal competitive factors in the CMOS PLD market include product features, price, customer support, and sales, marketing and distribution strength. In the high-density segment, the availability of competitive software development tools is also critical. In addition to product features such as speed, power consumption, reprogrammability, design flexibility and reliability, competition in the PLD market occurs on the basis of price and market acceptance of specific products and technology. Lattice believes that it competes favorably with respect to each of these factors. The Company intends to continue to address these competitive factors by working to continually introduce product enhancements and new products, by seeking to establish its products as industry standards in their respective markets, and by working to reduce the manufacturing cost of its products over their life cycle.

In the low-density PLD market, Lattice competes primarily with Advanced Micro Devices ("AMD"), a leader in the PLD market. AMD, a licensee of the Company's GAL patents, competes in the E(2)CMOS PLD market with a full line of GAL-compatible PLDs. Several other semiconductor companies offer products based on similar and competing CMOS technologies and architectures, however, these companies typically do not offer full product lines.

In the high-density PLD market, Lattice competes directly with Altera Corporation, AMD, Atmel, Cypress Semiconductor and Xilinx who offer competing, non-compatible CPLD architectures based on similar and competing CMOS technologies. The Company competes indirectly with manufacturers of FPGA devices such as Actel, AT&T, and Xilinx as well as other semiconductor companies providing non-PLD based logic solutions. As Lattice and these other companies seek to expand their markets, competition may increase.

Although to date Lattice has not experienced significant competition from companies located outside the United States, such companies may become a more significant competitive factor in the future. As the Company and its current competitors seek to expand their markets, competition may increase. Any such increases in competition could have an adverse effect on the Company's operating results.

PATENTS

Lattice seeks to protect its products and wafer fabrication process technology primarily through patents, trade secrecy measures, copyrights, mask work protection, trademark registrations, licensing restrictions, confidentiality agreements and other approaches designed to protect proprietary information. There can be no assurance that others may not independently develop competitive technology not covered by the Company's patents or that measures taken by the Company to protect its technology will be effective.

Lattice holds 29 domestic and European patents on its PLD products and has a number of patent applications pending in the United States, Japan and under the European Patent Convention. There can be no assurance that pending patent applications or other applications that may be filed will result in issued patents, or that any issued patents will survive challenges to their validity. Although the Company believes that its patents have value, there can be no assurance that the Company's patents, or any additional patents that may be issued in the future, will provide meaningful protection from competition. Lattice believes its success will depend primarily upon the technical expertise, experience, creativity and the sales and marketing abilities of its personnel.

Patent and other proprietary rights infringement claims are common in the semiconductor industry. Lattice has received a letter from a semiconductor manufacturer stating that it believes a number of its patents, related to product packaging, cover products sold by Lattice. While the manufacturer has offered to license certain of such patents to Lattice, there can be no assurance, on this or any other claim which may be made against the Company, that Lattice could obtain a license on terms or under conditions that would not have a material adverse effect.

LICENSES AND AGREEMENTS

Lattice has entered into long-term supply relationships and/or technology and product cross-licensing agreements with Seiko Epson and S-MOS, Chartered, National Semiconductor Corporation ("National"), SGS-Thomson Microelectronics ("SGS-Thomson") and AMD. Certain of these agreements are described below.

SEIKO-EPSON/S-MOS: In 1991, the Company extended its rolling three-year manufacturing agreement with S-MOS for the production of wafers. Under the terms of the agreement, S-MOS, a U.S. affiliate of Seiko, has agreed to provide manufactured wafers to the Company in quantities based on four-month rolling purchase orders provided by the Company. The Company has committed to buy certain minimum quantities of wafers per month. See Note 8 of Notes to Consolidated Financial Statements. The Company's products are manufactured in Japan at Seiko's wafer fabrication facilities and delivered to the Company by S-MOS. For a significant portion of this supply, the Company has been informed that Seiko supplies wafers to S-MOS pursuant to a distribution agreement, but that Seiko is not obligated under that agreement to continue to supply wafers to S-MOS. Prices for the wafers obtained from S-MOS are reviewed periodically and may be adjusted to reflect prevailing currency exchange rates.

In July 1994, the Company entered into an advance production payment agreement with Seiko and S-MOS, under which it advanced to Seiko $42 million during fiscal 1995 to be used by Seiko to finance additional sub-micron semiconductor wafer manufacturing capacity. Under the terms of the agreement, the advance is to be repaid in the form of sub-micron semiconductor wafers. Subject to certain conditions set forth in the agreement, Seiko has agreed to supply, and the Company has agreed to receive, such wafers at a price (in Japanese yen) and volume expected to achieve full repayment of the advance over a three to four year period. In conjunction with the advance production payment agreement, the Company also paid $2 million during fiscal 1995 for the development of sub-micron process technology and the fabrication of engineering wafers to be delivered over the same period. The agreement calls for wafers to be supplied by Seiko through S-MOS, pursuant to a purchase agreement with S-MOS. (See management's discussion and analysis of results of operations and notes to consolidated financial statements for more information related to these arrangements).

CHARTERED: In October 1990, Lattice entered into a five-year manufacturing agreement with Chartered for the production of wafers. However, the Company is not currently purchasing wafers from Chartered.

AMD: In November 1987, as part of the settlement of a patent infringement suit against Lattice, the Company and Monolithic Memories Inc. ("MMI", subsequently merged with AMD) entered into an agreement cross-licensing each other's patents covering programmable and reprogrammable logic devices based on patent applications having a first filing date prior to November 1989. The agreement was subsequently amended in May 1989 by Lattice and AMD, the successor to the rights and obligations of MMI in the original agreement. The amendment covers those patents relating to PLD products which are based on patent applications originally filed by Lattice, MMI and AMD prior to December 31, 1991. The license terminates, with respect to certain patents asserted by AMD, to cover Lattice's current principal products if the Company is acquired by a semiconductor manufacturer with sales in excess of a stated amount or by certain types of companies headquartered in designated Asian countries. No license has been granted to either party for any copyright work, trademark or process technology and, therefore, AMD has not been licensed to use the GAL trademark on its products.

FACTORS AFFECTING OPERATING RESULTS

The semiconductor industry is characterized by rapid technological change, intense competitive pressure and cyclical market patterns. Segments of the industry have historically experienced depressed business conditions during cyclical downturns. The Company's operating results are affected by a wide variety of external factors, including general economic conditions, conditions within the semiconductor industry, decreases in average selling prices over the life of any particular product, the timing of new product technologies and the rapid escalation of demand for certain products in the face of equally steep declines in demand for others. The Company attempts to promptly identify these changes in market conditions; however, the speed of change makes prediction of and reaction to such events difficult and there can be no assurance that the Company will be able to respond to such changes. Due to these and other factors, the Company's past results are a much less useful predictor of future results than is the case in more mature and less dynamic industries.

For further discussion refer to "Management's Discussion and Analysis of Financial Condition and Results of Operations" in the Company's 1995 Annual Report to Stockholders.

EMPLOYEES

As of April 1, 1995, Lattice had 438 full time employees. The Company believes that its future success will depend, in part, on its ability to continue to attract and retain highly skilled technical, marketing and management personnel.

None of the Company's employees is subject to a collective bargaining agreement. The Company has never experienced a work stoppage and considers its employee relations good.

ITEM 2. PROPERTIES.

The Company's corporate offices and testing and principal research and design facilities are located in two adjacent buildings owned by the Company in Hillsboro, Oregon comprising a total of 90,000 square feet. The Company's executive, administrative, marketing and production activities are also located at these facilities. The Company believes that its existing Oregon facilities will be adequate to meet its requirements for the foreseeable future. The Company also leases a 41,000 square foot research and design facility in Milpitas, California under a five-year lease which expires in August 1998.

The Company leases space in various locations in the United States for its domestic sales offices, and also leases space in Hong Kong, London, Munich, Paris and Tokyo for its foreign sales offices. The Company also owns a 13,000 square foot research and development facility and approximately 6,000 square feet of dormitory facilities in Shanghai.

ITEM 3. LEGAL PROCEEDINGS.

There are no material pending legal proceedings to which the Company is a party or to which any of its property is subject.

ITEM 4. SUBMISSION OF MATTERS TO A VOTE OF SECURITY HOLDERS.

Not applicable.

ITEM 4(a). EXECUTIVE OFFICERS OF THE REGISTRANT.

As of May 31, 1995, the executive officers of the Company are as set forth below.

Name	Age	Position
Cyrus Y. Tsui	49	President, Chief Executive Officer and Chairman of the Board
Albert L. Chan	45	Vice President, California Product Development
Stephen M. Donovan	44	Vice President, International Sales
Paul T. Kollar	49	Vice President, Sales
Steven A. Laub	36	Vice President and General Manager
Rodney F. Sloss	51	Vice President, Finance and Secretary

Jerry G. Taylor	46	Vice President, Oregon Product Development
Jonathan K. Yu	54	Vice President, Operations
Kenneth K. Yu	47	Vice President and Managing Director, Lattice Asia

Executive officers of the Company are appointed by the Board of Directors to serve at the discretion of the Board and hold office until the officers' successors are appointed.

Cyrus Y. Tsui joined the Company in September 1988 as President, Chief Executive Officer and Director, and in March 1991 was named Chairman of the Board. From 1987 until he joined the Company, Mr. Tsui was Corporate Vice President and General Manager of the Programmable Logic Division of AMD. He was Vice President and General Manager of MMI's Commercial Products Division from 1983 until the merger with AMD in 1987.

Albert L. Chan joined the Company in May 1989 as California Design Center Manager and has served since 1991 as Director, California Product Development Center. He was elected Vice President, California Product Development in August 1993. From 1988 until he joined the Company, Mr. Chan was Product Line Manager of the Programmable Gate Array Division of AMD. From 1983 to 1988 he held various engineering management positions at MMI and AMD.

Stephen M. Donovan joined the Company in October 1989 and has served as Director of Marketing and Director of International Sales. He was elected Vice President, International Sales in August 1993. Prior to joining the Company, Mr. Donovan served in several capacities at MMI and AMD, including Sales Director of the Major Accounts Group from 1988 to 1989, and General Manager, MMI Japan from 1986 to 1988.

Paul T. Kollar joined the Company in November 1985 and since that time has served as Vice President, Sales and Vice President, Sales and Marketing.

Steven A. Laub joined the Company in June 1990 as Vice President and General Manager. Prior to joining the Company, Mr. Laub was with Bain & Company, Inc., an international management consulting firm, from September 1983 to June 1990, most recently serving as a Vice President and senior member of the technology group.

Rodney F. Sloss joined the Company in May 1994 as Vice President, Finance and Corporate Secretary. From 1992 until he joined the Company, Mr. Sloss served as Chief Financial Officer of Alexander Haagen Company, a southern California based shopping center developer. He was a financial consultant with Sigoloff & Associates from 1990 to 1992, and from 1987 to 1990 Mr. Sloss served as Senior Vice President and Chief Financial Officer of Daisy Systems Corporation, a manufacturer of electronic design automation equipment.

Jerry G. Taylor joined the Company in May 1995 as Vice President, Oregon Product Development. From 1993 to until Mr. Taylor joined the Company, he pursued personal interests and was not engaged in business activities. From 1990 to 1993, Mr. Taylor was the Vice President of Product Development and Quality for Benchmarq Microelectronics, a semiconductor company founded in 1989 specializing in mixed signed products. Prior to that time, Mr. Taylor held senior management positions with Fairchild Semiconductor and Mostek Corporation.

Jonathan K. Yu joined the Company in February 1992 as Vice President, Operations. From 1987 until he joined the Company, Mr. Yu was President and Chief Executive Officer of Silicon Connections Corporation, a manufacturer of high speed BiCMOS logic and memory products. He served as President and Chief Operating Officer of Applied Micro Circuits Corporation, a manufacturer of high speed ASICs, from 1984 to 1987.

Kenneth K. Yu joined the Company in January 1991 as Director of Process Technology. He has served as Managing Director, Lattice Asia since November 1992 and was elected Vice President in August 1993. From 1987 to 1990 Mr. Yu was Vice President of Northwest Technology Group, a management and technology consulting firm. From 1984 to 1987 he served as Vice President of Development for Ateq Corporation, a manufacturer of high-speed laser lithography tools.

PART II

ITEM 5. MARKET FOR THE REGISTRANT'S COMMON STOCK AND RELATED STOCKHOLDER MATTERS.

The Company's common stock is traded on the over-the-counter market and prices are quoted on the NASDAQ National Market System under the symbol "LSCC". The following table sets forth the high and low sale prices for the common stock for the last two fiscal years and for the period since April 1, 1995. On June 19, 1995, the last reported sale price of the common stock was $35 1/4. All share prices have been adjusted for the three-for-two stock split effected in the form of a stock dividend which was paid on July 6, 1993. As of June 19, 1995, the Company had approximately 6,500 beneficial owners of its common stock.

	High	Low
Fiscal 1994:		
First Quarter	$20 13/16	$14 11/16
Second Quarter	26 3/4	14 3/4
Third Quarter	24 3/4	12 1/4
Fourth Quarter	19 3/8	14
Fiscal 1995:		
First Quarter	$19 5/8	$14 3/4
Second Quarter	20 1/8	17
Third Quarter	19 3/8	15 1/2
Fourth Quarter	27 1/8	16 3/8
Fiscal 1996:		
First Quarter (through June 19, 1995)	$35 5/8	$23

The payment of dividends on the common stock is within the discretion of the Company's Board of Directors. The Company intends to retain earnings to finance the growth of its business. The Company has not paid cash dividends on its common stock and the Board of Directors does not expect to declare cash dividends on the common stock in the near future.

ITEM 6. SELECTED FINANCIAL DATA.

The information required by this Item is set forth in the Company's 1995 Annual Report to Stockholders at page 17 under the caption "Selected Financial Data", which information is incorporated herein by reference.

ITEM 7. MANAGEMENT'S DISCUSSION AND ANALYSIS OF FINANCIAL CONDITION AND RESULTS OF OPERATIONS.

The information required by this Item is set forth in the Company's 1995 Annual Report to Stockholders at pages 14 through 16 under the caption "Management's Discussion and Analysis of Financial Condition and Results of Operations", which information is incorporated herein by reference.

ITEM 8. FINANCIAL STATEMENTS AND SUPPLEMENTARY DATA.

FINANCIAL STATEMENTS

The information required by this Item is set forth in the Company's 1995 Annual Report to Stockholders, at pages 17 through 24, which information is incorporated herein by reference.

No other schedules are included because the required information is inapplicable, not required or is presented in the financial statements or related notes thereto.

ITEM 9. CHANGES IN AND DISAGREEMENTS WITH ACCOUNTANTS ON ACCOUNTING AND FINANCIAL DISCLOSURE.

Not applicable.

With the exception of the information expressly incorporated by reference from the Annual Report to Stockholders into Parts II and IV of this Form 10-K, the Company's Annual Report to Stockholders is not to be deemed filed as part of this Report.

PART III

Certain information required by Part III is omitted from this Report in that the registrant will file its definitive proxy statement for the Annual Meeting of Stockholders to be held on August 14, 1995, pursuant to Regulation 14A of the Securities Exchange Act of 1934 (the "Proxy Statement"), not later than 120 days after the end of the fiscal year covered by this Report, and certain information included in the Proxy Statement is incorporated herein by reference.

ITEM 10. DIRECTORS AND EXECUTIVE OFFICERS OF THE REGISTRANT.

The information required by this item with respect to directors of the Company is included under "Proposal 1: Election of Directors" in the Company's Proxy Statement and is incorporated herein by reference. Information with respect to executive officers of the Company is included under Item 4(a) of Part I of this Report and is incorporated herein by reference.

ITEM 11. EXECUTIVE COMPENSATION.

The information required by this item with respect to executive compensation is included under "Proposal 1: Election of Directors," "Executive Compensation" and "Comparison of Total Cumulative Stockholder Return" in the Company's Proxy Statement and is incorporated herein by reference.

ITEM 12. SECURITY OWNERSHIP OF CERTAIN BENEFICIAL OWNERS AND MANAGEMENT.

The information required by this Item is incorporated herein by reference to the Company's Proxy Statement under the caption "Security Ownership of Certain Beneficial Owners and Management".

ITEM 13. CERTAIN RELATIONSHIPS AND RELATED TRANSACTIONS.

The information required by this Item is included under "Proposal 1: Election of Directors - Transactions with Management" in the Company's Proxy Statement and is incorporated herein by reference.

PART IV

ITEM 14. EXHIBITS, FINANCIAL STATEMENT SCHEDULES AND REPORTS ON FORM 8-K.

(a)(1) and (2) FINANCIAL STATEMENTS AND FINANCIAL STATEMENT SCHEDULES.

The information required by this item is included under Item 8 of this Report.

(a)(3) EXHIBITS.

3.1	Certificate of Incorporation, as amended (Incorporated by reference to Exhibit 3.1 filed with the Company's Annual Report on Form 10-K for the fiscal year ended March 31, 1990).
3.2	Bylaws, as amended (Incorporated by reference to Exhibit 3.2 filed with the Company's Annual Report on Form 10-K for the fiscal year ended March 30, 1991).
4.1	Preferred Shares Rights Agreement dated as of September 11, 1991 between Lattice Semiconductor Corporation and First Interstate Bank of Oregon, N.A., as Rights Agent (Incorporated by reference to Exhibit 1 filed with the Company's Registration Statement on Form 8-A on September 13, 1991).
10.1	Manufacturing and Technology Development Agreement dated October 31, 1990 between Chartered Semiconductor Pte. Ltd. and Lattice Semiconductor Corporation (Incorporated by reference to Exhibit 10.1 filed with the Company's Quarterly Report on Form 10-Q for the quarter ended December 29, 1990).(1)
10.2	Licensing, Co-development and Manufacturing Agreement between National Semiconductor Corporation and Lattice Semiconductor Corporation dated April 15, 1987 (Incorporated by reference to Exhibit 10.2, File No. 33-31231).(1)
10.3	Patent License Agreement dated November 10, 1989 between Monolithic Memories, Inc. and Lattice Semiconductor Corporation, as amended (Incorporated by reference to Exhibit 10.3, File No. 33-31231).(1)
10.4	Production and Non-exclusive License Agreement dated January 19, 1987 between Lattice Semiconductor Corporation and SGS Semiconductor Corporation (Incorporated by reference to Exhibit 10.4, File No. 33-31231).(1)
10.5	Manufacturing Agreement dated February 18, 1988 between Lattice Semiconductor Corporation and S-MOS Systems, Inc. (Incorporated by reference to Exhibit 10.5, File No. 33-35427).(1)

10.6	Extension effective December 31, 1990 to Manufacturing Agreement dated February 18, 1988 between Lattice Semiconductor Corporation and S-MOS Systems, Inc. (Incorporated by reference to Exhibit 10.6 filed with the Company's Annual Report on Form 10-K for the fiscal year ended March 30, 1991).
10.7	Form of Distributor Agreement (Incorporated by reference to Exhibit 10.6, File No. 33-31231).
10.8	Form of Representative Agreement (Incorporated by reference to Exhibit 10.7, File No. 33-31231).
10.9	* Lattice Semiconductor Corporation 1988 Stock Incentive Plan, as amended (Incorporated by reference to Exhibit 10.9 filed with the Company's Annual Report on Form 10-K for the fiscal year ended March 28, 1992).
10.10	* Form of Stock Option Agreement (Incorporated by reference to Exhibit 10.9, File No. 33-31231).
10.11	* Employment Letter dated September 2, 1988 from Lattice Semiconductor Corporation to Cyrus Y. Tsui (Incorporated by reference to Exhibit 10.10, File No. 33-31231).
10.12	Form of Proprietary Rights Agreement (Incorporated by reference Exhibit 10.11, File No. 33-31231).
10.13	* Outside Directors Compensation Plan (Incorporated by reference to Exhibit 10.12, File No. 33-31231).
10.14	* Amended Outside Directors Stock Option Plan (Incorporated by reference to Exhibit 10.13, File No. 33-35427).
10.15	* 1993 Outside Directors Stock Option Plan (Incorporated by reference to Exhibit 10.15 filed with the Company's Annual Report on Form 10-K for the fiscal year ended April 3, 1993).
10.16	* Employee Stock Purchase Plan, as amended (Incorporated by reference to Exhibit 10.16 filed with the Company's Annual Report on Form 10-K for the fiscal year ended April 3, 1993).
10.17	Advance Production Payment Agreement dated July, 5, 1994 among Lattice Semiconductor Corporation and Seiko Epson Corporation and S MOS Systems Inc. (1)
10.18	Engineering Payment Agreement dated July 5, 1994 among Lattice Semiconductor Corporation and Seiko Epson Corporation and S MOS Systems Inc.
11.1	Computation of Net Income Per Share.
13.1	1995 Annual Report to Stockholders

21.1	Subsidiaries of the Registrant.
23.1	Consent of Independent Accountants.
24.1	Power of Attorney (see page 21).
27	Financial Data Schedule for Twelve Months Ended April 1, 1995.

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(1) Pursuant to Rule 24b-2 under the Securities Exchange Act of 1934, confidential treatment has been granted to portions of this exhibit, which portions have been deleted and filed separately with the Securities and Exchange Commission.

* Management contract or compensatory plan or arrangement required to be filed as an Exhibit to this Annual Report on Form 10-K pursuant to Item 14(c) thereof.

(b) No reports on Form 8-K were filed during the last quarter of fiscal 1995.

(c) See (a)(3) above.

(d) See (a)(1) and (2) above.

SIGNATURES

Pursuant to the requirements of Section 13 or 15(d) of the Securities Exchange Act of 1934, the Registrant has duly caused this Report to be signed on its behalf by the undersigned, thereunto duly authorized, in the City of Hillsboro, State of Oregon, on the 23rd of June, 1995.

LATTICE SEMICONDUCTOR CORPORATION

By: /s/Rodney F. Sloss

Rodney F. Sloss, Vice President, Finance

POWER OF ATTORNEY

KNOW ALL PERSONS BY THESE PRESENTS, that each person whose signature appears below constitutes and appoints Cyrus Y. Tsui and Rodney F. Sloss, jointly and severally, his attorneys-in-fact, each with the power of substitution, for him in any and all capacities, to sign any amendments to this Report on Form 10-K, and to file the same, with exhibits thereto and other documents in connection therewith, with the Securities and Exchange Commission, hereby ratifying and confirming all that each of said attorneys-in-fact, or his substitute or substitutes, may do or cause to be done by virtue hereof.

Pursuant to the requirements of the Securities Exchange Act of 1934, this Report has been signed below by the following persons on the 23rd day of June, 1995 on behalf of the Registrant and in the capacities indicated:

SIGNATURE	TITLE
/s/Cyrus Y. Tsui Cyrus Y. Tsui	President, Chief Executive Officer and Chairman of the Board (Principal Executive Officer)
/s/Rodney F. Sloss Rodney F. Sloss	Vice President Finance (Principal Financial and Accounting Officer)
/s/Daniel S. Hauer Daniel S. Hauer	Director
/s/Harry A. Merlo Harry A. Merlo	Director

SIGNATURE	TITLE
/s/Larry W. Sonsini Larry W. Sonsini	Director
/s/Douglas C. Strain Douglas C. Strain	Director

121 S.W. Morrison Street Telephone: 503-224-9040
Suite 1800 Facsimile: 503-223-9051
Portland, Oregon 97204

PRICE WATERHOUSE LLP [LOGO]

REPORT OF INDEPENDENT ACCOUNTANTS ON FINANCIAL STATEMENT SCHEDULES

To the Board of Directors
of Lattice Semiconductor Corporation

Our audit's of the consolidated financial statements referred to in our report dated April 20, 1995 appearing on page 24 of the 1995 Annual Report to Stockholders of Lattice Semiconductor Corporation (which report and consolidated financial statements are incorporated by reference in this Annual Report on Form 10-K) also included an audit of the Financial Statement Schedules listed in Item 14(a) of this Form 10-K. In our opinion, these Financial Statement Schedules present fairly, in all material respects, the information set forth therein when read in conjunction with the related consolidated financial statements.

/s/ Price Waterhouse LLP

PRICE WATERHOUSE LLP

Portland, Oregon
April 20, 1995

Schedule VIII

LATTICE SEMICONDUCTOR CORPORATION

VALUATION AND QUALIFYING ACCOUNTS

(In thousands)

Column A Classification	Column B Balance at beginning of period	Column C Charged to costs and expenses	Column D Charged to other accounts (describe)	Column E Write-offs net of recoveries	Column F Balance at end of period
Year ended April 3, 1993:					
Allowance for doubtful accounts	$416	$601	$ -	$(394)	$623
Year ended April 2, 1994:					
Allowance for deferred tax asset.	-	$2,420	-	-	$2,420
Allowance for doubtful accounts	623	-	-	74	697
	$623	$2,420	$ -	$ 74	$3,117
Year ended April 1, 1995:					
Allowance for deferred tax asset.	$2,420	$399	-	-	$2,819
Allowance for doubtful accounts	697	75	-	(29)	743
	$3,117	$474	$ -	$(29)	$3,562

CONFIDENTIAL

ADVANCE PRODUCTION PAYMENT AGREEMENT

DATED JULY 5, 1994

AMONG

LATTICE SEMICONDUCTOR CORPORATION

AND

SEIKO EPSON CORPORATION

AND

S MOS SYSTEMS INC.

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EXHIBIT

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

ADVANCE PRODUCTION PAYMENT AGREEMENT

This Advance Production Payment Agreement ("APP Agreement"], is entered into this 5th day of July, 1994, by and among Seiko Epson Corporation, a Japanese corporation, having a place of business at 3-5, Owa 3-chome, Suwa-shi, Nagano-ken 392, Japan ("Epson"), S MOS Systems Inc., a California corporation, having a place of business at 2460 North First Street, San Jose, California 95131-1002, U.S.A. ("S MOS") and Lattice Semiconductor Corporation, a Delaware corporation, having a place of business at 5555 Northeast Moore Ct., Hillsboro, Oregon 97124-6421, U.S.A. ("Lattice").

1. BACKGROUND

1.1 EPSON. Epson is in the business of designing, manufacturing, testing and selling semiconductor devices, among other products. Epson manufactures such semiconductor devices at its plant located at 281 Fujimi, Fujimi-machi, Suwa-gun, Nagano-ken 399-02, Japan ("Fujimi Plant") and its plant located at 166-3 Jurizuka, Sakata-shi, Yamagata-ken 998-01, Japan ("Sakata Plant").

1.2 S MOS. S MOS is an affiliate of Epson and is Epson's authorized distributor in the United States for semiconductor devices. S MOS is in the business of designing, testing and selling semiconductor devices. S MOS conducts its business at its office located at 2460 North First Street, San Jose, California 95131-1002, U.S.A.

1.3 LATTICE. Lattice is in the business of designing, developing, manufacturing, marketing and selling both high-and low-density E(2)-CMOS(R) programmable logic devices ("PLDs").

1.4 SCOPE OF AGREEMENT. Epson and S MOS have an ongoing business relationship with Lattice whereby Epson fabricates semiconductor wafers for Lattice. The parties desire to expand this relationship. Specifically, Lattice desires to develop and sell high performance, advanced architecture PLDs and Epson desires to construct newly or additionally a 0.8-0.5 micron, 2-3 metal layer, 6 inch wafer CMOS process line installed in the Site (as hereafter defined) in order to fabricate such semiconductor wafers ("Products") and distribute them to Lattice through S MOS. Accordingly, the parties agree that Lattice will pay to Epson an advance production payment ("APP") only to be used as a credit to purchase the Products from Epson through S MOS over a specified period of time in accordance with APP Agreement. The Products shall be sold to S MOS from Epson under the terms and conditions of the Distributorship Agreement between the said parties dated April 1, 1988 as amended on September 10, 1991, and such Products shall be sold to Lattice from S MOS under the terms and conditions of the Purchase

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

Agreement (as hereafter defined). (In the event that S MOS has fallen into the situation that it could not play the role required under APP Agreement for any reason specifically prescribed in APP Agreement or any other reason, Epson and Lattice will mutually consult about the substitute form of the transaction contemplated herein.) Further, Lattice will pay a portion of certain engineering payment ("EP") incurred by Epson in connection with the fabrication of the Products in accordance with a separate agreement to be executed between the parties ("EP Agreement"). Prior to the execution of APP Agreement, Epson and Lattice have already executed a Letter of intent dated March 29, 1994 to agree on the essential terms of APP Agreement. This Letter of Intent is, however, to terminate at the time of the execution of APP Agreement.

1.5 POSITION OF S MOS. Notwithstanding any provision herein to the contrary, Lattice, Epson and S MOS acknowledge that although APP Agreement is executed by each of such three (3) parties, S MOS is a party hereto solely for the purpose to evidence its role, as the intermediary through which, under the terms of Purchase Agreement, the Products to be sold to Lattice by Epson will be sold, and to evidence S MOS's agreement to such an arrangement. S MOS shall under no circumstances have any rights under the APP and the EP Agreement (it being understood, however, that this Article 1.5 shall not in any way affect the rights of S MOS under the Purchase Agreement). In particular, and without limiting the generality of the foregoing, S MOS shall have no rights under Article 15 of APP Agreement (i.e., any reference to party or parties to APP Agreement shall be deemed to be only to Epson and Lattice unless specifically prescribed therein), and Epson and Lattice may amend APP Agreement in any respect. Epson agrees to cause S MOS to comply with all of the terms of the APP Agreement and the Purchase Agreement. Any material breach of the Purchase Agreement shall constitute a material breach to the APP Agreement for the purposes of Article 15.4 of the APP Agreement.

2. DEFINITIONS

2.1 "APP" will mean the advance production payment of Forty-Two Million US Dollars (US$42,000,000) to be made by Lattice to Epson in the manner described in Article 4.

2.2 "ENGINEERING WAFER" will mean the engineering wafers to be provided by Epson through S MOS free of charge as a consideration of Lattice's payment of the EP.

2.3 "EP" will mean the engineering payment of Two Million US Dollars (US$2,000,000) to be made by Lattice to Epson in the manner described in the EP Agreement.

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

2.4 "EP AGREEMENT" will mean the agreement under the terms of which Lattice shall make payment of the EP to Epson.

2.5 "EQUIPMENT" will mean the semiconductor fabrication equipment that Epson will install in the Facility for purpose of fabricating Facility Wafers.

2.6 "EXISTING AGREEMENTS" will mean those contracts for the development, fabrication, testing and/or sale of semiconductor devices between Epson and Lattice or S MOS and Lattice in effect as of the date of APP Agreement. Existing Agreements are listed on Exhibit A attached hereto.

2.7 "FACILITY" will mean the 0.8-0.5 micron, 2-3 metal layer, 6 inch wafer, CMOS process line already constructed or constructed newly or additionally at the Site using the Equipment.

2.8 "FACILITY WAFERS" will mean the semiconductor wafers to be fabricated by Epson for Lattice at the Facility of the types described in Exhibit B.

2.9 "FREE WAFERS" will have the meaning ascribed to them in Article 8.

2.10 "FUJIMI PLANT" will have the meaning ascribed to it in Article 1.1.

2.11 "OTHER EPSON AGREEMENTS" will mean the other agreements between Epson and Lattice contemplated hereby, including, without limitation, the EP Agreement and the agreement contemplated by Article 2.23.

2.12 "OTHER S MOS AGREEMENTS" will mean the other agreements between S MOS and Lattice contemplated hereby, including, without limitation, the EP Agreement and' the Purchase Agreement.

2.13 "OTHER LATTICE AGREEMENTS" will mean the other agreements between Epson and Lattice contemplated hereby, including, without limitation, the EP Agreement and the agreement contemplated by Article 2.23.

2.14 "PLDS" will have the meaning ascribed to it in Article 1.3.

2.15 "PRICE" will have the meaning ascribed to it in Article 11.1.

2.16 "PRODUCTS" will mean those specific types of Facility Wafers as described in Exhibit B.

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

2.17 "PURCHASE AGREEMENT" will mean the agreement by and between S MOS and Lattice pursuant to which S MOS agrees to sell and Lattice agrees to purchase the Products. It is the intention of the parties to execute the Purchase Agreement by July 29, 1994. In the event the parties do not enter into a mutually acceptable Purchase Agreement by such date, Lattice may terminate the APP Agreement and the EP Agreement by notice to Epson, in which event Epson shall return all payments previously made by Lattice thereunder within thirty (30) days of the date of such termination.

2.18 "PURCHASE COMMITMENT" will have the meaning ascribed to it in Article 7.1 and Exhibit C.

2.19 "SAKATA PLANT" will have the meaning ascribed to it in Article 1.1.

2.20 "SITE" will mean that portion of the Sakata and the Fujimi Plant where the Facility Wafers and certain type of Engineering Wafers will be fabricated.

2.21 "SUPPLY COMMITMENT" will have the meaning ascribed to it in Article 6.1 and Exhibit C.

2.22 "0.8-0.5 MICRON PROCESS" will mean the 0.8, 0.7, 0.6 and 0.5 micron, 2 and 3 metal layer, 6 inch wafer, E(2)CMOS processes as owned, licensed or developed by Epson which will be used at the Facility. The 0.8-0.5 Micron Process will include (a) all process flow, process steps, process conditions (and modifications thereto) used to manufacture semiconductor wafers at the Facility as well as (b) all methods, formulae, procedures, technology and know-how associated with such process steps and process conditions. The 0.8-0.5 Micron Process will not include any methods, formulae, procedures, technology and know-how licensed or received from Lattice under APP Agreement, the Existing Agreements or other agreements executed between the parties in the future unless otherwise agreed in writing. If the parties find it necessary or convenient to document process flow for any Product, such documentation will be signed by the parties and attached to the appropriate Purchase Agreement as an exhibit. 0.8-0.5 Micron Process herein, however, shall exclude the UltraMOS 5 Processes, UM5A and UM5C, and UltraM0S6 Processes, UM6C, UM6F and UM6CZ which shall be defined in Article 2.23 below.

2.23 "ULTRAMOS 5 PROCESSES, UM5A AND UM5C, AND ULTRAMOS 6 PROCESSES, UM6C, UM6F AND UM6CZ" will mean the 0.8, 0.7, 0.6 and 0.5 micron, 2 and 3 metal layer, 6 inch wafer E(2)CMOS processes in which Lattice's E(2) methods, formula, procedures, technology or know-how are merged with Epson's CMOS processes, and will be specified in Exhibit B. These processes are not to be used for the benefit of any Lattice's competitors of the PLDs. The detail of ownership and right to use these processes will be set forth in separate

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

agreement to be executed between Epson and Lattice, and such agreement shall supersede this Article 2.23.

3. CONSTRUCTION AND REPRESENTATION

3.1 CONSTRUCTION OF FACILITY

Epson hereby agrees, subject to its receipt of (a) the first installment as provided in Article 4.3 and (b) Lattice's commitment to make all other installments on a timely basis as provided in Article 4.3, to construct the Facility newly or additionally at the Site and to install the Equipment therein. Construction herein shall be made in accordance with the milestones described in Exhibit D. Epson covenants that these new or additional facilities will be capable of manufacturing semiconductor wafers meeting the requirements of the Products.

3.2 REPRESENTATIONS OF EPSON

In order to induce Lattice and S MOS to enter into APP Agreement and to make the APP hereunder, Epson hereby represents and warrants that:

3.2.1 CORPORATE STATUS. Epson (a) is duly organized, validly existing and in good standing under the laws of the jurisdiction of its incorporation, (b) has the corporate power to own or lease its assets and to transact business in which it is currently engaged and (c) is in compliance with all requirements of law except to the extent that the failure to comply therewith will not materially affect the ability of Epson to perform its obligations under APP Agreement or the Other Epson Agreements.

3.2.2 CORPORATE AUTHORITY. (a) Epson has the corporate power, authority and legal right to execute, deliver and perform APP Agreement and the Other Epson Agreements and has taken as of the date thereof all necessary corporate action to execute, deliver and perform APP Agreement and the Other Epson Agreements, (b) the person executing APP Agreement has, and each person who executes the Other Epson Agreements will at the time thereof have, actual authority to do so on behalf of Epson and (c) there are no laws, regulations or court orders and no outstanding assignments, grants, licenses, encumbrances, obligations or agreements, either written, oral or implied, that prohibit execution or performance of APP Agreement or the Other Epson Agreements.

3.2.3 OWNERSHIP OF THE SITE. Epson has such right, title and interest in and to the Site and the structures located thereon as is required to permit the operation of the Site as currently conducted and contemplated to be conducted under APP Agreement.

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

3.2.4 NO MATERIAL LITIGATION. No litigation, investigation or administrative proceeding is presently pending, or to the knowledge of Epson, threatened against Epson which, if adversely determined, would materially affect Epson's ability to carry out the terms and conditions of APP Agreement or the Other Epson Agreements. If such material litigation, investigation or administrative proceeding is commenced against Epson, Epson shall notify Lattice thereof within thirty (30) days of the commencement.

3.3 REPRESENTATIONS OF S MOS

In order to induce Lattice and Epson to enter into APP Agreement and to make the Supply Commitment, S MOS hereby represents and warrants that:

3.3.1 CORPORATE STATUS. S MOS (a) is duly organized, validly existing and in good standing under the laws of the jurisdiction of its incorporation, (b) has the corporate power to own or lease its assets and to transact business in which it is currently engaged and (c) is in compliance with all requirements of law except to the extent that the failure to comply therewith will not materially affect the ability of S MOS to perform its obligations under APP Agreement or the Other S MOS Agreements.

3.3.2 AUTHORITY. (a) S MOS has the corporate power, authority and legal right to execute, deliver and perform APP Agreement and has taken as of the date hereof all necessary corporate action to execute, deliver and perform APP Agreement or the Other S MOS Agreements, (b) the person executing APP Agreement or the Other S MOS Agreements has, and each person who executes the Other S MOS Agreements will at the time thereof have, actual authority to do so on behalf of S MOS and (c) there are no laws, regulations or court orders and no outstanding assignments, grants, licenses, encumbrances, obligations-or agreements, either written, oral or implied, that prohibit execution or performance of APP Agreement or the Other S MOS Agreements.

3.3.3 NO MATERIAL LITIGATION. No litigation, investigation or administrative proceeding is presently pending, or to the knowledge of S MOS, threatened against S MOS which, if adversely determined, would materially affect S MOS's ability to carry out the terms and conditions of APP Agreement or the Other S MOS Agreements. If such material litigation, investigation or administrative proceeding is commenced against S MOS, S MOS shall notify Lattice thereof within thirty (30) days of the commencement.

3.4 REPRESENTATIONS OF LATTICE

In order to induce Epson and S MOS to enter into APP Agreement and to make the Supply Commitment, Lattice hereby represents and warrants that:

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

3.4.1 CORPORATE STATUS. Lattice (a) is duly organized, validly existing and in good standing under the laws of the jurisdiction of its incorporation, (b) has the corporate power to own or lease its assets and to transact business in which it is currently engaged and (c) is in compliance with all requirements of law except to the extent that the failure to comply therewith will not materially affect the ability of Lattice to perform its obligations under APP Agreement or the Other Lattice Agreements.

3.4.2 CORPORATE AUTHORITY. (a) Lattice has the corporate power, authority and legal right to execute, deliver and perform APP Agreement and has taken as of the date hereof all necessary corporate action to execute deliver and perform APP Agreement and the Other Lattice Agreements, (b) the person executing APP Agreement has, and each person who executes the Other S MOS Agreements will at the time thereof have, actual authority to do so on behalf of Lattice and (c) there are no laws, regulations or court orders and outstanding assignments, grants, licenses, encumbrances, obligations or agreements, either written, oral or implied, that prohibit execution and performance of APP Agreement or the Other Lattice Agreements.

3.4.3 NO MATERIAL LITIGATION. No litigation, investigation or administrative proceeding is presently pending, or to the knowledge of Lattice, threatened against Lattice which, if adversely determined, would materially affect Lattice's ability to carry out the terms and conditions of APP Agreement or the Other Lattice Agreements. If such material litigation, investigation or administrative proceeding is commenced against Lattice, Lattice shall notify Epson and S MOS thereof within thirty (30) days of the commencement.

4. APP AND EP

4.1 APP. Lattice shall pay to Epson an amount equal to Forty-Two Million US Dollars (US$42,000,000) ("APP") or its equivalent amount in Japanese Yen, in the manner specified in Article 4.3, which APP will be credited against certain future purchases of Facility Wafers by Lattice as provided in Article 5.

4.2 EP. Lattice shall pay to Epson an amount equal to Two Million US Dollars (US$ 2,000,000) ("EP"), to be used in the manner provided in Article 9, and such payment shall be made in accordance with the EP Agreement.

4.3 APP INSTALLMENTS. Lattice will pay the APP in U.S. Dollars or its equivalent amount of Japanese Yen to Epson according to the following payment schedule (according to Japan time):

1st installment (US$ 10.5 million) on or before 7/12/94

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2nd installment (U$$ 10.5 million) on or before 9/27/94

3rd installment (US$ 10.5 million) on or before 1/10/95

4th installment (U$$ 10.5 million) on or before 3/28/95

4.4 PAYMENT METHOD. All payments made by Lattice to Epson will be in immediately available funds and will be made by wire transfer in US Dollars or its equivalent amount of Japanese Yen to the following bank account of Epson at:

Bank: Fuji Bank

Branch: Head Office (5-5, Otemachi l-chome, Chiyoda-ku, Tokyo 100, Japan)

Account Name: Seiko Epson Corporation

5. CREDIT OF APP

5.1 CREDIT OF APP. The purchase price of all Facility Wafers purchased by Lattice under the Purchase Agreements will be credited against the amount of the APP until the aggregate dollar value of all Facility Wafers (excluding the Free Wafers and the Engineering Wafers) purchased and received by Lattice, calculated pursuant to Article 5.2 and Exhibit E, equals or exceeds the APP. The APP shall be applied to the purchase orders issued by Lattice on or after July 12, 1994. The criteria and time required for wafer acceptance by Lattice will be described in the Purchase Agreement.

5.2 CALCULATION OF AGGREGATE CREDIT VALUE. The amount of the APP will be offset and reduced on a dollar for dollar basis, at the end of each calendar month of APP Agreement by an amount equal to the Price for the Facility Wafers multiplied by the total number of Facility Wafers (excluding the Free Wafers and the Engineering Wafers) shipped to Lattice pursuant to the Purchase Agreement during the previous calendar month with adjustment of the increase pursuant to the methods provided in the Purchase Agreement, however under no circumstances shall the APP balance be increased, except as provided for in Article 15.8 of the APP Agreement.

5.3 INVOICES. Epson will cause S MOS to provide Lattice with invoices under the Purchase Agreements which, for the purpose of APP application, specify the purchase price of the Facility Wafers. Also S MOS shall provide Lattice and Epson with the monthly report describing, among other things, the outstanding balance of the APP (after the application of all prior offsets, reductions and credits) as of the commencement of the month subject to the invoice, the number of Facility Wafers shipped to Lattice during that calendar month and the applied Price, and the outstanding

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balance of the APP as of the end of such calendar month. Such report shall be signed by the respective responsible person at Epson, S MOS and Lattice, provided that Lattice shall not be required to sign any such report unless it is satisfied with the accuracy and completeness thereof. Lattice may, for its signature, review all invoices and reports for its inaccuracies and also may request to make correction thereto if any inaccuracy was found by such review and Epson and S MOS confirm it.

6. SUPPLY COMMITMENT

6.1 CONTENTS OF SUPPLY COMMITMENT. It is the intent of Lattice to purchase and Epson to supply Facility Wafers until a total of seventy-two thousand (72,000) wafers (exclusive of Free Wafers and Engineering Wafers) have been supplied to Lattice by Epson through S MOS and received and accepted by Lattice ("Supply Commitment"). The Supply Commitment and the supply schedule thereof are set forth in Exhibit F. The Supply Commitment herein shall remain in effect until Lattice has received and accepted a total of seventy-two thousand (72,000) wafers (exclusive of the Free Wafers and the Engineering Wafers) through S MOS from Epson under APP Agreement. Dealing of wafers rejected by Lattice for any reason shall be described in the Purchase Agreement. The Supply Commitment for a particular month may be modified as specifically set forth in APP Agreement, but under no circumstances shall the aggregate Supply Commitment of seventy-two thousand (72,000) Facility Wafers be reduced.

6.2 PURCHASE AGREEMENTS. The Supply Commitment will apply to Products covered by all Purchase Agreements and Exhibit B. The parties anticipate that such Purchase Agreements will apply to PLDs distributed by Lattice which require fabrication using the 0.8-0.5 Micron Process. Epson will cause S MOS to execute the Purchase Agreement contemplated by this APP Agreement and all amendments and supplements thereto required to implement the intent of the APP Agreement.

6.3 EXCESS CAPACITY. Epson will use its best efforts to provide Lattice, through S MOS, with excess capacity for the Facility exceeding the Supply Commitment if Lattice requests so in the manner specified below. In this case, however, APP shall not be applied to the Lattice's orders of the Facility Wafers in excess of the Supply Commitment of the month and Lattice shall make regular payment for such excess volume of the Facility Wafers supplied by Epson according to the Price. Also the Free Wafers prescribed in Article 8 shall not be provided for such excess volume of the Facility Wafers.

First, in the event that Lattice desires to purchase Facility Wafers in excess of the Purchase Commitment, Lattice will specify

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in writing the amount of capacity required, the Product(s) it desires to purchase and the date from which such capacity is required and notify Epson of it through S MOS.

Second, Epson will then determine how much capacity is available and notify Lattice of its determination through S MOS. Epson will give Lattice priority over third parties for excess capacity of the Facility except to the extent that Epson is already obligated to provide such third parties with capacity.

Third, the parties will then mutually agree upon a preliminary excess capacity allocation. Any excess capacity allocated under this Article 6.3 will not be applied to the Supply Commitment and to the Purchase Commitment.

6.4 FAILURE TO MEET SUPPLY COMMITMENT

6.4.1 FAILURE DUE TO EPSON. In the event that (a) Epson fails to fulfill the Supply Commitment by the end of any month during the term of APP Agreement or (b) Epson has reason to believe that it will be unable to fabricate the Supply Commitment by the end of such month; then Epson will take the following measures:

First, Epson will promptly notify Lattice in writing and describe the nature of the difficulty.

Second, Epson will use its best efforts to remedy the difficulty in an expeditious manner by the end of the second full month following the month in which Epson is unable to meet the Supply Commitment (in other words, the third month including the month in which the difficulty occurs).

Third, Epson will use its best efforts to make available during the above-referenced three (3) month period sufficient capacity at the Sakata Plant and the Fujimi Plant to cover the deficiency between the Supply Commitment and the actual capacity. The parties acknowledge, however, that Epson cannot guarantee the use of existing capacity at the Sakata Plant or the Fujimi Plant.

Notwithstanding any provision to the Agreement to the contrary, in the event that Epson fails to fulfill the Supply Commitment (including any failure by virtue of the action or inaction of S MOS or any of the events described in Article 6.4.4), and is unable to cover the deficiency within the three (3) month period referenced above, such failure shall constitute a material breach of APP Agreement and Epson, S MOS and Lattice shall discuss the relief of such breach prior to Lattice's termination of APP Agreement based on the right permitted in Article 15.4 (which termination may be made without the notice and cure period contemplated by Article 15.4).

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6.4.2 FAILURE DUE TO LATTICE. Notwithstanding anything contained in Article 6.4.1 to the contrary, in the event that Epson fails to fulfill the Supply Commitment in any month due to (a) design defects in Products caused by Lattice, (b) design changes requested by Lattice, (c) process flow changes requested by Lattice or (d) any other reason caused by Lattice, Epson will only be required to make reasonable efforts to fulfill the Supply Commitment in such month, however Epson will be required to fulfill the Supply Commitment not affected by those causes above in accordance with this Article 6. Provisions concerning Lattice's failure to fulfill its Purchase Commitment are set forth in Article 7.3.

6.4.3 FAILURE DUE TO BOTH PARTIES. Notwithstanding anything contained in Articles 6.4.1, 6.4.2 or 7.1 to the contrary, in the event that Epson fails to fulfill the Supply Commitment and Lattice fails to fulfill the Purchase Commitment due to difficulties caused jointly by Lattice and Epson, the parties will mutually agree in writing upon a fair and equitable solution.

6.4.4 FAILURE DUE TO CATASTROPHE. In the event that any fire, flood, earthquake, explosion or any other catastrophe prevents Epson from fabricating Facility Wafers for Lattice, (a) Epson will immediately implement the measures required by Article 6.4.1, (b) Epson will permit Lattice to inspect the Facility, and (c) the parties will begin good faith negotiations to agree on a corrective action plan.

7. PURCHASE COMMITMENT

7.1 CONTENT OF PURCHASE COMMITMENT. Lattice intends to purchase each month the number of Facility Wafers ("Purchase Commitment") equal to the Supply Commitment. Lattice will not be required to fulfill the Purchase Commitment in the event that Epson cannot fulfill the Supply Commitment in the manner specified in Article 6.4.1. Instead, subject to the terms of the Purchase Agreement, Lattice will be required to purchase only those Facility Wafers that Epson is able to fabricate up to the Purchase Commitment for each month. Lattice will not be required to fulfill the Purchase Commitment because of difficulties caused by both Epson and Lattice. Instead, the parties will mutually agree in writing upon a fair and equitable solution.

7.2 SALE OF UNUSED CAPACITY. In the event that Lattice is unable to fulfill the Purchase Commitment in any month period for reasons not due to Epson, Epson will use its best efforts to sell unused capacity to other purchasers, to sell unused capacity to other customers, or to allocate unused capacity for the fabrication of Epson products during such month. Further, the Supply Commitment for such month will be reduced to the same extent that Lattice is unable to fulfill the Purchase Commitment. When Lattice desires

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to increase its monthly purchases after Epson has sold or otherwise allocated unused capacity, then Epson will use its best efforts to increase capacity for Lattice to the Supply Commitment in an expeditious manner. The parties will mutually agree upon the specific rate at which Epson will be required to ramp up capacity to the Supply Commitment.

7.3 FAILURE TO SELL UNUSED CAPACITY. In the event that Epson is unable to sell unused capacity or to allocate unused capacity for the fabrication of Products in the month described in Article 7.2, Epson may, but will not be required to, reduce its Supply Commitment in the two (2) full months thereafter to the same extent that Lattice is unable to fulfill the Purchase Commitment in the month described in Article 7.2. (In other words, Epson's Supply Commitment may be reduced for a three (3) month period including the month described in Article 7.2.) However, Epson will not impose any monetary penalty on Lattice for any failure to fulfill the Purchase Commitment. When Lattice desires to increase its monthly purchases after Epson has reduced the Supply Commitment, then Epson will use its best efforts to increase capacity for Lattice to the Supply Commitment in an expeditious manner not to exceed three (3) months (including the month in which Lattice requests an increase in capacity). The parties will mutually agree upon the specific rate at which Epson will be required to ramp up capacity to the Supply Commitment.

8. FREE WAFERS

As a consideration for Lattice's payment of the APP, Epson shall provide Lattice with [*] free wafers (in lieu of interest) of the Product ("Free Wafers") through S MOS pursuant to the Purchase Agreement for every 1,000 wafers of the Products ordered by Lattice after the execution of APP Agreement (1,000 wafers ordered PLUS [*] free wafers) until Epson has supplied the total of seventy-two thousand (72,000) Facility Wafers (excluding the Free Wafers and the Engineering Wafers).

9. EP

Lattice shall pay Epson Two Million US Dollars (US$2,000,000) as engineering payment ("EP") incurred by Epson in connection with the fabrication of the Products. In consideration of receipt of the EP, Epson agrees to fabricate for Lattice a certain volume of the Engineering Wafers for a certain period of time pursuant to the terms and conditions set forth in the EP Agreement.

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10. FABRICATION, PURCHASE AND SALE

10.1 GENERAL TERMS AND CONDITIONS. The terms and conditions for the prototype wafer fabrication, wafer fabrication, order and acceptance, shipping, insurance and warranty for the Products will be set forth in the Purchase Agreements. On behalf of Epson, S MOS shall sign all Purchase Agreements required to implement the terms and conditions of APP Agreement and Epson agrees to be bound thereby. Epson agrees to cause S MOS to provide all Products covered by APP Agreement in the manner required by the Purchase Agreements.

10.2 START OF PRODUCTION. Qualification testing for the Products will be conducted in the manner specified in the Purchase Agreements. Once any Product has been qualified, Epson will begin mass production of such Product in the manner specified by the Purchase Agreements.

11. PRICING AND PAYMENT

11.1 DETERMINATION OF PRICE. The general method for determining the price of the Products ("Price") shall be set forth in Exhibit G. Epson agrees that at any time the Prices shall be no greater than the prices charged by Epson to any third party. If Epson provides any third party with a lower price for particular type of the Facility Wafers than the Price, Epson shall promptly notify Lattice thereof and the prices to Lattice of such particular type shall be adjusted accordingly.

11.2 SHIPPING, INSURANCE, TAXES, DUTIES AND OTHERS. Epson will deliver the Products to S MOS on a C.I.F., San Jose basis, and S MOS will deliver such Products to Lattice on a F.O.B., San Jose basis. Bearing of sales, use, excise, ad valorem, withholding or other taxes or duties that may be applicable to purchase of the Products by Lattice shall be prescribed in the Purchase Agreement.

11.3 PAYMENT. Other than through offset of the APP, except the case prescribed in Article 6.3, Lattice will not be required to pay for any Facility Wafers delivered under APP Agreement or any Purchase Agreement until the APP has been fully offset and reduced. Once the APP is fully offset and reduced, Lattice will be required to pay in the manner specified in the Purchase Agreements.

12. TECHNICAL COOPERATION AND SUPPORT

The parties desire to engage in various types of joint development and technical cooperation activities required to fabricate Products and to effectuate the terms and conditions of APP Agreement. The parties, including S MOS, agree to negotiate in

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good faith joint development and technical cooperation agreements, including UM7, in the future.

13. INTELLECTUAL PROPERTY RIGHTS

All intellectual property rights relating to the 0.8-0.5 Micron Process and the Products will be set forth in the Purchase Agreements. Lattice agrees that any indemnity or warranty that Lattice expressly provides to Epson or S MOS under the Purchase Agreements will be fully enforceable by Epson even though Epson has not executed the Purchase Agreements. Furthermore, Epson agrees that any indemnity or warranty that Epson or S MOS purports to provide to Lattice under the Purchase Agreements will be fully enforceable by Lattice even though Epson has not executed the Purchase Agreements. In the event that any claims for intellectual property rights infringements described in the Purchase Agreements prevent the parties from fulfilling the Supply Commitment and the Purchase Commitment, the parties will mutually agree on a fair and equitable solution without affecting in any way the right of either party to terminate the Agreement for cause pursuant to Article 15.4 as a consequence of failure of the other party to fulfill the APP Agreement and the Purchase Agreement as the case may be. The parties acknowledge that the covenants contained in this Article 13 are an essential part of the Agreement.

14. CONFIDENTIAL INFORMATION

14.1 DEFINITION. "Confidential Information" means technical information, specifications, data, drawings, designs or know-how disclosed between Epson and Lattice, or S MOS and Lattice in connection with APP Agreement. Confidential Information includes information or material that is expressly covered by confidentiality provisions of Existing Agreements or the Purchase Agreements.

14.2 MARKING. If Confidential Information is provided in a tangible form, it will be marked as confidential or proprietary. If Confidential Information is provided orally, it will be treated as confidential and proprietary if it is treated as confidential or proprietary at the time of disclosure by the disclosing party and described in written English provided to the other party within thirty (30) days of the oral disclosure, which writing will be marked as confidential or proprietary. Material that is not marked as required by this Article 14.2 will not be deemed Confidential Information.

14.3 RESTRICTIONS ON USE. During the term of APP Agreement and for a period of five (5) years following termination hereof, the receiving party will: (a) hold the Confidential Information in

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confidence using the same degree of care that it normally exercises to protect its own proprietary information but no less than a reasonable degree of care, (b) restrict disclosure and use of Confidential Information solely to those employees (including any contract employees or consultants) of such party on a need-to-know basis, and not disclose it to other employees or parties, and (c) restrict the number of copies of Confidential Information to the number required to carry out its obligations under APP Agreement.

14.4 EXCEPTIONS TO CONFIDENTIALITY OBLIGATION. Neither party will use nor disclose the other party's Confidential Information except as permitted by APP Agreement. The receiving party, however, will have no obligations concerning the disclosing party's Confidential Information if the disclosing party's Confidential Information:

(a) is made public before the disclosing party discloses it to the receiving party;

(b) is made public after the disclosing party discloses it to the receiving party (unless its publication is a breach of APP Agreement or any other agreement between Epson and Lattice);

(c) is rightfully in the possession of the receiving party before the disclosing party discloses it to the receiving party;

(d) is independently developed by the receiving party without the use of the Confidential Information, if such independent development is supported by documentary evidence; or

(e) is rightfully obtained by the receiving party from a third party who is lawfully in possession of the information and not in violation of any contractual, legal or fiduciary obligation to the disclosing party with respect to the information.

Each party may disclose any Confidential Information to the extent that such party has been advised by counsel that such disclosure is necessary to comply with laws or regulations provided that such party shall give the other party reasonable advanced notice of such proposed disclosure, shall use its best efforts to secure confidential treatment of such Confidential Information, and shall advise the other party in writing of the manner of the disclosure.

14.5 RETURN OF CONFIDENTIAL INFORMATION. Upon termination of APP Agreement, a party who has received Confidential Information from the other party pursuant to APP Agreement will return, within fourteen (14) days of the disclosing party's request for return, all Confidential Information that the disclosing party delivered to the receiving party.

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15. TERM AND TERMINATION

15.1 TERM. The term of APP Agreement will be effective until (a) Epson's completion of the supply of, and receipt and acceptance by Lattice of, seventy-two thousand (72,000) Facility Wafers in total (excluding the Free Wafers and the Engineering Wafers), or (b) the completion of off-setting the APP, whichever occurs later. No notice or other action will be required for the automatic expiration described above.

15.2 TERMINATION. Either party may terminate APP Agreement effective immediately and without liability (except for the terms provided in Article 15.5 and 15.6) upon written notice to the other party if any one of the following events occurs:

(a) the other party files a voluntary petition in bankruptcy or otherwise seeks protection under any law for the protection of debtors;

(b) a proceeding is instituted against the other party under any provision of any bankruptcy laws which is not dismissed within ninety (90) days;

(c) the other party is adjudged bankrupt;

(d) a court assumes jurisdiction of all or a substantial portion of the assets of the other party under a reorganization law;

(e) a trustee or receiver is appointed by a court for all or a substantial portion of the assets of the other party;

(f) the other party becomes insolvent, ceases or suspends all or substantially all of its business;

(g) the other party makes an assignment of the majority of its assets for the benefit of its creditors;

(h) the other party fails to pay all or a substantial portion of its debts as they become due or admits in writing its inability to pay all or a substantial portion of its debts as they become due; or

(i) force majeure, as prescribed in Article 16.14, becomes in effect and will not be restored within six (6) months after such force majeure's occurrence.

15.3 TERMINATION DUE TO ACQUISITION OR SALE OF ASSETS. In the event that a direct competitor of one party acquires, through merger, consolidation, acquisition or otherwise, an interest in

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excess of fifty percent (50%) of the voting securities or assets of the other party, or the other party transfers all or substantially all of its business to which it relates to other than its Subsidiaries, the non-acquiring or non-transferring party will be permitted, upon written notice to the other party, to require that the transactions contemplated by APP Agreement and the Purchase Agreements be phased out and terminated at a rate not to exceed, per three month period, twenty-five percent (25%) of the business existing at the time of the acquisition or transfer according to the following schedule:

A *	B *
3 months	>75%
6 months	>50%
9 months	>25%
12 months	0%

A - Time elapsed since acquisition or transfer of assets

B - Level to which business may be phased out measured as a percentage of business existing at the time of the acquisition or transfer of assets

Alternatively, the business may be phased out and terminated under this Article 15.3 in a manner otherwise agreed upon in writing by the parties.

15.4 TERMINATION FOR CAUSE. If either party fails to perform or violates any material obligation of APP Agreement, then, sixty (60) days after providing written notice to the breaching party specifying the default ("Default Notice"), the non-breaching party may terminate this agreement, without liability, unless:

(a) the breach specified in the Default Notice has been cured within the sixty (60) day period; or

(b) the default reasonably required more than sixty (60) days to correct, and the defaulting party has begun substantial corrective action to remedy the default within such sixty (60) day period and diligently pursues such action, in which event, the non-breaching party may not terminate or suspend APP Agreement unless one hundred twenty (120) days has expired from the date of the Default Notice without such corrective action being completed and the default remedied.

15.5 TERMINATION BY EPSON. In the event that Epson terminates APP Agreement pursuant to this Article 15, then, unless otherwise agreed upon in writing, Epson may offset and reduce the APP to cover all direct material and labor costs for work in process

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rendered unusable by the termination and will ship such work in process to Lattice, at Lattice's expense, if requested to do so. Upon such termination, Epson shall refund the remaining portion of the APP (reduced by the amount of any such offset and reduction to cover direct material and labor costs for work in process rendered unusable by the termination) and also then-unused balance of the commitment for the Engineering Wafers calculated in accordance with Article 15.6 below no later than thirty (30) business days after the date of termination.

15.6 TERMINATION BY LATTICE. In the event that Lattice terminates APP Agreement pursuant to this Article 15, then, unless otherwise agreed in writing, Lattice may either (a) request that Epson refund the remaining portion of the APP (from which Epson may offset and reduce to cover all direct material and labor costs for work in process rendered unusable by the termination) and then Epson will refund the remaining portion of the APP (as so offset and reduced) or (b) request Epson to complete all work in process and ship them under normal terms and conditions, and then Epson will refund the remaining portion of the APP (excluding, without limitation, the costs and expenses arisen in connection with completing all work in process and shipping thereof), with in either such case such refund to be paid upon the earlier to occur of:

(a) receipt of sufficient funding from a financial institution or other source for purposes of paying the refund, or

(b) thirty (30) days from the date of termination.

Also the then-unused balance of the commitment for the Engineering Wafers shall be computed as follows and returned to Lattice within thirty (30) business days from the effective date of such termination; provided that any Engineering Wafers not supplied during any period specified in Article 2.2 of the EP Agreement, if any, shall be counted as already shipped by Epson in the said period in such computation:

[*]

15.7 RETENTION OF RIGHTS AFTER TERMINATION. Notwithstanding anything contained in this Article 15 to the contrary, in the event that either party is entitled to terminate APP Agreement pursuant to Articles 15.2 (f), (g) or (h) or either party is subject to a bankruptcy, reorganization or liquidation proceeding, the other party may elect to (a) retain its rights in APP Agreement existing immediately prior to termination pursuant to Article 15.2(f), (g) or (h) or the institution of such proceeding or (b) treat any such proceeding or attempted rejection of APP Agreement by a bankruptcy trustee as an event of termination. Unless otherwise provided, in

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the event of such termination, Epson shall refund the remaining portion of the APP in accordance with Article 15.5 and 15.6.

15.8 RECONCILIATION. In the event of termination that results in a refund of the APP balance pursuant to Article 15 (or would result in such a refund if the APP balance were increased by the net return material account balances, if any, under the Purchase Agreement), Epson shall cause S MOS to bring current the APP, Free Wafers, Engineering Wafers and return material account balances as provided for in the Purchase Agreement in order to reconcile the accounts with Lattice, and to refund the mutually agreed net amount.

15.9 SURVIVAL OF OBLIGATION. The following Articles will survive any expiration, termination or cancellation of APP Agreement and the parties will continue to be bound by the terms and conditions thereof: Articles 12, 13, 14, 15 and 16.

16. MISCELLANEOUS

16.1 ORDER OF PRECEDENCE. In the event of any conflicts between APP Agreement and any Purchase Agreement, any purchase orders, acceptances, correspondence, memoranda, listing sheets or other documents forming part of an order for the Products placed by Lattice and accepted by S MOS (or Epson), priority will be given first, to APP Agreement, second to the Purchase Agreement, third to S MOS's or Epson's acceptance, fourth to Lattice's order and then to any other documents. In no event, however, will Lattice's, S MOS's or Epson's standard terms and conditions be applicable to the transactions between Lattice and S MOS (or Epson).

16.2 GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the laws of California, U.S.A. without reference to conflict of law principals.

16.3 DISPUTE RESOLUTION

16.3.1 MEETING OF EXECUTIVES. In the event that any dispute or disagreement between the parties as to any provision of APP Agreement arises, prior to taking any other action, the matter will be referred to responsible executives of the parties for consideration and resolution. Any party may commence such proceedings by delivering a written request to the other party for a meeting of such responsible executives. The other party will be required to set a date for the meeting to be held within thirty (30) days after receipt of such request and the parties agree to exercise their best efforts to settle the matter amicably.

16.3.2 LOCATION OF MEETING. In the event that Epson initiates the proceedings described in Article 16.3.1, the first

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meeting will be held in Hillsboro, Oregon and all subsequent meetings will alternate between Tokyo, Japan, and Hillsboro, Oregon. In the event that Lattice initiates the proceedings described in Article 16.3.1, the first meeting will be held in Tokyo, Japan and all subsequent meetings will alternate between Hillsboro, Oregon and Tokyo, Japan.

16.3.3 DEMAND FOR ARBITRATION. If any dispute or disagreement hereunder is not settled within sixty (60) days from the initial meeting pursuant to Articles 16.3.1 and 16.3.2, such dispute or disagreement may, at the demand of either party, be referred to and decided by arbitration. The arbitration will be held in the country of the responding party. If the arbitration is to be held in Japan it will be conducted in Tokyo under the then current Rules of Arbitration of the International Chamber of Commerce in Japanese, with iterative translations into English. If the arbitration is to be held in the United States it will be conducted in Hillsboro, Oregon under the then current Rules of Arbitration of the International Chamber of Commerce in English, with iterative translations into Japanese.

16.3.4 ARBITRATORS. The arbitration will be conducted by three (3) arbitrators. No person with a beneficial interest in the dispute under arbitration may be an arbitrator. Such 3 arbitrators shall be (a) an arbitrator selected and appointed by Epson, (b) an arbitrator selected and appointed by Lattice and (c) an arbitrator selected and appointed by the arbitrators of Epson and Lattice.

16.3.5 BINDING EFFECT. The decision or award rendered or made in connection with such arbitration will be binding upon the parties and judgment thereon may be entered in any court having jurisdiction and/or application may be made to such court for enforcement of such decision or award. However, the arbitrators will not have the authority to create any licenses. They will only be permitted to enforce licenses which the parties have otherwise agreed to in the Agreement or the Existing Agreements.

16.3.6 EXPENSES. The expenses of the arbitrators will be shared equally by the parties; each party will otherwise be responsible for the costs and attorneys' fees incurred by it; provided, however, if the arbitrators appointed in Article 16.3.4 find that the position of the non-prevailing party or parties in such arbitration was without substantial justification or was frivolous, in which event the arbitrators may assess all of the costs and expenses together with reasonable attorney's fees against the non-prevailing party or parties.

16.4 CONSEQUENTIAL DAMAGES. IN NO EVENT WILL EITHER PARTY BE LIABLE TO THE OTHER PARTY FOR ANY INDIRECT, SPECIAL, CONSEQUENTIAL OR INCIDENTAL DAMAGES (INCLUDING LOST PROFITS) WHETHER BASED ON

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WARRANTY, CONTRACT, TORT OR ANY OTHER LEGAL THEORY REGARDLESS OF WHETHER SUCH PARTY HAD ACTUAL OR CONSTRUCTIVE NOTICE OF SUCH DAMAGES; PROVIDED, HOWEVER, THIS LIMITATION WILL NOT APPLY IF DAMAGES OCCUR AS A RESULT OF GROSS NEGLIGENCE OR WILLFUL MISCONDUCT OF EITHER PARTY IN THE PERFORMANCE OF THEIR RESPONSIBILITIES UNDER THIS AGREEMENT.

16.5 ASSIGNMENT. Neither party will assign, transfer or otherwise dispose of APP Agreement in whole or in part without the prior consent of other party in writing, and such consent will not be unreasonably withheld; provided that, in case of Lattice, APP Agreement may be assigned to any successor entity, whether by merger, consolidation, acquisition of all or substantially all of the assets of Lattice. Upon the completion of such assignment, Lattice shall promptly provide a written notice to, Epson.

16.6 PUBLIC ANNOUNCEMENTS. Neither party will publicly announce the execution or existence of APP Agreement or disclose the terms and conditions of APP Agreement without first submitting the text of such announcement to the other party and receiving the approval of the other party of such text, which approval, unless public disclosure is required by a court or a government agency or by applicable law, may be withheld for any reason. However, Lattice may disclose the existence and the terms of APP Agreement in any document legitimately required to be filed with the Securities and Exchange Commission (and may file a copy of the APP Agreement required legitimately with such filing) or in accordance with the generally accepted accounting procedures under the rules of the Securities and Exchange Commission or National Association of Securities Dealers Automated Quotations.

16.7 NOTICE AND COMMUNICATION. Any notices required or permitted to be given hereunder will be in English and be sent by (i) registered airmail or (ii) cable, facsimile or telex to be confirmed by registered airmail, addressed to:

to Epson: 281 Fujimi, Fujimi-machi,
Suwa-gun, Naganoken 399-02, Japan
Attn: Saburo Kusama
Managing Director,
Co-Chief Operation Officer and
General Manager of the
Semiconductor Operations Division
Tel: 81-266-61-1211
Fax: 81-266-61-1270

to S MOS: 2460 North First Street
San Jose, California 95131-1002, U.S.A.
Attn: Dan Hauer, President
Tel: 1-408-922-0200
Fax: 1-408-922-0238

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

to Lattice: 5555 Northeast Moore Ct.
Hillsboro, Oregon 97124-6421, U.S.A.
Attn: Cyrus Tsui
President and Chief Executive Officer
Tel: 1-503-681-0118
Fax: 1-503-681-3077

Any such notice will be deemed given at the time of its receipt by the addressee.

16.8 RELATIONSHIP OF THE PARTIES. Epson and Lattice are independent contractors and neither of them will be nor represent themselves to be the legal agent, partner or employee of the other party for any purpose. Neither party will have the authority to make any warranty or representation on behalf of the other party nor to execute any contract or otherwise assume any obligation or responsibility in the name of or on behalf of the other party, except to the extent as specifically authorized in writing by the other party. In addition, neither party will be bound by, nor liable to, any third person for any act or any obligation or debt incurred by the other party, except to the extent specifically agreed to in writing by the parties.

16.9 WAIVER AND AMENDMENT. Failure by either party, at any time, to require performance by the other party or to claim a breach of any provision of APP Agreement will not be construed as a waiver of any right accruing under APP Agreement, nor will it affect subsequent breach or the effectiveness of APP Agreement or any part hereof, or prejudice either party with respect to any subsequent action. A waiver of any right accruing to either party pursuant to APP Agreement will not be effective unless given in writing.

16.10 SEVERABILITY. In the event that any provision of APP Agreement will be unlawful or otherwise unenforceable, such provision will be severed, and the entire agreement will not fail on account thereof, the balance continuing in full force and effect, and the parties will endeavor to replace the severed provision with a similar provision that is not unlawful or otherwise unenforceable.

16.11 RIGHTS AND REMEDIES CUMULATIVE. The rights and remedies provided herein will be cumulative and not exclusive of any other rights or remedies provided by law or otherwise.

16.12 HEADINGS. The Article headings in APP Agreement are for convenience only and will not be considered a part of, or affect the interpretation of, any provision of APP Agreement.

16.13 GOVERNING LANGUAGE. This Agreement and all communications pursuant to it will be in the English language. If

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

there is any conflict between the English version and any translated version of APP Agreement, the English version will govern.

16.14 FORCE MAJEURE. Except as otherwise expressly provided for herein, no party will be liable in any manner for failure or delay in fulfillment of all or part of APP Agreement directly or indirectly owing to any causes or circumstances beyond its control, including, but not limited to, acts of God, governmental order or restrictions, war, war-like conditions, hostilities, sanctions, revolution, riot, looting, strike, lockout, plague or other epidemics, fire and flood.

16.15 COUNTERPARTS. This Agreement may be executed in any number of counterparts, and each such counterpart hereof will be deemed to be an original instrument, but all such counterparts will together constitute but one Agreement.

16.16 INTEGRATION. This Agreement sets forth the entire agreement and understanding between the parties as to its subject matter and supersedes all prior agreements, understandings and memoranda between the parties, except for the Existing Agreements. No amendments or supplements to APP Agreement will be effective for any purpose except by a written agreement signed by the parties.

16.17 GOVERNMENT APPROVALS; EXPORT CONTROL LAWS. Epson will file all reports and notifications that may be required to be filed with any agency of the Government of Japan in order to allow the performance of APP Agreement according to its terms. Lattice will file all reports and notifications that may be required to be filed with any agency of the Government of U.S.A. in order to allow the performance of APP Agreement according to its terms. Neither party will transmit indirectly or directly any Products or technical information contained in the Confidential Information except in accordance with applicable Japanese and American export control laws, regulations and procedures.

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

IN WITNESS WHEREOF, the parties have signed APP Agreement as of the date first above written.

SEIKO EPSON CORPORATION

By: /s/ SABURO KUSAMA

Name: Saburo Kusama

Title: Managing Director, Co-Chief Operating Officer and General Manager of Semi-conductor Operations Division

LATTICE SEMICONDUCTOR CORPORATION

By: /s/ CYRUS TSUI

Name: Cyrus Tsui

Title: President and CEO

S MOS SYSTEMS, INC.

By: /s/ DAN HAUER

Name: Dan Hauer

Title: President

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

EXHIBIT A

EXISTING AGREEMENTS

MANUFACTURING AGREEMENT

BETWEEN

LATTICE SEMICONDUCTOR CORPORATION

AND

S-MOS SYSTEMS, INCORPORATED

As Amended on

April 10, 1991

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

EXHIBIT B

"PRODUCTS"

TYPE	PROCESS TECHNOLOGY
UM5A	Transistor Feature Size = 0.65 um Basical Design Rule = 0.80 um 5V operation
UM5C	Transistor Feature Size = 0.65 um Basical Design Rule = 0.72 um 5V operation
UM6C (with UM5 metal module)	Transistor Feature Size = 0.5 um Basical Design Rule = 0.72 um 3V operation
UM6C (with "New" metal module)	Transistor Feature Size = 0.5 um Basical Design Rule = 0.6 um 3V operation, New Metal Module
UM6F	Transistor Feature Size = 0.6 um Basical Design Rule = 0.6 um 5V operation, New Metal Module
UM6CZ	Transistor Feature Size = 0.5 um Basical Design Rule = 0.6 um 3V operation, New Metal Module

+ In addition to Products above, their derivatives are also included in the Products.

+ New Metal Module means metalization process technology using Organic SOG for IMD and BPSG for ILD.

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EXHIBIT C

"SUPPLY/PURCHASE COMMITMENT"

WAFER VOLUME PER MONTH

Jun. 94-Sep. 94	Oct. 94-Mar. 95	Apr. 95-Mar. 96	Apr. 96-Mar. 97	Apr. 97-Mar. 98
[*]	[*]	[*]	[*]	[*]

+ The committed investment capacity of [*] wafers per month shall be divided between Sakata and Fujimi in a mutually agreeable manner by both parties, providing that the process control capabilities and defect densities are the same within practical limits at the two facilities.

+ This table is based on wafer start date.

+ Supply/Purchase Commitment will expire when a total of 72,000 Facility Wafers has been fulfilled as described in Article 6.1 and 7.1 (in any case, excluding Free Wafers and Engineering Wafers). Once 72,000 of Facility Wafers have been supplied and purchased before March 1998, the above table will not be applied to the parties after that time. But in the case that a total of the Facility Wafers supplied and purchased does not reach 72,000 on March, 1998, Supply/Purchase Commitment will continue until 72,000 of the Facility Wafers have been fully supplied and purchased.

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EXHIBIT D

"PROJECTED COMPLETION SCHEDULE"

+ Construction Schedule of new or additional Facilities at Sakata and Fujimi.

	Item		Sakata and Fujimi
1.	Agreement (signing up)		July 5, 1994
2.	Utility Construction	Finish	Jan. 1995
3.	Equipment Installation and Connection	Finish	Apr. 1995
4.	Equipment Characterization and Qualification	Finish	Jun. 1995
5.	Products Production		
	1st 500WFs	Start	Jul. 1995
	1st 500WFs	Shipment	Sep. 1995
	1st 1000WFs	Shipment	Oct. 1995
	1st 1500WFs	Shipment	Nov. 1995
	1st 2000WFs	Shipment	Dec. 1995

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EXHIBIT E

"APP CREDIT METHOD"

1. Lattice will pay each amount of the Advance Payment in U.S. dollars to Epson in the manner specified in Article 4.3. All parties will have the balance book for this Advance Payment on U.S. dollar basis

2. The aggregate Yen value of the Products shipped from S MOS to Lattice in each month will be converted into the equivalent amount of dollar by applying the exchange rates defined in item 3. And this value will be rounded to three decimal places.

3. For the calculation of item 2, the parties agree to use the closing price of prime foreign exchange rate at Tokyo Market on the final business day of the previous month. This exchange rate is specified in the Japanese newspaper "NIHON KEIZAI SHIMBUN". Epson shall inform Lattice and S MOS of this exchange rate and send a copy of the newspaper within two weeks from the first day of each month.

4. The Dollar amount determined in item 2 above will be used to offset and reduce the Advance Payment on the monthly basis. S MOS shall provide Lattice and Epson with a monthly report of all Products shipped to Lattice during the proceeding month in the manner specified in Article 5.3. This report will be signed by responsible personnel of Epson, S MOS and Lattice after review and acceptance.

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

EXHIBIT F

"SUPPLY SCHEDULE"

Start of [*] wafer fabrication Jun. 1994; ship in Aug. 1994

Start of [*] wafer fabrication Oct. 1994; ship in Dec. 1994

Start of [*] wafer fabrication Apr. 1995; ship in Jun. 1995

Start of first [*] wafer fabrication Apr. 1996; ship in Jun. 1996

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

EXHIBIT G

"PRICE"

1. For Facility Wafers covered by the Supply Commitment
(The below price after Jul. 95 shall be applied to the wafers from the new or additional Facility.)

		Jul. 94 - Sep. 94	Oct. 94 - Dec. 94	Jan. 95 - Mar. 95	Apr. 95 - Jun. 95	Jul. 95 - Dec. 95	Jan. 96 - Jun. 96	Jul. 96 - Dec. 96	Jan. 97 - Jun. 97	Jul. 97 - Dec. 97
Sakata	Average Price					[*]	[*]	[*]	[*]	[*]
	UM5 A/C	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
	UM6 C +1	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
	UM6 C +2	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
	UM6 F	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
	UM6 C Z	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
Fujimi	Average Price					[*]	[*]	[*]	[*]	[*]
	UM5 A/C	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
	UM6 C +1	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
	UM6 C +2	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
	UM6 F	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
	UM6 C Z	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]

\+ 1 with UM5 metal module
\+ 2 with "New" metal module

2. For Facility Wafers beyond the Supply Commitment (Existing and New or Additional Facility)

		Jul. 94 - Sep. 94	Oct. 94 - Dec. 94	Jan. 95 - Mar. 95	Apr. 95 - Jun. 95	Jul. 95 - Dec. 95	Jan. 96 - Jun. 96	Jul. 96 - Dec. 96	Jan. 97 - Jun. 97	Jul. 97 - Dec. 97
Sakata	Average Price					[*]	[*]	[*]	[*]	[*]
	UM5 A/C	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
	UM6 C +1	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
	UM6 C +2	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
	UM6 F	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
	UM6 C Z	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
Fujimi	Average Price					[*]	[*]	[*]	[*]	[*]
	UM5 A/C	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
	UM6 C +1	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
	UM6 C +2	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
	UM6 F	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]
	UM6 C Z	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]

\+ 1 with UM5 metal module
\+ 2 with "New" metal module

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

3. For Facility Wafers covered by the Supply Commitment
(The below price shall be only used if New Facility construction is delayed.)

		Jul. 94 - Sep. 94	Oct. 94 - Dec. 94	Jan. 95 - Mar. 95	Apr. 95 - Jun. 95	Jul. 95 - Dec. 95	Jan. 96 - Jun. 96	Jul. 96 - Dec. 96	Jan. 97 - Jun. 97	Jul. 97 - Dec. 97
Fujimi	UM5 A/C	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]	[*]

+ The time scale of the tables in this Exhibit G is based on order placement date.
+ The prices of the above tables are the resale prices from S MOS.
+ All prices in the above table are production prices and those are applied for all sub-micron wafers Epson will supply to Lattice through S MOS. Engineering wafer prices are [*] times of production prices and they are applied to the engineering wafers quantities greater than [*] per year.
+ All prices in "Jan. 97-Jun. 97" and "Jul. 97-Dec. 97" are TBD and will be agreed by Dec. 1995.
+ Epson shall make efforts to guarantee the same yield of the Facility Wafers beyond the Supply Commitment as those covered by Supply Commitment in the equal process. Target defect densities are equal or below [*] and mutual activity plans for the defect densities improvement shall be agreed later between Lattice and Epson.

ENGINEERING PAYMENT AGREEMENT

DATED JULY 5, 1994

AMONG

LATTICE SEMICONDUCTOR CORPORATION

AND

SEIKO EPSON CORPORATION

AND

S MOS SYSTEMS INC.

ENGINEERING PAYMENT AGREEMENT

This Engineering Payment Agreement ("EP Agreement"), is entered into this 5th day of July, 1994, by and among Seiko Epson Corporation, a Japanese corporation, having a place of business at 3-5, Owa 3-chome, Suwa-shi, Nagano-ken 392, Japan ("Epson"), S MOS Systems Inc., a California corporation, having a place of business at 2460 North First Street, San Jose, California 95131-1002, U.S.A. ("S MOS") and Lattice Semiconductor Corporation, a Delaware corporation, having a place of business at 5555 Northeast Moore Ct., Hillsboro, Oregon 97124-6421, U.S.A. ("Lattice").

1. BACKGROUND

1.1 EPSON. Epson is in the business of designing, manufacturing, testing and selling semiconductor devices among other products. Epson manufactures such semiconductor devices at the Fujimi and the Sakata Plant.

1.2 S MOS. S MOS is an affiliate of Epson and is Epson's authorized distributor in the United States for semiconductor devices. S MOS is in the business of designing, testing and selling semiconductor devices. S MOS conducts its business at its office located at 2460 North First Street, San Jose, California 95131-1002, U.S.A.

1.3 LATTICE. Lattice is in the business of designing, developing, manufacturing, marketing and selling both high- and low-density E(2)CMOS - -Registered Trademark- programmable logic devices ("PLDs").

1.4 SCOPE OF AGREEMENT AND RELATIONSHIP TO OTHER AGREEMENTS. Epson, S MOS and Lattice have an ongoing business relationship whereby Epson fabricates semiconductor devices for Lattice. The parties desire to expand this relationship. Accordingly, the parties have executed that certain Advance Production Payment Agreement ("APP Agreement") dated as of July 5, 1994 pursuant to which (a) Epson will construct a 0.8-0.5 micron, 2-3 metal layer, 6 inch wafer CMOS process line in order to fabricate the Facility Wafers for Lattice and (b) Lattice will pay to Epson the APP to be used as a credit to purchase Facility Wafers from Epson over a specified period of time. Further, pursuant to this EP Agreement, Lattice will pay as a portion of certain engineering payment ("EP") incurred by Epson in connection with the fabrication of engineering samples of the Facility Wafers. In consideration of receipt of such payment, Epson will fabricate Engineering Wafer for Lattice free of charge and provide them through S MOS in the manner specified by this EP Agreement.

1.5 POSITION OF S MOS. Notwithstanding any provision herein to the contrary, Lattice, Epson and S MOS acknowledge that although EP Agreement is executed by each of such three (3) parties, S MOS

is a party hereto solely for the purpose to evidence its role, as the intermediary through which, under the terms of Purchase Agreement, the Products to be sold to Lattice by Epson will be sold, and to evidence S MOS's agreement to such an arrangement. S MOS shall under no circumstances have any rights under the APP and the EP Agreement, however shall maintain full rights as provided in the Purchase Agreement. In particular, and without limiting the generality of the foregoing, S MOS shall have no rights under Article 15 of APP Agreement (i.e., any reference to party or parties to EP Agreement shall be deemed to be only to Epson and Lattice unless specifically prescribed therein), and Epson and Lattice may amend the EP Agreement in any respect. Epson agrees to cause S MOS to comply with all of the terms of the Purchase Agreement. Any material breach of the Purchase Agreement shall constitute a material breach to the EP Agreement for the purposes of Article 15.4 of the APP Agreement.

2. ENGINEERING EXPENSES

2.1 AMOUNT, METHOD OF PAYMENT AND PURPOSE. Lattice will pay Epson Two Million U.S. Dollars (US$2,000,000) to cover the EP incurred in fabrication of the Products for Lattice. The EP will cover certain expenses, in excess of the construction of the Facility and the acquisition of the Equipment. The EP shall be remitted to Epson together with the payment of the first APP installment as prescribed in Article 4.3 of the APP Agreement. The EP will not be included in the APP or used as a credit for purchase of the Products.

2.2 SUPPLY OF ENGINEERING WAFERS. As a consideration for Lattice's payment of the EP, Epson shall provide Lattice through S MOS, free of charge, with a maximum of 500 Engineering Wafers, to be used for Research and Development purposes by Lattice, ordered for up to 10 types of the Products per period, each of which are established as below; provided that any Engineering Wafers not supplied during any period will not be carried over into the next period and that Epson's obligation herein shall be completed by providing 500 Engineering Wafers in a period even if those 500 wafers do not contain 10 types of the Products (i.e. the total number of provided Engineering Wafers takes precedence over the type of the Products). The Engineering Wafer herein shall be manufactured in the Facility.

1st period from 7/12/94 to 7/11/95
2nd period from 7/12/95 to 7/11/96
3rd period from 7/12/96 to 7/11/97
4th period from 7/12/97 to 7/11/98

3. PAYMENT METHOD

All payments made by Lattice to Epson will be in immediately available funds and will be made by wire transfer in U.S. Dollars to the same bank account designated in Article 4.4 of the APP Agreement.

4. FABRICATION, PURCHASE AND SALE

The terms and conditions for the Engineering Wafer fabrication, order and acceptance, shipping, insurance and warranty for the Products will be set forth in the Purchase Agreements. On behalf of Epson, S MOS shall sign all Purchase Agreements required to implement the terms and conditions of this Agreement. Epson agrees to cause S MOS to provide all Engineering Wafers covered by this Agreement in the manner required by the Purchase Agreements.

5. SHIPPING, INSURANCE, TAXES, DUTIES AND OTHER FEES

Epson will deliver the Products to S MOS on a C.I.F., San Jose basis, and S MOS will deliver such Products to Lattice on a F.O.B., San Jose basis. Bearing of sales, use, excise, ad valorem, withholding or other taxes or duties that may be applicable to purchase of the Products by Lattice shall be prescribed in the Purchase Agreement.

6. INTELLECTUAL PROPERTY RIGHTS

All intellectual property rights relating to the Engineering Wafers will be as set forth in, or as established pursuant to, the APP Agreements.

7. CONFIDENTIAL INFORMATION

The confidentiality obligations and restrictions set forth in the APP Agreement will apply to all Confidential Information disclosed under this EP Agreement.

8. TERM AND TERMINATION OF AGREEMENT

8.1 TERM. This Agreement shall be effective for a period of 4 years from the EP Installment Date unless terminated earlier pursuant to Articles 15.2, 15.3 or 15.4 of the APP Agreement or pursuant to Article 8.3 of the EP Agreement.

8.2 TERMINATION. The terms and conditions of Articles 15.2, 15.3, 15.4, 15.5 and 15.6 of the APP Agreement are incorporated into this EP Agreement concurrent with such termination.

8.3 EXPIRATION. This Agreement will automatically expire when Epson has provided all the required Engineering Wafers through S MOS to Lattice in the manner required by Article 2.2. No notice or other action will be required for the automatic expiration described above.

8.4 SURVIVAL OF OBLIGATIONS. The following Articles will survive any expiration, termination or cancellation of this Agreement and the parties will continue to be bound by the terms and conditions thereof: 6, 7 and 9.

9. MISCELLANEOUS

The terms and conditions of Article 16 of the APP Agreement are incorporated into this EP Agreement and the parties will be bound by all such terms and conditions. All references to the defined terms herein such as, but not limited to, "APP," "Facility Wafer," "Engineering Wafer" or "Product" shall be construed in compliance with the respective definition in the APP Agreement.

IN WITNESS WHEREOF, the parties have signed this EP Agreement as of the date first above written.

SEIKO EPSON CORPORATION	LATTICE SEMICONDUCTOR CORPORATION
By: /s/ Saburo Kusama	By: /s/ Cyrus Tsui
Name: Saburo Kusama	Name: Cyrus Tsui
Title: Managing Director, Co-Chief Operating Officer and General manager of Semi-conductor Operations Division	Title: President and CEO

S MOS SYSTEMS, INC.

By: /s/ Dan Hauer

Name: Dan Hauer

Title: President

EXHIBIT 11.1

LATTICE SEMICONDUCTOR CORPORATION

COMPUTATION OF NET INCOME PER SHARE
(In thousands, except per share data)

	Year Ended		
	April 1, 1995	April 2, 1994	April 3, 1993
Net income	$26,966	$22,490	$17,399
Weighted average common stock and common stock equivalents:			
Common	18,627	18,182	17,427
Options and warrants	537	764	1,031
	19,164	18,946	18,458
Net income per share	$ 1.41	$ 1.19	$ .94

MANAGEMENT'S DISCUSSION AND ANALYSIS OF FINANCIAL CONDITION AND RESULTS OF OPERATIONS

Lattice Semiconductor Corporation, founded in 1983, designs, develops and markets high and low density, high-speed E2CMOS[REGISTERED TRADEMARK] programmable logic devices (PLDs). PLDs shorten design cycles and reduce development cost by allowing the customer to quickly and efficiently incorporate different logic functions on a single device. Lattice products are sold worldwide through an extensive network of independent sales representatives and distributors, primarily to OEM customers in the fields of microcomputers, computer peripherals, graphic systems, workstations, telecommunications, military systems and industrial controls.

RESULTS OF OPERATIONS

The following table sets forth, for the periods indicated, the percentage of revenue represented by selected items reflected in the Company's statement of operations.

	YEAR ENDED		
	APRIL 1, 1995	APRIL 2, 1994	APRIL 3, 1993
Revenue	100%	100%	100%
Costs and expenses:			
Costs of products sold	41	42	42
Research and development	16	16	16
Selling, general and administrative	17	18	20
	74	76	78
Income from operations	26	24	22
Interest and other income (net)	2	2	2
Income before provision for income taxes	28	26	24
Provision for income taxes	9	8	7
Net income	19%	18%	17%

REVENUE Revenue was $144.1 million in fiscal 1995, an increase of 14% over fiscal 1994. The fiscal 1994 revenue of $126.2 million represented an increase of 22% from the $103.4 million recorded in fiscal 1993. Substantially all of the Company's revenue is derived from sales of PLDs (programmable logic devices). Most of the Company's revenue for the years presented was derived from sales of GAL[REGISTERED TRADEMARK] products, which address the low density segment of the CMOS programmable logic market. These devices have been the source of most of the Company's revenue to date. The Company entered the high density segment of the PLD market in fiscal 1993 with its pLSI[REGISTERED TRADEMARK] and ispLSI [REGISTERED TRADEMARK] product families. The increases in revenue since fiscal 1993 resulted primarily from the increased sales of new products, especially high density products. Revenue from international sales was approximately 47%, 43% and 45% of total revenue for fiscal 1995, 1994 and 1993, respectively. The Company expects export sales to continue to represent a significant portion of revenue.

Overall average selling prices remained relatively stable for the three fiscal years presented. Although selling prices of mature products generally decline over time, this decline is at times offset by higher selling prices of new products. The Company's ability to maintain its recent trend of revenue growth and market penetration is in large part dependent on the continued development, introduction and market acceptance of new products.

GROSS MARGIN The Company's gross margin as a percentage of revenue was 59% in fiscal 1995 and 58% in fiscal 1994 and fiscal 1993. The increase in gross margin over fiscal 1994 was primarily due to improved capacity utilization and reductions in the Company's manufacturing costs. Profit margins on older products tend to decrease over time as selling prices decline, but the Company's strategy has been to offset these decreases by continuously introducing new products with higher margins.

The Company's wafer purchases are denominated in Japanese yen. Therefore, gross margins are adversely affected by increases in yen valuation compared to the dollar. The Company managed to offset most of the adverse currency movement through fiscal 1995 with manufacturing efficiencies. From March 1995 to date, the value of the yen with respect to the dollar has strengthened significantly. In absence of a recovery by the dollar, it is likely that future gross margins will be adversely affected.

The Company's gross margin percentage in future periods will be negatively affected if the Company fails to execute its new product strategy, if the profit contribution from new products is not sufficient to offset the anticipated margin decline from older products, or if the Company is unable to offset adverse yen to dollar exchange rate changes. The increase in gross margin since fiscal 1994 is not necessarily indicative of future margin trends.

RESEARCH AND DEVELOPMENT Research and development expense was $22.9 million, $20.6 million and $16.5 million in fiscal 1995, 1994 and 1993, respectively. For the last three years, the Company has maintained its investment in research and development at a relatively constant 16% of revenue. The spending increases were

related primarily to the development of new technologies and new products, including the Company's high density product families and their related software development tools. The Company believes that a continued commitment to research and development is essential in order to maintain product leadership in its existing product families and to provide innovation in new product offerings, and therefore expects to continue to make significant investments in research and development in the future.

SELLING, GENERAL AND ADMINISTRATIVE Selling, general and administrative expense increased to $25.0 million in fiscal 1995 from $22.3 million in fiscal 1994, which was an increase from $20.5 million in fiscal 1993. The increase each year was primarily due to expansion of the Company's sales force, the addition of field applications engineers to provide enhanced customer assistance, and higher sales commissions associated with the higher revenue levels. Selling, general and administrative expense as a percentage of revenue decreased slightly in fiscal 1995 to 17% from 18% in fiscal 1994, and from 20% in fiscal 1993.

INCOME FROM OPERATIONS Income from operations increased 24%, from $30.0 million to $37.3 million, from fiscal 1994 to fiscal 1995, and increased 32%, from $22.7 million, between fiscal 1993 and fiscal 1994. Income from operations increased as a percentage of revenue, from 22% in fiscal 1993 to 24% in fiscal 1994, and then to 26% in fiscal 1995.

INTEREST AND OTHER INCOME Interest and other income (net of expense) remained relatively constant as a percentage of revenue over the three years. During fiscal 1993 and 1994, this was due to larger invested cash balances offsetting lowering interest rates. Interest rates began rising in fiscal 1995, offsetting the decrease in cash balances beginning in the second fiscal quarter due to the advance payments made to Seiko (see "Significant Transactions" below).

PROVISION FOR INCOME TAXES The Company's effective tax rate was 33.5% for fiscal 1995 as compared to 31% recorded in each of the two preceding fiscal years. This increase occurred primarily because both net operating loss and tax credit carryforwards were available in fiscal 1994, while only the remaining tax credit carryforwards were available in fiscal 1995.

The Company expects its effective tax rate in future years to be slightly higher than the current rate due to the full utilization during fiscal 1995 of the remaining tax credit carryforwards.

Deferred tax asset valuation allowances are recorded to offset deferred tax assets that can only be realized by earning taxable income in distant future years. Management established the valuation allowances because it cannot determine if it is more likely than not that such income will be earned.

In February 1992, the Financial Accounting Standards Board issued Statement of Financial Accounting Standards (SFAS) No. 109, "Accounting for Income Taxes," which the Company adopted in fiscal 1994. The adoption of SFAS No. 109 did not have a material impact on the Company's consolidated financial statements.

NET INCOME Net income increased 20%, from $22.5 million to $27.0 million, from fiscal 1994 to fiscal 1995, and increased 29%, from $17.4 million, between fiscal 1993 and fiscal 1994. Net income increased as a percentage of revenue each fiscal year, from 17% in fiscal 1993 to 18% in fiscal 1994, and then to 19% in fiscal 1995.

In May 1993, the Company's Board of Directors approved a three-for-two split of the Company's common stock which was effected in the form of a stock dividend paid on July 6, 1993 to stockholders of record as of June 14, 1993.

FACTORS AFFECTING FUTURE RESULTS In the future, the Company's operating results may fluctuate as a result of a number of factors, including but not limited to cancellations or delays of orders, interruption or delays in the supply of raw materials, increases in the cost of raw materials, interruption or delays in work performed by third-party contractors, changes in customer base or product mix, delays in purchase decisions due to new product announcements by the Company or its competitors, increased competition, reductions in average selling prices, the Company's ability to obtain and defend competitive patents and other intellectual property, and weak economic conditions, political instability or other natural disasters in foreign markets in which the Company distributes or manufactures its products.

Due to the complexity of the manufacturing process and the extremely low defect tolerances associated with the manufacture of complex integrated circuits, the Company considers the relationship with its wafer supplier to be critical to its success. State-of-the-art semiconductor manufacturing processes are sensitive to a wide variety of factors, including the level of contaminants in the manufacturing environment, impurities in the raw materials and the performance of the personnel and equipment employed. Through fiscal 1995, the Company has been successful in obtaining adequate wafer capacity commitments and has not experienced any material difficulties or delays in the supply of wafers. Presently, demand on wafer suppliers is growing and existing capacity commitments may not be sufficient to satisfy the Company's continued growth. Moreover, all of the Company's wafer requirements are currently supplied by Seiko Epson Corporation. Although the Company has existing wafer supply commitments from such supplier which it believes will be adequate through the second quarter of fiscal 1996, such supplier has recently indicated that it does not presently intend to supply wafers at increased levels. In the event the Company is unable to obtain additional wafers from an alternate supplier and Seiko continues to be unable to increase wafer supplies to the Company, the Company's ability to increase sales of its products would be adversely affected. In addition, there can be no assurance such supplier will not reduce its allocation of wafers to the Company in future periods or that any such reduction could be offset from alternative sources of supply. If such supplier were to reduce its wafer allocations to the Company and the Company were unable to replace such capacity through alternative sources of supply, sales of the Company's products would be materially adversely affected. The Company also expects that, as is customary in the semiconductor business, it will in the future seek to convert its fabrication process arrangements to larger wafer sizes, to more advanced process technologies, or to new or additional suppliers in order to maintain or enhance its competitive position. Such conversions entail inherent technological risks that could adversely affect yields and delivery times, and have material adverse impact on the Company's operating results.

The Company's continued success will depend in large part on its ability to introduce new products on a timely basis that achieve market acceptance, are competitively priced and produce acceptable profit margins, and also on various factors outside of the Company's control, such as the health and cyclical nature of the semiconductor industry and the worldwide economy. Due to its rapidly changing technology and competitive nature, the semiconductor industry from time to time experiences depressed economic conditions. In addition, the inherent volatility of the industry has produced and may continue to produce fluctuations in the price of the stock of companies participating in this industry, including

the Company's common stock.

The growth in the Company's revenue and gross margin percentage over the past three fiscal years was due primarily to sales of GAL[REGISTERED TRADEMARK] products, many of which are second sourced from other suppliers. Continued revenue growth will be largely dependent on market acceptance of the Company's new and proprietary products, including the high density product families, and the availability of competitive software development tools.

SIGNIFICANT TRANSACTIONS

In July 1994, the Company entered into an advance production payment agreement with Seiko Epson Corporation ("Seiko") and S-MOS Systems, Inc. ("S-MOS"), a U.S. affiliate of Seiko, under which it advanced to Seiko $42 million during fiscal 1995 to be used by Seiko to finance additional sub-micron semiconductor wafer manufacturing capacity. Under the terms of the agreement, the advances are to be repaid in the form of advanced technology sub-micron semiconductor wafers. Subject to certain conditions set forth in the agreement, Seiko has agreed to supply, and the Company has agreed to receive, such wafers at a price (in Japanese yen) and volume expected to achieve full repayment of the advance over a three to four year period. In connection with the advance production payment agreement, the Company also paid $2 million during fiscal 1995 for the development of sub-micron process technology and the fabrication of engineering wafers to be delivered over the same period.

Funds advanced to Seiko under the agreement terms are accounted for as a Wafer Supply Advance and are included in current and noncurrent assets based upon management's estimate of when the advance will be realized in wafer receipts. Wafers received under the agreement terms are recorded as inventory at agreed upon prices (in Japanese yen) at which time the advance is reduced by a corresponding amount. When products made from the wafers are sold, product costs are charged to operations. The agreement does not call for interest payments or cash repayment of advances. No interest income is recorded. The benefit of funds advanced to Seiko is returned to the Company through pricing and wafer supply commitments. Agreement related transactions in comparison to other wafer purchases are not expected to have a significant effect on future gross margins. The absence of cash payments for wafers received under agreement terms will favorably affect future cash flows.

The advanced production payment agreement calls for the wafers to be supplied by Seiko through S-MOS, as U.S. distributor for Seiko, pursuant to a purchase agreement concluded with S-MOS.

All of the Company's wafer requirements are currently supplied by Seiko. Daniel S. Hauer, a member of the Company's Board of Directors, is Chairman of the Board of S-MOS.

LIQUIDITY AND CAPITAL RESOURCES

The Company's financial condition strengthened during fiscal 1995. Cash and short-term investments decreased by $4.8 million, from $93.6 million at April 2, 1994 to $88.8 million at April 1, 1995. This balance decreased primarily because the cash generated from operations was offset by the advance payments made to Seiko (see "Significant Transactions" above).

Accounts receivable and deferred income on sales to distributors increased 56% and 66%, respectively, as compared to the balances at April 2, 1994. These increases are primarily due to the increase in revenue of 34% for the fiscal 1995 fourth quarter over the fiscal 1994 fourth quarter. Accounts payable and accrued expenses increased 104% as compared to the balance at April 2, 1994 due to increased expense activity related to the higher revenue levels as well as timing of payments.

The increase in income taxes payable of 27% between April 1, 1995 and April 2, 1994 is primarily attributable to increased profitability in fiscal 1995 as compared to fiscal 1994 and the timing of quarterly tax payments.

Substantially all of the Company's silicon wafer purchases are denominated in Japanese yen. The Company maintains yen-denominated bank accounts and bills its Japanese customers in yen. The yen bank deposits utilized to hedge yen-denominated wafer purchases are accounted for as identifiable hedges against specific and firm wafer purchases.

As of April 1, 1995, the Company's principal source of liquidity was $88.8 million of cash and short-term investments. The Company also has available an unsecured $10 million demand bank credit facility with interest due on outstanding balances at a money market rate. This facility has not been used.

Capital expenditures were approximately $6.3 million, $7.2 million and $11.7 million for fiscal years 1995, 1994 and 1993, respectively. These expenditures consisted primarily of manufacturing test equipment, lab equipment, engineering workstations, buildings and building improvements.

The Company currently anticipates capital expenditures of approximately $14 million to $18 million for the fiscal year ending March 30, 1996. A significant portion of these expenditures is planned for improvements and expansions to the Company's manufacturing capacity and facilities.

The Company believes its existing sources of liquidity and funds expected to be generated from operations will provide adequate cash to fund the Company's anticipated cash operating needs for at least the next 12 months.

SELECTED FINANCIAL DATA

(IN THOUSANDS, EXCEPT PER SHARE DATA)	YEAR ENDED APRIL 1, 1995	APRIL 2, 1994	APRIL 3, 1993	MARCH 28, 1992	MARCH 30, 1991
STATEMENT OF OPERATIONS DATA:					
Revenue	$144,083	$126,241	$103,391	$71,009	$64,539
Costs and expenses:					
Cost of products sold	58,936	53,266	43,650	31,015	29,919
Research and development	22,859	20,636	16,530	12,535	10,363
Selling, general and administrative	25,020	22,299	20,465	14,144	12,142
	106,815	96,201	80,645	57,694	52,424
Income from operations	37,268	30,040	22,746	13,315	12,115
Interest and other income, net	3,349	2,566	2,470	2,420	2,439
Income before provision for income taxes	40,617	32,606	25,216	15,735	14,554
Provision for income taxes	13,651	10,116	7,817	4,880	4,257
Net income	$ 26,966	$ 22,490	$ 17,399	$10,855	$10,297
Net income per share	$ 1.41	$ 1.19	$ 0.94	$ 0.61	$ 0.61
Weighted average common and common equivalent shares outstanding	19,164	18,946	18,458	17,834	16,770
BALANCE SHEET DATA:					
Working capital	$106,021	$105,007	$ 79,878	$64,297	$51,770
Total assets	192,917	146,093	128,876	91,653	79,081
Long-term lease obligations, excluding current portion	--	--	--	205	566
Stockholders' equity	157,797	125,068	98,481	75,643	63,230

	YEAR ENDED APRIL 1, 1995				YEAR ENDED APRIL 2, 1994			
	FOURTH QUARTER	THIRD QUARTER	SECOND QUARTER	FIRST QUARTER	FOURTH QUARTER	THIRD QUARTER	SECOND QUARTER	FIRST QUARTER
UNAUDITED QUARTERLY DATA:								
Revenue	$40,318	$36,288	$34,564	$32,913	$30,187	$28,573	$34,136	$33,345
Gross profit	$23,608	$21,478	$20,566	$19,495	$17,741	$16,503	$19,627	$19,104
Net income	$ 7,698	$ 6,850	$ 6,419	$ 5,999	$ 5,640	$ 5,083	$ 6,097	$ 5,670
Net income per share	$ 0.40	$ 0.36	$ 0.34	$ 0.32	$ 0.30	$ 0.27	$ 0.32	$ 0.30

ALL SHARE AND PER SHARE AMOUNTS HAVE BEEN ADJUSTED TO REFLECT THE THREE-FOR-TWO STOCK SPLIT EFFECTED IN THE FORM OF A STOCK DIVIDEND WHICH WAS PAID ON JULY 6, 1993.

CONSOLIDATED BALANCE SHEET

(IN THOUSANDS, EXCEPT SHARE AMOUNTS)	APRIL 1, 1995	APRIL 2, 1994
ASSETS		
Current assets:		
Cash and cash equivalents	$ 7,697	$ 18,363
Short-term investments	81,113	75,239
Accounts receivable, net	18,147	11,661
Inventories (note 2)	14,131	13,847
Prepaid expenses and other current assets (note 8)	12,751	1,401
Deferred income taxes (note 6)	7,302	5,521
Total current assets	141,141	126,032
Deposits and other assets	341	238
Wafer supply advance (note 8)	31,320	-
Property and equipment, less accumulated depreciation (note 3)	20,115	19,823
	$192,917	$146,093
LIABILITIES AND STOCKHOLDERS' EQUITY		
Current liabilities:		
Accounts payable and accrued expenses (note 8)	$ 12,774	$ 6,258
Accrued payroll obligations	5,389	3,590
Income taxes payable (note 6)	5,206	4,091
Deferred income	11,751	7,086
Total current liabilities	35,120	21,025
Commitments and contingencies (notes 4, 5, 8, 9 and 10)	-	-
Stockholders' equity (note 7):		
Preferred stock, $.01 par value, 10,000,000 shares authorized; none issued and outstanding	-	-
Common stock, $.01 par value, 100,000,000 shares authorized; 18,889,703 and 18,411,035 shares issued and outstanding	189	184
Paid-in capital	82,802	77,044
Retained earnings	74,806	47,840
	157,797	125,068
	$192,917	$146,093

THE ACCOMPANYING NOTES ARE AN INTEGRAL PART OF THIS STATEMENT.

CONSOLIDATED STATEMENT OF OPERATIONS

(IN THOUSANDS, EXCEPT PER SHARE DATA)	YEAR ENDED APRIL 1, 1995	APRIL 2, 1994	APRIL 3, 1993
Revenue	$ 144,083	$ 126,241	$ 103,391
Cost and expenses:			
Cost of products sold (note 8)	58,936	53,266	43,650
Research and development	22,859	20,636	16,530
Selling, general and administrative	25,020	22,299	20,465
	106,815	96,201	80,645
Income from operations	37,268	30,040	22,746
Other income (expense):			
Interest income	3,437	2,794	2,378
Other income (expense), net	(88)	(228)	92
Income before provision for income taxes	40,617	32,606	25,216
Provision for income taxes (note 6)	13,651	10,116	7,817
Net income	$ 26,966	$ 22,490	$ 17,399
Net income per share	$ 1.41	$ 1.19	$ .94
Weighted average number of common and common equivalent shares outstanding	19,164	18,946	18,458

THE ACCOMPANYING NOTES ARE AN INTEGRAL PART OF THIS STATEMENT.

CONSOLIDATED STATEMENT OF CHANGES IN STOCKHOLDERS' EQUITY

(IN THOUSANDS)	COMMON STOCK ($.01 PAR VALUE) SHARES	AMOUNT	PAID-IN CAPITAL	RETAINED EARNINGS	TOTAL
Balances, March 28, 1992	17,028	$ 170	$ 67,522	$ 7,951	$ 75,643
Common stock issued	897	9	1,941	-	1,950
Tax benefit of option exercises	-	-	3,449	-	3,449
Other	-	-	40	-	40
Net income for fiscal 1993	-	-	-	17,399	17,399
Balances, April 3, 1993	17,925	179	72,952	25,350	98,481
Common stock issued	486	5	2,061	-	2,066
Tax benefit of option exercises	-	-	2,172	-	2,172
Other	-	-	(141)	-	(141)
Net income for fiscal 1994	-	-	-	22,490	22,490
Balances, April 2, 1994	18,411	184	77,044	47,840	125,068
Common stock issued	479	5	3,659	-	3,664
Tax benefit of option exercises	-	-	2,133	-	2,133
Other	-	-	(34)	-	(34)
Net income for fiscal 1995	-	-	-	26,966	26,966
Balances, April 1, 1995	18,890	$ 189	$ 82,802	$ 74,806	$ 157,797

THE ACCOMPANYING NOTES ARE AN INTEGRAL PART OF THIS STATEMENT.

CONSOLIDATED STATEMENT OF CASH FLOWS

(IN THOUSANDS)	YEAR ENDED APRIL 1, 1995	APRIL 2, 1994	APRIL 3, 1993
CASH FLOW FROM OPERATING ACTIVITIES:			
Net income	$ 26,966	$ 22,490	$ 17,399
Adjustments to reconcile net income to net cash provided by operating activities:			
Depreciation and amortization	6,007	5,788	4,713
Deferred income taxes	(1,781)	(3,325)	(1,001)
Changes in assets and liabilities:			
Accounts receivable	(6,486)	965	(3,908)
Inventories	(284)	(338)	(7,459)
Prepaid expenses and other current assets	(100)	(367)	(226)
Deposits and other assets	(103)	(61)	(120)
Wafer supply advance, net of wafer receipts	(42,570)	-	-
Accounts payable and accrued expenses	6,516	(10,870)	7,101
Accrued payroll obligations	1,799	424	869
Income taxes payable	1,115	1,150	2,634
Deferred income	4,665	70	4,151
Net cash provided (used) by operating activities	(4,256)	15,926	24,153
CASH FLOW FROM INVESTING ACTIVITIES:			
Purchase of short-term investments, net	(5,874)	(5,086)	(13,697)
Proceeds from sale of fixed assets	-	-	40
Capital expenditures	(6,299)	(7,185)	(11,687)
Net cash used by investing activities	(12,173)	(12,271)	(25,344)
CASH FLOW FROM FINANCING ACTIVITIES:			
Net proceeds from issuance of common stock	5,763	4,097	5,439
Payments of capital lease obligations	-	(144)	(368)
Net cash provided by financing activities	5,763	3,953	5,071
Net increase (decrease) in cash and cash equivalents	(10,666)	7,608	3,880
Beginning cash and cash equivalents	18,363	10,755	6,875
Ending cash and cash equivalents	$ 7,697	$ 18,363	$ 10,755

THE ACCOMPANYING NOTES ARE AN INTEGRAL PART OF THIS STATEMENT.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS

NOTE 1. DESCRIPTION OF BUSINESS AND SIGNIFICANT ACCOUNTING POLICIES

DESCRIPTION OF BUSINESS Lattice Semiconductor Corporation (the Company), founded in 1983, designs, develops, and markets high- and low-density, high-speed E2CMOS[REGISTERED TRADEMARK] PLDs.

FISCAL REPORTING PERIOD AND PRINCIPLES OF CONSOLIDATION The Company reports on a 52 or 53 week fiscal year, which ends on the Saturday closest to March 31. The accompanying consolidated financial statements include the accounts of Lattice Semiconductor Corporation and its wholly owned foreign subsidiaries, Lattice Gmbh, Lattice Semiconducteurs SARL, Lattice Semiconductor KK, Lattice Semiconductor Shanghai Co. Ltd., Lattice Semiconductor Asia Ltd., Lattice Semiconductor International Ltd. and Lattice Semiconductor UK Ltd. The assets, liabilities, and results of operations of these entities were not significant for any of the years presented in the consolidated financial statements and all intercompany accounts and transactions have been eliminated.

CASH EQUIVALENTS AND SHORT-TERM INVESTMENTS The Company considers all highly liquid investments, which are readily convertible into cash and have original maturities of three months or less, to be cash equivalents. Short-term investments, which have maturities greater than three months and less than one year, are composed of money market preferred stocks ($49.2 million), government obligations ($26.6 million) and time deposits ($5.3 million).

Prior to fiscal 1995, the Company reported investments at cost which approximated market. Effective beginning in the first quarter of fiscal 1995, the Company adopted Statement of Financial Accounting Standards No. 115, "Accounting for Certain Investments in Debt and Equity Securities" (SFAS No. 115), which creates certain classification categories for such investments based on the nature of the securities and intent of the Company. SFAS No. 115 has been adopted on a prospective basis, and the cumulative effect of the change was not material. Pursuant to adoption, the Company has categorized its investments as held-to-maturity. Securities classified as held-to-maturity are stated at amortized cost with corresponding premiums or discounts amortized over the life of the investment to interest income. Realized gains or losses are reflected in other income. Such gains or losses were not significant for the fiscal years presented.

FINANCIAL INSTRUMENTS All of the Company's significant financial assets and liabilities are recognized in the Consolidated Balance Sheet as of April 1, 1995. The value reflected in the Consolidated Balance Sheet (carrying value) approximates fair value for the Company's financial assets and liabilities. The Company estimates the fair value of its cash and cash equivalents, short-term investments, accounts receivable, other current assets and current liabilities based upon existing interest rates related to such assets and liabilities compared to the current market rates of interest for instruments of similar nature and degree of risk.

CONCENTRATIONS OF CREDIT RISK Financial instruments which potentially expose the Company to concentrations of credit risk consist primarily of short-term investments and trade receivables. The Company places its investments through several financial institutions and mitigates the concentration of credit risk by placing percentage limits on the maximum portion of the investment portfolio which may be invested in any one investment instrument. Investments consist primarily of A1 and P1 or better rated U.S. commercial paper, U.S. government agency obligations and other money market instruments, and "AA" or better rated municipal obligations and money market preferred stocks. Concentrations of credit risk with respect to trade receivables are mitigated by a geographically diverse customer base and the Company's credit and collection process. The Company performs credit evaluations for all customers and secures transactions with letters of credit or advance payments where necessary. Write-offs for uncollected trade receivables have not been significant to date.

REVENUE RECOGNITION AND ACCOUNTS RECEIVABLE Revenue from sales to OEM (original equipment manufacturer) customers is recognized upon shipment. Certain of the Company's sales are made to distributors under agreements providing price protection and right of return on unsold merchandise. Revenue and cost relating to distributor sales are deferred until the product is sold by the distributor and related revenue and costs are then reflected in income. Accounts receivable are shown net of allowance for doubtful accounts of $743,000 and $697,000 at April 1, 1995 and April 2, 1994, respectively.

Revenue from two distributors was $17.3 million and $16.1 million for fiscal 1995, $14.7 million and $12.6 million for fiscal 1994 and $11.7 million and $11.6 million for fiscal 1993. Export revenue was approximately $68.4 million, $54.6 million and $46.8 million for fiscal 1995, 1994 and 1993, respectively. Sales to Europe were approximately $24.5 million, $16.1 million and $13.1 million, and to Asia $40.6 million, $34.3 million and $32.7 million in fiscal 1995, 1994 and 1993, respectively.

INVENTORIES Inventories are stated at the lower of first-in, first-out cost or market.

PROPERTY AND EQUIPMENT Property and equipment are recorded at cost. Depreciation is computed using the straight-line method for financial reporting purposes over the estimated useful lives of the related assets, generally three to five years for equipment and thirty years for buildings. Accelerated methods of computing depreciation are generally used for income tax purposes.

TRANSLATION OF FOREIGN CURRENCIES The Company translates accounts denominated in foreign currencies in accordance with Statement of Financial Accounting Standards (SFAS) No. 52, "Foreign Currency Translation." Translation adjustments related to the consolidation of foreign subsidiary financial statements have not been significant to date.

RESEARCH AND DEVELOPMENT Research and development costs are expensed as incurred.

INCOME TAXES Income taxes are calculated in accordance with SFAS No. 109, "Accounting for Income Taxes," which the Company adopted on a prospective basis in the first quarter of fiscal 1994. The Company had previously adopted SFAS No. 96 during fiscal 1988. Both statements utilize the asset and liability method for computing deferred income taxes. Accordingly, adoption of SFAS No. 109 had no material effect on the Company's provision for income taxes or results of operations.

NET INCOME PER SHARE Net income per share is computed based on the weighted average number of shares of common stock and common stock equivalents assumed to be outstanding during the period (using the treasury stock method). Common stock equivalents consist of stock options and warrants to purchase common stock. All share and per share amounts presented in the accompanying consolidated financial statements and notes thereto have been adjusted to reflect the three-for-two stock split effected in the form of a stock dividend which was paid on July 6, 1993.

FOREIGN EXCHANGE Substantially all of the Company's silicon wafer purchases are denominated in Japanese yen. The Company maintains yen-denominated bank accounts and bills its Japanese customers in yen. The yen bank deposits utilized to hedge yen-denominated wafer purchases are accounted for as identifiable hedges against specific and firm wafer purchases. Gains or losses from foreign exchange rate fluctuations on unhedged balances denominated in foreign currencies are reflected in other income.

STATEMENT OF CASH FLOWS Income taxes paid approximated $11.9 million, $10.1 million and $3.0 million in fiscal 1995, 1994 and 1993, respectively. Interest paid does not differ materially from interest expense, which aggregated approximately $28,000, $23,000 and $39,000 in fiscal 1995, 1994 and 1993, respectively.

NOTE 2. INVENTORIES

(IN THOUSANDS)	APRIL 1, 1995	APRIL 2, 1994
Work in progress	$ 9,686	$ 9,984
Finished goods	4,445	3,863
	$ 14,131	$ 13,847

NOTE 3. PROPERTY AND EQUIPMENT

(IN THOUSANDS)	APRIL 1, 1995	APRIL 2, 1994
Land	$ 1,455	$ 1,455
Buildings	5,473	5,142
Computer and test equipment	33,372	28,626
Office furniture and equipment	2,518	2,380
Leasehold and building improvements	2,223	1,894
	45,041	39,497
Accumulated depreciation and amortization	(24,926)	(19,674)
	$ 20,115	$ 19,823

NOTE 4. CREDIT FACILITIES

The Company has available an unsecured $10 million demand bank credit facility with interest due on outstanding balances at a money market rate. This facility has not been used.

NOTE 5. LEASE OBLIGATIONS

Certain facilities and equipment of the Company are leased under operating leases, which expire at various times through fiscal 1999. Rental expense under the operating leases was approximately $815,000, $672,000 and $505,000 for fiscal 1995, 1994 and 1993, respectively.

Future minimum lease commitments at April 1, 1995 are as follows:

FISCAL YEAR (IN THOUSANDS)	
1996	$ 361
1997	381
1998	391
1999	165
	$1,298

NOTE 6. INCOME TAXES

As described in Note 1, the Company adopted SFAS No. 109, "Accounting for Income Taxes" on a prospective basis in fiscal 1994. The adoption of SFAS No. 109 did not have a material impact on the Company's provision for income taxes or results of operations. SFAS No. 109 is an asset and liability approach that

requires the recognition of deferred tax assets and liabilities for the expected future tax consequences of temporary differences between the carrying amounts of assets and liabilities for financial reporting purposes and the amounts used for income tax purposes. In estimating future tax consequences, SFAS No. 109 generally considers all expected future events other than enactments of changes in the tax laws or rates. Previously, the Company operated under the provisions of SFAS No. 96, which also used an asset and liability approach but gave no recognition of future events other than the recovery of assets and settlement of liabilities at their carrying amounts.

The components of the provision for income taxes for fiscal 1995, 1994 and 1993 are presented in the following table:

	YEAR ENDED		
(IN THOUSANDS)	APRIL 1, 1995	APRIL 2, 1994	APRIL 3, 1993
Current:			
Federal	$ 13,849	$ 11,761	$ 7,890
State	1,583	1,680	928
	15,432	13,441	8,818
Deferred:			
Federal	(1,598)	(2,909)	(896)
State	(183)	(416)	(105)
	(1,781)	(3,325)	(1,001)
	$ 13,651	$ 10,116	$ 7,817

The provision for income taxes differs from the amount of income tax determined by applying the U.S. statutory federal income tax rate to pretax income as a result of the following differences:

	YEAR ENDED		
(IN THOUSANDS)	APRIL 1, 1995	APRIL 2, 1994	APRIL 3, 1993
Computed income tax expense at the statutory rate	$ 14,216	$ 11,412	$ 8,573
Adjustments for tax effects of:			
State taxes, net	1,625	1,630	1,009
Research and development credits, current	(193)	(272)	(454)
Research and development and investment tax credit carryforwards	(243)	(601)	-
Benefit of operating loss carryforward	-	(658)	(1,336)
Nontaxable investment income	(1,020)	(824)	(756)
Other	(734)	(571)	781
	$13,651	$ 10,116	$ 7,817

The components of the Company's net deferred tax asset under SFAS No. 109 were as follows:

(IN THOUSANDS)	APRIL 1, 1995	APRIL 2, 1994
Deferred income	$ 4,172	$ 2,120
Expenses and allowances not currently deductible	5,949	4,959
Research and development credit	-	520
Other, net	-	342
Total deferred tax assets	10,121	7,941
Valuation allowance	(2,819)	(2,420)
	$ 7,302	$ 5,521

The valuation allowances are recorded to offset deferred tax assets which can only be realized by earning taxable income in distant future years. Management established the valuation allowances because it cannot determine if it is more likely than not that such income will be earned.

NOTE 7. STOCKHOLDERS' EQUITY

STOCK WARRANTS During fiscal 1995, 1994, 1993, and 1991 the Company issued to a vendor warrants to purchase 62,125 shares at $17.38 per share, 106,500 shares at $20.17 per share, 106,500 shares at $10.17 per share, and 84,000 shares at $6.17 per share, respectively. In fiscal 1993, the vendor exercised warrants for 189,000 shares; total shares issued to the vendor were 94,782 after surrender of 94,218 shares to cover exercise costs of approximately $1.1 million. During fiscal 1994, the vendor exercised warrants for 106,500 shares; total shares issued to the vendor were 50,904 after surrender of 55,596 shares to cover exercise costs of approximately $1.1 million. The remaining outstanding warrants at April 1, 1995 expire on July 1, 1998.

STOCK OPTION PLAN As of April 1, 1995, the Company had reserved 5,775,000 shares of common stock for issuance to officers and key employees under a stock option plan. The options, which are generally granted at no less than fair market value at the date of grant, are exercisable immediately and expire five years from date of grant. The transfer of certain shares of common stock acquired through exercise of employee stock options is restricted under stock vesting agreements that grant the Company the right to repurchase unvested shares at the exercise price if employment is terminated. Generally, the Company's repurchase rights lapse quarterly over four years.

The following table summarizes activity under the plan during the past three years:

	SHARES UNDER OPTION	PRICE RANGE
Balance, March 28, 1992	2,323,477	$ .07 - $ 9.83
Options granted	820,230	$10.17 - $17.83
Options canceled	(163,626)	$ .27 - $14.50
Options exercised	(716,557)	$ .07 - $ 9.83
Balance, April 3, 1993	2,263,524	$ .07 - $17.83
Options granted	491,180	$14.88 - $23.75
Options canceled	(203,266)	$ .07 - $23.75
Options exercised	(371,835)	$ .07 - $14.50
Balance, April 2, 1994	2,179,603	$ .27 - $23.75
Options granted	548,400	$16.38 - $23.50
Options canceled	(113,790)	$ .27 - $23.75
Options exercised	(393,726)	$ .27 - $18.88
Balance April 1, 1995	2,220,487	$ 3.67 - $23.50
Available for grant at April 1, 1995	1,111,202	

OUTSIDE DIRECTORS STOCK OPTION PLAN The 1993 Outside Directors Stock Option Plan was approved by the stockholders in August 1993, replacing the 1990 Amended Outside Directors Stock Option Plan. The new plan provides for the issuance of stock options to members of the Company's Board of Directors who are not employees of the Company; 225,000 shares of the Company's Common Stock are reserved for issuance thereunder. In August 1993, each non-employee director was granted under the new plan an option to purchase 18,000 shares of common stock. These options generally become exercisable quarterly over a four-year period beginning on the date of grant. As of April 1, 1995 and April 2, 1994, options to purchase 128,625 shares of common stock had been granted to non-employee directors under the former plan. The last grants under the former plan were made in August 1993, and no additional grants under the former plan are anticipated.

The following table summarizes activity under these plans during the past three years:

	SHARES UNDER OPTION	PRICE RANGE
Balance, March 28, 1992	50,250	$ 0.27 - $ 9.83
Options granted	20,250	$10.17 - $17.83
Options exercised	(16,500)	$ 0.27 - $ 9.50
Balance, April 3, 1993	54,000	$ 0.27 - $17.83
Options granted	100,875	$20.17 - $23.75
Options exercised	(12,375)	$ 0.27 - $ 9.50
Balance, April 2, 1994	142,500	$ 3.75 - $23.75
Options canceled	(13,500)	$23.75
Options exercised	(9,000)	$ 3.75 - $20.17
Balance April 1, 1995	120,000	$ 9.50 - $23.75
Available for grant at April 1, 1995	148,500	

STOCK PURCHASE PLAN The Company's employee stock purchase plan was approved by the stockholders in August 1990, and became effective January 1, 1991. The plan permits eligible employees to purchase shares of common stock through payroll deductions, not to exceed 10% of the employee's compensation. The purchase price of the shares is the lower of 85% of the fair market value of the stock at the beginning of each six-month offering period or 85% of the fair market value at the end of such period, but in no event less than the book value per share at the mid-point of each offering period. Amounts accumulated through payroll deductions during the offering period are used to purchase shares on the last day of the offering period. Of the 450,000 shares authorized to be issued under the plan, 70,973, 45,789 and 62,190 shares were issued during fiscal 1995, 1994 and 1993, respectively, and 169,498 shares were available for issuance at April 1, 1995.

SHAREHOLDER RIGHTS PLAN A shareholder rights plan approved on September 11, 1991 provides for the issuance of one right for each share of outstanding common stock. With certain exceptions, the rights will become exercisable only in the event that an acquiring party accumulates beneficial ownership of 20% or more of the Company's outstanding common stock or announces a tender or exchange offer, the consummation of which would result in ownership by that party of 20% or more of the Company's outstanding common stock.

The rights expire on September 11, 2001 if not previously redeemed or exercised. Each right entitles the holder to purchase, for $60.00, a fraction of a share of the Company's Series A Participating Preferred Stock with economic terms similar to that of one share of the Company's common stock. The Company will generally be entitled to redeem the rights at $0.01 per right at any time on or prior to the tenth day after an acquiring person has acquired beneficial ownership of 20% or more of the Company's common stock. If, prior to the redemption or expiration of the rights, an acquiring person or group acquires beneficial ownership of 20% or more of the Company's outstanding common stock, each right not beneficially owned by the acquiring person or group will entitle its holder to purchase, at the rights' then current exercise price, that number of shares of common stock having a value equal to two times the exercise price.

NOTE 8. TRANSACTIONS WITH PRINCIPAL SUPPLIER

The Chairman of the Board of the Company's wafer supplier is a member of the Company's Board of Directors. In July 1994, the Company signed an agreement with this wafer supplier under which it advanced $44 million to the supplier during fiscal 1995 to be used in conjunction with the construction of additional wafer fabrication capacity and technological development. The advance will be repaid in the form of semiconductor wafers over a multi-year period. No interest income is recorded. Total wafer receipts under this agreement aggregated approximately $1,430,000 during fiscal 1995. The balance sheet caption "Prepaid expenses and other current assets" includes management's estimate of such wafers to be received under the agreement during fiscal 1996, aggregating $11,250,000.

The Company continues to purchase a portion of its wafer supply from this supplier for cash using commercial terms. Wafer purchases totalled $27.8 million, $25.4 million and $22.7 million for fiscal 1995, 1994 and 1993, respectively. Accounts payable and accrued expenses at April 1, 1995 included $4.1 million due this vendor; such balances were insignificant at April 2, 1994. Open purchase commitments to this supplier approximated $9.6 million at April 1, 1995.

NOTE 9. EMPLOYEE BENEFIT PLANS

PROFIT SHARING PLAN The Company initiated a profit sharing plan effective April 1, 1990. Under the provisions of this plan, as approved by the Board of Directors, a percentage of the operating income of the Company, as defined and calculated at the end of the second and fourth quarter of each fiscal year for each respective six-month period, is to be paid equally to qualified employees. In fiscal 1995, 1994 and 1993, approximately $1.4 million, $1.2 million and $983,000, respectively, were charged against operations in connection with the plan.

QUALIFIED INVESTMENT PLAN In 1990, the Company adopted a 401(k) plan, which provides participants with an opportunity to accumulate funds for retirement. Under the terms of the plan, eligible participants may contribute up to 15% of their eligible earnings to the plan Trust. The plan allows for discretionary matching contributions by the Company; no such contributions have occurred to date.

NOTE 10. COMMITMENTS AND CONTINGENCIES

The Company is exposed to certain asserted and unasserted potential claims. Patent and other proprietary rights infringement claims are common in the semiconductor industry and the Company has received a letter from a semiconductor manufacturer stating that it believes certain patents held by it cover products previously sold by the Company. While this manufacturer has offered to license certain of such patents to the Company, there can be no assurance that, on this or any other claim which may be made against the Company, the Company could obtain a license on terms or under conditions that would not have a material adverse effect to the Company. Management believes that the disposition of these claims will not have a material adverse effect on the Company's financial position or results of operations.

NOTE 11. RELATED PARTY

Larry W. Sonsini is a member of the Company's Board of Directors and is presently the Chairman of the Executive Committee of Wilson, Sonsini, Goodrich & Rosati, a law firm that provides corporate legal services to the Company. Legal services billed to the Company aggregated approximately $46,000, $129,000 and $68,000, respectively, for fiscal 1995, 1994 and 1993. Amounts payable to the law firm were not significant at April 1, 1995 or April 2, 1994.

REPORT OF INDEPENDENT ACCOUNTANTS
To the Board of Directors and Stockholders of
Lattice Semiconductor Corporation

In our opinion, the accompanying consolidated balance sheet and the related consolidated statements of operations, of changes in stockholders' equity and of cash flows present fairly, in all material respects, the financial position of Lattice Semiconductor Corporation and its subsidiaries at April 1, 1995 and April 2, 1994, and the results of their operations and their cash flows for each of the three years in the period ended April 1, 1995, in conformity with generally accepted accounting principles. These financial statements are the responsibility of the Company's management; our responsibility is to express an opinion on these financial statements based on our audits. We conducted our audits of these statements in accordance with generally accepted auditing standards which require that we plan and perform the audit to obtain reasonable assurance about whether the financial statements are free of material misstatement. An audit includes examining, on a test basis, evidence supporting the amounts and disclosures in the financial statements, assessing the accounting principles used and significant estimates made by management, and evaluating the overall financial statement presentation. We believe that our audits provide a reasonable basis for the opinion expressed above.

As discussed in Note 6 to the consolidated financial statements, the

Company changed its method of accounting for income taxes in fiscal year 1994.

/s/PRICE WATERHOUSE LLP
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Portland, Oregon
April 20, 1995

CORPORATE DIRECTORY

BOARD OF DIRECTORS

Cyrus Y. Tsui
Chairman of the Board, President and
Chief Executive Officer

Daniel S. Hauer
Chairman of the Board,
S-MOS Systems Inc.

Harry A. Merlo(1)
President and Chairman,
Louisiana-Pacific Corp.

Douglas C. Strain(2)
Vice Chairman,
Electro Scientific Industries, Inc.

Larry W. Sonsini(2)
Partner and Chairman of the
Executive Committee,
Wilson, Sonsini, Goodrich & Rosati

OFFICERS

Cyrus Y. Tsui
Chairman of the Board,
President and Chief Executive Officer

Albert L. Chan
Vice President,
California Product Development

Stephen M. Donovan
Vice President, International Sales

Paul T. Kollar
Vice President, Sales

Steven A. Laub
Vice President and General Manager

Rodney F. Sloss
Vice President, Finance and Secretary

Jerry G. Taylor
Vice President, Oregon Product
Development

Jonathan K. Yu
Vice President, Operations

Kenneth K. Yu
Vice President and Managing Director,
Lattice Asia
Technology Advisor to the
Office of the President

(1)MEMBER OF THE AUDIT COMMITTEE
(2)MEMBER OF THE COMPENSATION COMMITTEE

LEGAL COUNSEL

Wilson, Sonsini, Goodrich & Rosati
650 Page Mill Road
Palo Alto, California 94304-1050
415/493-9300

INDEPENDENT ACCOUNTANTS

Price Waterhouse LLP
121 S.W. Morrison Street, Suite 1800
Portland, Oregon 97204
503/224-9040

CORPORATE OFFICES

Lattice Semiconductor Corporation
5555 N.E. Moore Court
Hillsboro, Oregon 97124-6421
Telephone: 503/681-0118
Facsimile: 503/681-0347

REGISTRAR AND TRANSFER AGENT

First Interstate Bank
Stock Transfer Administration
P.O. Box 21927
Seattle, Washington 98111
206/292-3696

ANNUAL MEETING

The annual meeting of stockholders for Lattice Semiconductor Corporation will be held at the Embassy Suites Hotel, 9000 S.W. Washington Square Road, Tigard, OR 97223, on Monday, August 14, 1995, at 1:00 pm.

FORM 10-K
A copy of the Company's Annual Report on Form 10-K, as filed with the Securities and Exchange Commission, will be made available without charge to all stockholders upon written request to the Company.

COMMON STOCK
Lattice Semiconductor Corporation's common stock is traded on the NASDAQ National Market System under the symbol "LSCC."

STOCK PRICE HISTORY
The Company's common stock is traded on the over-the-counter market and prices are quoted on the NASDAQ National Market System under the symbol "LSCC." The following table sets forth the high and low sale prices for the last two fiscal years.

	HIGH	LOW
Fiscal 1994:		
First Quarter	20 13/16	14 11/16
Second Quarter	26 3/4	14 3/4
Third Quarter	24 3/4	12 1/4
Fourth Quarter	19 3/8	14
Fiscal 1995:		
First Quarter	19 5/8	14 3/4
Second Quarter	20 1/8	17
Third Quarter	19 3/8	15 1/2
Fourth Quarter	27 1/8	16 3/8

In May 1993 the Company's Board of Directors approved a three-for-two split of its common stock which was effected in the form of a stock dividend. The stock dividend was paid on July 6, 1993 to stockholders of record as of June 14, 1993. The above sale prices have been adjusted to reflect the stock split.

EXHIBIT 21.1

LATTICE SEMICONDUCTOR CORPORATION

SUBSIDIARIES OF THE REGISTRANT

	Name	Jurisdiction of Incorporation
1.	Lattice GmbH	Germany
2.	Lattice Semiconducteurs SARL	France
3.	Lattice Semiconductor KK	Japan
4.	Lattice Semiconductor (Shanghai) Co. Ltd.	China
5.	Lattice UK Limited	United Kingdom
6.	Lattice Semiconductor International Limited	Jamaica
7.	Lattice Semiconductor Asia Limited	Hong Kong

Exhibit 23.1

CONSENT OF INDEPENDENT ACCOUNTANTS

We hereby consent to the incorporation by reference in the Prospectus constituting part of this Registration Statement on Form S-8 (No. 33-33833, No. 33-35259, No. 33-38521, No. 33-78368 and No. 33-69495) of Lattice Semiconductor Corporation of our report dated April 20, 1995 appearing on page 24 of the Annual Report to Stockholders which is incorporated in this Annual Report on Form 10-K. We also consent to the incorporation by reference of our report on the Financial Statement Schedules which appears on page S-1 of this Form 10-K.

PRICE WATERHOUSE LLP

Portland, Oregon
June 26, 1995

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APR-01-1995
APR-03-1994
APR-01-1995
7,697
81,113
18,147
743
14,131
141,141
45,041
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0
0
(3,349)
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13,651
26,966
0
0
0
26,966
1.41
1.41