Registration No. 333-41146
Filed Pursuant to Rule 424(b)(4)

4,000,000 Shares

[LOGO]

Common Stock

The common stock is quoted on the Nasdaq National Market under the symbol "LSCC". The last reported sale price of the common stock on July 31, 2000 was $54.875 per share.

SEE "RISK FACTORS" BEGINNING ON PAGE 7 TO READ ABOUT FACTORS YOU SHOULD CONSIDER BEFORE BUYING SHARES OF OUR COMMON STOCK.

NEITHER THE SECURITIES AND EXCHANGE COMMISSION NOR ANY STATE SECURITIES COMMISSION HAS APPROVED OR DISAPPROVED OF THESE SECURITIES OR PASSED UPON THE ACCURACY OR ADEQUACY OF THIS PROSPECTUS. ANY REPRESENTATION TO THE CONTRARY IS A CRIMINAL OFFENSE.

	Per Share	Total
Initial price to public	$54.875	$219,500,000
Underwriting discount	$ 2.470	$ 9,880,000
Proceeds, before expenses, to Lattice	$52.405	$209,620,000

If the underwriters sell more than 4,000,000 shares of common stock, the underwriters have the option to purchase up to an additional 600,000 shares from Lattice at the public offering price less the underwriting discount.

The underwriters expect to deliver the shares against payment in New York, New York on August 4, 2000.

JOINT BOOKRUNNING MANAGERS

GOLDMAN, SACHS & CO. MORGAN STANLEY DEAN WITTER

PRUDENTIAL VOLPE TECHNOLOGY
a unit of Prudential Securities

Prospectus dated July 31, 2000.

PROSPECTUS SUMMARY

THIS SUMMARY HIGHLIGHTS INFORMATION WE PRESENT MORE FULLY ELSEWHERE IN THIS PROSPECTUS AND IN THE DOCUMENTS INCORPORATED BY REFERENCE INTO THIS PROSPECTUS. THIS SUMMARY DOES NOT CONTAIN ALL OF THE INFORMATION THAT YOU SHOULD CONSIDER BEFORE BUYING SHARES IN THE OFFERING. YOU SHOULD READ CAREFULLY THE ENTIRE PROSPECTUS AND ALL OF THE DOCUMENTS INCORPORATED BY REFERENCE INTO THIS PROSPECTUS.

LATTICE SEMICONDUCTOR CORPORATION

We design, develop and market high performance programmable logic devices and related software. We are the world's leading supplier of in-system programmable logic devices. Programmable logic devices are widely-used semiconductor components that can be configured by the end customer as specific logic circuits, and enable the end customer to shorten design cycle times and reduce development costs. Our end customers are primarily original equipment manufacturers, in the markets of data communications and telecommunications, as well as computing, industrial and military systems. During the June 2000 quarter, we derived approximately 66% of our $139.9 million in revenue from the communications markets and approximately 20% from the computing market.

Manufacturers of electronic systems are increasingly challenged to bring differentiated products to market quickly. These competitive pressures often preclude the use of custom-designed application specific integrated circuits which generally entail significant design risks and time delay. Standard logic products, an alternative to custom-designed application specific integrated circuits, limit a manufacturer's flexibility to customize an end system. Programmable logic devices give system designers the ability to quickly create their own custom logic circuits, provide product differentiation and rapidly bring products to market.

According to Dataquest, the programmable logic device market in 1999 was approximately $2.6 billion. The programmable logic device market has two primary segments: high-density programmable logic devices, with more than 1,000 logic gates, and low-density programmable logic devices, with fewer than 1,000 logic gates. High-density programmable logic devices include devices based on both the complex programmable logic device and the field programmable gate array architectures. Dataquest estimated that in 1999 the complex programmable logic device market was $0.8 billion and the field programmable gate array market was $1.6 billion.

We offer a full product line in both the high-density complex programmable logic device market and the low-density programmable logic device market. Our strategy has been to continue to increase our market share in the rapidly growing complex programmable logic device market with differentiated proprietary products, software and technology and at present we hold the number two position in this market. Since we introduced our first complex programmable logic device products in 1992, we have continued to focus on increasing the percentage of our total revenue generated by complex programmable logic device products. During the June 2000 quarter, complex programmable logic device revenue accounted for approximately 75% of our total revenue.

Our complex programmable logic device products provide our customers with industry-leading performance, density and number of input/output pins. In addition, we currently offer 29 complex programmable logic device products that operate using a 3.3-volt or 2.5-volt power supply instead of the older 5-volt standard, the largest portfolio of low-voltage complex programmable logic device products in the marketplace. Lower voltage programmable logic devices benefit end users by consuming less power and providing compatibility with other advanced electronic components. We believe that our innovative low-voltage complex programmable logic device products provide us a competitive advantage as our customers transition the power supply of their systems from 5 volts to 3.3 volts.

We pioneered the development of in-system programmability, which has become an industry standard feature in the programmable logic device market. In contrast to standard programmable logic

device programming technologies, in-system programmability allows the system designer to configure and reconfigure a programmable logic device without removing the device from the system board. By enhancing the flexibility of programmable logic devices, in-system programmability provides a number of important benefits to a system manufacturer over the lifecycle of an electronic system product. In-system programmability can allow customers to reduce design cycle times, accelerate time to market, reduce prototyping costs, reduce manufacturing costs, lower inventory requirements and perform simplified and cost-effective field upgrades.

In June 1999, we acquired Vantis Corporation, the programmable logic device subsidiary of Advanced Micro Devices. This acquisition has increased our share of the programmable logic device market, accelerated development of new products and technologies and expanded our penetration into new and existing customers.

Our manufacturing strategy has been to procure silicon wafers for our products from leading manufacturers under current purchase orders and long-term agreements. This has allowed us to avoid the cost of establishing our own wafer fabrication facility.

We sell our products directly to end customers through a network of independent sales representatives and indirectly through a network of distributors. We use a direct sales management and field applications engineering organization together with manufacturers' representatives and distributors to reach a broad base of potential end customers. We believe our distribution channels provide a cost-effective means for reaching end customers.

We were incorporated in Oregon in 1983 and reincorporated in Delaware in 1985. Our principal offices are located at 5555 N.E. Moore Court, Hillsboro, Oregon 97124, our telephone number is (503) 268-8000 and our website can be accessed at www.latticesemi.com. Information contained in our website is not intended to constitute part of this prospectus.

THE OFFERING

Shares offered	4,000,000 shares
Shares to be outstanding after this offering	53,446,405 shares
Nasdaq National Market symbol	LSCC
Use of proceeds	General corporate purposes, including working capital, and potentially for investments to maintain and expand our wafer supply capacity and for acquisition opportunities that may arise in the future

The number of shares to be outstanding after this offering includes:

- 49,446,405 shares of common stock outstanding at June 30, 2000; and

- 4,000,000 shares of common stock offered in this offering.

The number of shares to be outstanding after this offering excludes:

- 7,517,248 shares of common stock issuable upon exercise of stock options outstanding at June 30, 2000, with a weighted average exercise price of $23.83 per share;

- 3,061,191 shares of common stock available for grant at June 30, 2000 under our 1996 stock option plan;

- 126,000 shares of common stock available for grant at June 30, 2000 under our 1993 directors' stock option plan;

- 319,096 shares of common stock available for issuance at June 30, 2000 under our employee stock purchase plan;

- 313,396 shares of common stock issuable upon exercise of warrants outstanding at June 30, 2000, at a weighted average exercise price of $24.10 per share; and

- 6,274,131 shares of common stock issuable upon conversion of our 4 3/4% convertible subordinated notes.

Except as otherwise indicated, information in this prospectus assumes no exercise of the underwriters' option to purchase additional shares in the offering.

SUMMARY CONSOLIDATED FINANCIAL DATA
(IN THOUSANDS, EXCEPT PER SHARE DATA)

	YEAR ENDED MARCH 31,		NINE MONTH FISCAL PERIOD ENDED DEC. 31,	SIX MONTHS ENDED JUNE 30,		
	1998	1999	1999(1)	1999	PRO FORMA 1999(2)	2000
					(UNAUDITED)	
CONSOLIDATED STATEMENT OF OPERATIONS DATA:						
Revenue	$245,894	$200,072	$269,699	$113,526	$205,378	$265,933
Gross profit	147,011	121,632	161,012	69,902	119,980	162,710
Income (loss) from operations	75,065	51,624	(70,350)	(62,352)	(1,623)	44,541
Net income (loss)	56,567	42,046	(48,146)(3)	(39,315)	(6,419)	121,563(4)
Basic net income (loss) per share	$ 1.22	$ .90	$ (1.01)	$ (.83)	$ (.14)	$ 2.48
Diluted net income (loss) per share	$ 1.18	$ .88	$ (1.01)	$ (.83)	$ (.14)	$ 2.16
Shares used in per share calculations:						
Basic	46,478	46,974	47,714	47,189	47,189	48,987
Diluted	47,788	47,638	47,714	47,189	47,189	58,568

	JUNE 30, 2000	
	ACTUAL	AS ADJUSTED(5)
	(UNAUDITED)	
CONSOLIDATED BALANCE SHEET DATA:		
Cash, cash equivalents and short-term investments	$ 253,581	$ 463,201
Working capital	254,744	464,364
Total assets	1,096,364	1,305,984
Long-term debt	260,000	260,000
Stockholders' equity	634,239	843,859

- ------------------------------

(1) In 1999, we changed our fiscal year end from March 31 to December 31. This period includes financial results for our acquisition of Vantis since June 15, 1999. The pro forma results of operations for the period ended December 31, 1999 have been reflected in the Form 8-K filed July 11, 2000, which is incorporated by reference in this prospectus.

(2) Reflects our acquisition of Vantis Corporation. The pro forma unaudited consolidated statement of operations data for the six months ended June 30, 1999 are presented using our unaudited condensed consolidated statement of operations for the six months ended June 30, 1999 combined with Vantis' unaudited condensed consolidated statement of operations for the six months ended July 3, 1999 assuming the transaction occurred on the first day of that period.

(3) Includes the effects of an $89.0 million charge for in-process research and development and the related income tax effects incurred and recorded in conjunction with our acquisition of Vantis on June 15, 1999, and an extraordinary loss of $1.7 million, net of income taxes, for unamortized debt issuance costs related to bank debt retired with the proceeds from our issuance of 4 3/4% convertible subordinated notes during the period. See Notes 4 and 8 to the consolidated financial statements for the period ended December 31, 1999 incorporated by reference in this prospectus.

(4) Includes the effects of a $150 million gain ($92.1 million after-tax) representing the appreciation of investments made in two Taiwanese semiconductor foundry companies. See Note 10 to the unaudited consolidated financial statements for the period ended June 30, 2000 incorporated by reference in this prospectus.

(5) The as adjusted column gives effect to the sale of 4,000,000 shares of common stock at an offering price to the public of $54.875 per share and after deducting the underwriting discount and assuming that the underwriters' option to purchase additional shares in the offering is not exercised.

RISK FACTORS

YOU SHOULD CAREFULLY CONSIDER THE RISKS DESCRIBED BELOW BEFORE MAKING AN INVESTMENT DECISION. IF ANY OF THE FOLLOWING RISKS ACTUALLY OCCURS, OUR BUSINESS, FINANCIAL CONDITION AND RESULTS OF OPERATIONS COULD BE HARMED. THIS COULD CAUSE THE TRADING PRICE OF OUR COMMON STOCK TO DECLINE, AND YOU MAY LOSE ALL OR PART OF YOUR INVESTMENT.

RISKS RELATED TO OUR BUSINESS

OUR WAFER SUPPLY MAY BE INTERRUPTED OR REDUCED, WHICH MAY RESULT IN A SHORTAGE OF FINISHED PRODUCTS AVAILABLE FOR SALE.

We do not manufacture finished silicon wafers. Currently, all of our silicon wafers are manufactured by Seiko Epson in Japan, AMD in the United States and UMC in Taiwan. If Seiko Epson, through its U.S. affiliate Epson Electronics America, AMD or UMC significantly interrupts or reduces our wafer supply, our operating results could be harmed.

In the past, we have experienced delays in obtaining wafers and in securing supply commitments from our foundries. At present, we anticipate that our supply commitments are adequate. However, these existing supply commitments may not be sufficient for us to satisfy customer demand in future periods. Additionally, notwithstanding our supply commitments we may still have difficulty in obtaining wafer deliveries consistent with the supply commitments. We negotiate wafer prices and supply commitments from our suppliers on at least an annual basis. If any of Seiko Epson, Epson Electronics America, AMD or UMC were to reduce its supply commitment or increase its wafer prices, and we cannot find alternative sources of wafer supply, our operating results could be harmed.

Many other factors that could disrupt our wafer supply are beyond our control. Since worldwide manufacturing capacity for silicon wafers is limited and inelastic, we could be harmed by significant industry-wide increases in overall wafer demand or interruptions in wafer supply. Additionally, a future disruption of Seiko Epson's, AMD's or UMC's foundry operations as a result of a fire, earthquake or other natural disaster could disrupt our wafer supply and could harm our operating results.

IF OUR FOUNDRY PARTNERS EXPERIENCE QUALITY OR YIELD PROBLEMS, WE MAY FACE A SHORTAGE OF FINISHED PRODUCTS AVAILABLE FOR SALE.

We depend on our foundries to deliver reliable silicon wafers with acceptable yields in a timely manner. As is common in our industry, we have experienced wafer yield problems and delivery delays. If our foundries are unable to produce silicon wafers that meet our specifications, with acceptable yields, for a prolonged period, our operating results could be harmed.

Substantially all of our revenue is derived from products based on a specialized silicon wafer manufacturing process technology called E(2)CMOS-Registered Trademark-. The reliable manufacture of high performance E(2)CMOS semiconductor wafers is a complicated and technically demanding process requiring:

- a high degree of technical skill;
- state-of-the-art equipment;
- the absence of defects in the masks used to print circuits on a wafer;
- the elimination of minute impurities and errors in each step of the fabrication process; and
- effective cooperation between the wafer supplier and the circuit designer.

As a result, our foundries may experience difficulties in achieving acceptable quality and yield levels when manufacturing our silicon wafers.

WE MAY BE UNSUCCESSFUL IN DEFINING, DEVELOPING OR SELLING NEW PRODUCTS REQUIRED TO MAINTAIN OR EXPAND OUR BUSINESS.

As a semiconductor company, we operate in a dynamic environment marked by rapid product obsolescence. Our future success depends on our ability to introduce new or improved products that meet customer needs while achieving acceptable margins. If we fail to introduce these new products in a timely manner or these products fail to achieve market acceptance, our operating results would be harmed.

The introduction of new products in a dynamic market environment presents significant business challenges. Product development commitments and expenditures must be made well in advance of product sales. The success of a new product depends on accurate forecasts of long-term market demand and future technology developments.

Our future revenue growth is dependent on market acceptance of our new product families and the continued market acceptance of our software development tools. The success of these products is dependent on a variety of specific technical factors including:

- successful product definition;

- timely and efficient completion of product design;

- timely and efficient implementation of wafer manufacturing and assembly processes;

- product performance; and

- the quality and reliability of the product.

If, due to these or other factors, our new products do not achieve market acceptance, our operating results would be harmed.

OUR PRODUCTS MAY NOT BE COMPETITIVE IF WE ARE UNSUCCESSFUL IN MIGRATING OUR MANUFACTURING PROCESSES TO MORE ADVANCED TECHNOLOGIES.

To develop new products and maintain the competitiveness of existing products, we need to migrate to more advanced wafer manufacturing processes that use larger wafer sizes and smaller device geometries. We also may need to use additional foundries. Because we depend upon foundries to provide their facilities and support for our process technology development, we may experience delays in the availability of advanced wafer manufacturing process technologies at existing or new wafer fabrication facilities. As a result, volume production of our advanced E(2)CMOS process technologies at the new fabs of Seiko Epson, UMC or future foundries may not be achieved. This could harm our operating results.

IF OUR ASSEMBLY AND TEST SUBCONTRACTORS EXPERIENCE QUALITY OR YIELD PROBLEMS, WE MAY FACE A SHORTAGE OF FINISHED PRODUCTS AVAILABLE FOR SALE.

We rely on subcontractors to assemble and test our devices with acceptable quality and yield levels. As is common in our industry, we have experienced quality and yield problems in the past. If we experience prolonged quality or yield problems in the future, our operating results could be harmed.

The majority of our revenue is derived from semiconductor devices assembled in advanced packages. The assembly of advanced packages is a complex process requiring:

- a high degree of technical skill;

- state-of-the-art equipment;

- the absence of defects in lead frames used to attach semiconductor devices to the package;

- the elimination of raw material impurities and errors in each step of the process; and

- effective cooperation between the assembly subcontractor and the device manufacturer.

As a result, our subcontractors may experience difficulties in achieving acceptable quality and yield levels when assembling and testing our semiconductor devices.

DETERIORATION OF CONDITIONS IN ASIA MAY DISRUPT OUR EXISTING SUPPLY ARRANGEMENTS AND RESULT IN A SHORTAGE OF FINISHED PRODUCTS AVAILABLE FOR SALE.

Two of our three silicon wafer suppliers operate fabs located in Asia. Our finished silicon wafers are assembled and tested by independent subcontractors located in Hong Kong, Malaysia, the Philippines, South Korea, Taiwan and Thailand. A prolonged interruption in our supply from any of these subcontractors could harm our operating results.

Economic, financial, social and political conditions in Asia have been volatile. Financial difficulties, governmental actions or restrictions, prolonged work stoppages or any other difficulties experienced by our suppliers may disrupt our supply and could harm our operating results.

Our wafer purchases from Seiko Epson are denominated in Japanese yen. The value of the dollar with respect to the yen fluctuates. Substantial deterioration of dollar-yen exchange rates could harm our operating results.

EXPORT SALES ACCOUNT FOR A SUBSTANTIAL PORTION OF OUR REVENUES AND MAY DECLINE IN THE FUTURE DUE TO ECONOMIC AND GOVERNMENTAL UNCERTAINTIES.

Our export sales are affected by unique risks frequently associated with foreign economies including:

- changes in local economic conditions;

- exchange rate volatility;

- governmental controls and trade restrictions;

- export license requirements and restrictions on the export of technology;

- political instability;

- changes in tax rates, tariffs or freight rates;

- interruptions in air transportation; and

- difficulties in staffing and managing foreign sales offices.

For example, our export sales have been affected by regional economic crises. Significant changes in the economic climate in the foreign countries where we derive our export sales could harm our operating results.

OUR FUTURE QUARTERLY OPERATING RESULTS MAY FLUCTUATE AND THEREFORE MAY FAIL TO MEET EXPECTATIONS.

Our quarterly operating results have fluctuated and may continue to fluctuate. Consequently, our operating results may fail to meet the expectations of analysts and investors. As a result of industry conditions and the following specific factors, our quarterly operating results are more likely to fluctuate and are more difficult to predict than a typical non-technology company of our size and maturity:

- general economic conditions in the countries where we sell our products;

- the timing of our and our competitors' new product introductions;

- product obsolescence;

- the scheduling, rescheduling and cancellation of large orders by our customers;

- the cyclical nature of demand for our customers' products;

- our ability to develop new process technologies and achieve volume production at the new fabs of Seiko Epson, UMC or at other foundries;

- changes in manufacturing yields;

- adverse movements in exchange rates, interest rates or tax rates; and

- the availability of adequate supply commitments from our wafer foundries and assembly and test subcontractors.

As a result of these factors, our past financial results are not necessarily a good predictor of our future results.

OUR STOCK PRICE MAY CONTINUE TO EXPERIENCE LARGE SHORT-TERM FLUCTUATIONS.

In recent years, the price of our common stock has fluctuated greatly. These price fluctuations have been rapid and severe and have left investors little time to react. The price of our common stock may continue to fluctuate greatly in the future due to a variety of company specific factors, including:

- quarter-to-quarter variations in our operating results;

- shortfalls in revenue or earnings from levels expected by securities analysts; and

- announcements of technological innovations or new products by other companies.

RISKS RELATED TO OUR INDUSTRY

THE CYCLICAL NATURE OF THE SEMICONDUCTOR INDUSTRY MAY LIMIT OUR ABILITY TO MAINTAIN OR INCREASE REVENUE AND PROFIT LEVELS DURING FUTURE INDUSTRY DOWNTURNS.

The semiconductor industry is cyclical. Our financial performance has been negatively affected by significant downturns in the semiconductor industry as a result of:

- the cyclical nature of the demand for the products of semiconductor customers;

- general reductions in inventory levels by customers;

- excess production capacity; and

- accelerated declines in average selling prices.

If these or other conditions in the semiconductor industry occur, our operating results could be harmed.

WE MAY NOT BE ABLE TO SUCCESSFULLY COMPETE IN THE HIGHLY COMPETITIVE SEMICONDUCTOR INDUSTRY.

The semiconductor industry is intensely competitive and many of our direct and indirect competitors have substantially greater financial, technological, manufacturing, marketing and sales resources. If we are unable to compete successfully in this environment, our operating results could be harmed.

The current level of competition in the programmable logic market is high and may increase as our market expands. We currently compete directly with companies that have licensed our products and technology or have developed similar products. We also compete indirectly with numerous semiconductor companies that offer products and solutions based on alternative technologies. These direct and indirect competitors are established multinational semiconductor companies as well as emerging companies. We also may experience significant competition from foreign companies in the future.

WE MAY FAIL TO RETAIN OR ATTRACT THE SPECIALIZED TECHNICAL AND MANAGEMENT PERSONNEL REQUIRED TO SUCCESSFULLY OPERATE OUR BUSINESS.

To a greater degree than most non-technology companies or larger technology companies, our future success depends on our ability to attract and retain highly qualified technical and management personnel. As a mid-sized company, we are particularly dependent on a relatively small group of key employees. Competition for skilled technical and management employees is intense within our industry. As a result, we may be unable to retain our existing key technical and management personnel or attract additional qualified employees. If we are unable to retain existing key employees or hire new qualified employees, our operating results could be harmed.

IF WE ARE UNABLE TO ADEQUATELY PROTECT OUR INTELLECTUAL PROPERTY RIGHTS, OUR FINANCIAL RESULTS AND COMPETITIVE POSITION MAY SUFFER.

Our success depends, in part, on our proprietary technology. However, we may fail to adequately protect this technology. As a result, we may lose our competitive position or face significant expense to protect or enforce our intellectual property rights.

We intend to continue to protect our proprietary technology through patents, copyrights and trade secrets. Despite this intention, we may not be successful in achieving adequate protection. Claims allowed on any of our patents may not be sufficiently broad to protect our technology. Patents issued to us also may be challenged, invalidated or circumvented. Finally, our competitors may develop similar technology independently.

Companies in the semiconductor industry vigorously pursue their intellectual property rights. If we become involved in protracted intellectual property disputes or litigation we may use substantial financial and management resources, which could harm our operating results.

We may also be subject to future intellectual property claims or judgements. If these were to occur, we may not be able to obtain a license on favorable terms or without our operating results being harmed.

YOU SHOULD NOT RELY ON FORWARD-LOOKING STATEMENTS BECAUSE THEY ARE INHERENTLY UNCERTAIN

This prospectus, including the documents that we incorporate by reference, contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934. Any statements about our expectations, beliefs, plans, objectives, assumptions or future events or performance are not historical facts and may be forward-looking. We use words or phrases such as "anticipate," "estimate," "plans," "project," "continuing," "ongoing," "expect," "management believes," "we believe," "we intend" and similar words or phrases to identify forward-looking statements.

Forward-looking statements involve estimates, assumptions and uncertainties that could cause actual results to differ materially from those expressed in them. Any forward-looking statements are qualified in their entirety by reference to the factors discussed throughout this prospectus. Among the key factors that could cause our actual results to differ materially from the forward-looking statements are:

- delay in product or technology development;
- change in economic conditions of the various markets we serve;
- lack of market acceptance or demand for our new products;
- dependencies on silicon wafer suppliers and semiconductor assemblers;
- the impact of competitive products and pricing;
- opportunities or acquisitions that we pursue; and
- the availability and terms of financing.

You should not unduly rely on forward-looking statements because our actual results could materially differ from those expressed in any forward-looking statements made by us. Further, any forward-looking statement applies only as of the date on which it is made. We are not required to update any forward-looking statement or statements to reflect events or circumstances after the date on which such statement is made or to reflect the occurrence of unanticipated events.

USE OF PROCEEDS

The net proceeds we will receive from our sale of the 4,000,000 shares of common stock in this offering are estimated to be $209.6 million, or $241.1 million if the underwriters exercise in full their option to purchase additional shares in the offering. These estimates are calculated based on a public offering price of $54.875 per share and after deducting the underwriting discount.

We intend to use the net proceeds for general corporate purposes, including working capital, and potentially for investments in order to maintain and expand our wafer supply capacity.

We may, when and if the opportunity arises, use a portion of the net proceeds to acquire complementary products, technologies or businesses. Until we use the net proceeds of this offering, we intend to invest the net proceeds in interest-bearing, investment-grade securities.

COMMON STOCK PRICE RANGE

Our common stock is quoted on the Nasdaq National Market under the symbol "LSCC". The following table sets forth the low and high last reported sale prices for our common stock for the last two fiscal years and for the period since January 1, 2000. On July 31, 2000, the last reported sale price of our common stock was $54.875. As of July 28, 2000, we had approximately 588 stockholders of record.

	LOW	HIGH
Fiscal year ended March 31, 1999		
First quarter	$13.438	$26.563
Second quarter	11.875	18.313
Third quarter	9.562	22.953
Fourth quarter	19.125	27.500
Fiscal period ended December 31, 1999		
First quarter	$19.812	$31.125
Second quarter	26.938	34.500
Third quarter	28.125	53.750
Fiscal year ending December 31, 2000		
First quarter	$41.625	$79.062
Second quarter	51.500	82.688
Third quarter (through July 31, 2000)	54.625	78.563

All share amounts have been adjusted retroactively to reflect the two-for-one stock split effected in the form of a stock dividend of one share of common stock for each share of our outstanding common stock that was paid on September 16, 1999.

DIVIDEND POLICY

The payment of dividends on our common stock is within the discretion of our board of directors. Currently, we intend to retain earnings to finance the growth of our business. We have not paid cash dividends on our common stock, and the board of directors does not expect to declare cash dividends on the common stock in the near future.

CAPITALIZATION

The following table sets forth our capitalization as of June 30, 2000 on an actual basis and as adjusted to give effect to the sale of the 4,000,000 shares of common stock, at an offering price to the public of $54.875 per share and after deducting the underwriting discount and assuming the underwriters' option to purchase additional shares in the offering is not exercised. This table should be read in conjunction with our consolidated financial statements, related notes and the other information included or incorporated by reference in this prospectus.

	JUNE 30, 2000	
	ACTUAL	AS ADJUSTED
	(IN THOUSANDS)	
Long-term obligations:		
Long-term debt	$260,000	$ 260,000
Other long-term liabilities	16,994	16,994
Total long-term obligations	276,994	276,994
Stockholders' equity:		
Preferred stock, $0.01 par value; 10,000,000 shares authorized; none issued or outstanding, actual and as adjusted	--	--
Common stock, $0.01 par value; 300,000,000 shares authorized; 49,446,405 shares issued and outstanding, actual and 53,446,405 shares issued and outstanding, as adjusted	494	534
Paid-in capital	303,575	513,155
Other comprehensive loss	(3,455)	(3,455)
Retained earnings	333,625	333,625
Total stockholders' equity	634,239	843,859
Total capitalization	$911,233	$1,120,853

The table above excludes:

- 7,517,248 shares of common stock issuable upon exercise of stock options outstanding at June 30, 2000, with a weighted average exercise price of $23.83 per share;
- 3,061,191 shares of common stock available for grant at June 30, 2000 under our 1996 stock option plan;
- 126,000 shares of common stock available for grant at June 30, 2000 under our 1993 directors' stock option plan;
- 319,096 shares of common stock available for issuance at June 30, 2000 under our employee stock purchase plan;
- 313,396 shares of common stock issuable upon exercise of warrants outstanding at June 30, 2000, at a weighted average exercise price of $24.10 per share;
- 6,274,131 shares of common stock issuable upon conversion of our 4 3/4% convertible subordinated notes.

SELECTED CONSOLIDATED FINANCIAL DATA

The following selected consolidated financial data should be read in conjunction with our consolidated financial statements, related notes and other financial information incorporated herein by reference and "Management's Discussion and Analysis of Financial Condition and Results of Operations" included elsewhere in this prospectus. The consolidated statement of operations data for the fiscal years ended March 31, 1998 and March 31, 1999, and for the nine months ended December 31, 1999, and the consolidated balance sheet data as of March 31, 1998, March 31, 1999 and December 31, 1999 are derived from the audited consolidated financial statements previously filed with the SEC. The consolidated statement of operations data for the six months ended June 30, 1999 and June 30, 2000 and the consolidated balance sheet data as of June 30, 2000 are derived from our unaudited consolidated financial statements and include, in the opinion of management, all adjustments, including normal recurring adjustments, necessary to present fairly the financial information therein. These results are not necessarily indicative of the results that may be expected for future periods. All per share data below has been adjusted to reflect a two-for-one stock split effected in the form of a stock dividend that was paid on September 16, 1999.

	FISCAL YEAR ENDED		NINE MONTH FISCAL PERIOD ENDED	SIX MONTHS ENDED	
	MARCH 31, 1998	MARCH 31, 1999	DECEMBER 31, 1999(1)(2)	JUNE 30, 1999	JUNE 30, 2000
				(UNAUDITED)	
	(IN THOUSANDS, EXCEPT PER SHARE DATA)				
CONSOLIDATED STATEMENT OF OPERATIONS DATA:					
Revenue	$245,894	$200,072	$269,699	$113,526	$ 265,933
Costs and expenses:					
Cost of products sold	98,883	78,440	108,687	43,624	103,223
Research and development	32,012	33,190	45,903	18,766	37,649
Selling, general and administrative	39,934	36,818	50,676	20,321	39,451
In-process research and development	--	--	89,003	89,003	--
Amortization of intangible assets	--	--	45,780	4,164	41,069
Total costs and expenses	170,829	148,448	340,049	175,878	221,392
Income (loss) from operations	75,065	51,624	(70,350)	(62,352)	44,541
Gain on appreciation of foundry investments	--	--	--	--	149,960(3)
Other income (expense), net	10,643	10,668	(4,120)	4,665	(2,152)
Income (loss) before provision (benefit) for income taxes	85,708	62,292	(74,470)	(57,687)	192,349
Provision (benefit) for income taxes	29,141	20,246	(27,989)	(18,372)	70,786
Income (loss) before extraordinary item	56,567	42,046	(46,481)	(39,315)	121,563
Extraordinary item, net of income taxes	--	--	(1,665)	--	--
Net income (loss)	$ 56,567	$ 42,046	$(48,146)	$(39,315)	$ 121,563
Basic net income (loss) per share, before extraordinary item	$ 1.22	$ .90	$ (.97)	$ (.83)	$ 2.48
Diluted net income (loss) per share, before extraordinary item	$ 1.18	$ .88	$ (.97)	$ (.83)	$ 2.16
Basic net income (loss) per share	$ 1.22	$ .90	$ (1.01)	$ (.83)	$ 2.48
Diluted net income (loss) per share	$ 1.18	$ .88	$ (1.01)	$ (.83)	$ 2.16
Shares used in per share calculations:					
Basic	46,478	46,974	47,714	47,189	48,987
Diluted	47,788	47,638	47,714	47,189	58,568

	MARCH 31,		DECEMBER 31,	JUNE 30,
	1998	1999	1999	2000
				(UNAUDITED)
			(IN THOUSANDS)	
CONSOLIDATED BALANCE SHEET DATA:				
Cash, cash equivalents and short-term investments.....	$267,110	$319,434	$214,140	$ 253,581
Working capital.....	283,678	324,204	152,758	254,744
Total assets.....	489,066	540,896	916,155	1,096,364
Long-term debt.....	--	--	260,000	260,000
Stockholders' equity.....	434,686	483,734	482,773	634,239

- ------------------------------

(1) In 1999, we changed our fiscal year end from March 31 to December 31. This period includes financial results for our acquisition of Vantis since June 15, 1999.

(2) Includes the effects of an $89.0 million charge for in-process research and development and the related income tax effects incurred and recorded in conjunction with our acquisition of Vantis on June 15, 1999, and an extraordinary loss of $1.7 million, net of income taxes, for unamortized debt issuance costs related to bank debt retired with the proceeds from our issuance of 4 3/4% convertible subordinated notes during the period. See Notes 4 and 8 to the consolidated financial statements for the period ended December 31, 1999 incorporated by reference in this prospectus.

(3) Includes the effects of a $150 million gain ($92.1 million after-tax) representing the appreciation of investments made in two Taiwanese semiconductor foundry companies. See Note 10 to the unaudited consolidated financial statements for the period ended June 30, 2000 incorporated by reference in this prospectus.

MANAGEMENT'S DISCUSSION AND ANALYSIS OF
FINANCIAL CONDITION AND RESULTS OF OPERATIONS

OVERVIEW

We design, develop and market high performance programmable logic devices, or PLDs, and related software. We are the world's leading supplier of in-system programmable, or ISP-TM-, logic devices. PLDs are widely used semiconductor components that can be configured by the end customer as specific logic circuits, and enable the end customer to shorten design cycle times and reduce development costs. Our products are sold worldwide through an extensive network of independent sales representatives and distributors, primarily to OEMs in the fields of data communications and telecommunications, as well as computing, industrial and military systems. Approximately one-half of our revenue is derived from export sales, mainly to Europe and Asia. We were founded in 1983 and are based in Hillsboro, Oregon.

In June 1999, we acquired Vantis Corporation from Advanced Micro Devices ("AMD") for approximately $500 million in cash. The transaction was accounted for under the purchase method in our consolidated financial statements beginning in the period ended July 3, 1999. We have also agreed with AMD to sign a mutual election under the Internal Revenue Code that will allow us to deduct the purchase price for tax purposes over a 15-year period. We believe that this acquisition has increased our share of the PLD market, accelerated development of new products and technologies and expanded our penetration into new and existing customers.

In March 1997, we entered into an advance payment production agreement with Seiko Epson and its affiliated U.S. distributor, Epson Electronics America, Inc., under which we agreed to advance approximately $85 million, payable upon completion of specific milestones, to Seiko Epson to finance construction of an eight-inch sub-micron wafer manufacturing facility. Under the terms of the agreement, the advance is to be repaid with semiconductor wafers over a multi-year period. The agreement calls for wafers to be supplied by Seiko Epson through Epson Electronics America, Inc. pursuant to purchase agreements with Epson Electronics America, Inc. We also have an option under this agreement to advance Seiko Epson an additional $60 million for additional wafer supply under similar terms. The first payment pursuant to this agreement, approximately $17.0 million, was made during fiscal 1997. During fiscal 1998, we made two additional payments aggregating approximately $34.2 million. The balance of the advance payment is currently anticipated to be made in two installments during fiscal 2000.

In September 1995, we entered into a series of agreements with UMC pursuant to which we agreed to join UMC and several other companies to form a separate Taiwanese company, UICC, for the purpose of building and operating an advanced semiconductor manufacturing facility in Taiwan. Under the terms of the agreement, we invested approximately $49.7 million between fiscal 1996 and fiscal 1998 for an approximate 10% equity interest in UICC and the right to purchase a percentage of the facility's wafer production at market prices.

In October 1996, we entered into an agreement with Utek Corporation, a public Taiwanese company in the wafer foundry business that became affiliated with the UMC Group in 1998, pursuant to which we agreed to make a series of equity investments totaling approximately $17.5 million in Utek under specific terms. In exchange for these investments we received the right to purchase a percentage of Utek's wafer production.

On January 3, 2000, UICC and Utek merged into UMC. We own approximately 73 million shares of UMC common stock and have retained our capacity rights. Due to contractual and regulatory restrictions, the majority of our UMC shares may not be sold until July 2000. These regulatory restrictions will gradually expire between July 2000 and January 2004.

In the fourth quarter of calendar 1999, we changed our reporting period to a 52 or 53 week year ending on the Saturday closest to December 31 from a 52 or 53 week fiscal year ending on the Saturday closest to March 31. For ease of presentation, December 31, March 31 and June 30 have been utilized as the fiscal period end dates for all financial statement captions. Additionally, for purposes of these

consolidated financial statements, the three-month and six-month fiscal periods ended July 3, 1999 are referred to as "the second quarter of 1999" and "the first six months of 1999", respectively. The three-month and six-month fiscal periods ended July 1, 2000 are referred to as "the second quarter of 2000" and "the first six months of 2000", respectively. In the consolidated financial statements, the first six months of 1999 includes the fourth quarter of the twelve-month fiscal year ended March 31, 1999, and the first quarter of the nine-month fiscal period ended December 31, 1999.

RESULTS OF OPERATIONS

The following table sets forth, for the periods indicated, the percentage of revenue represented by selected items reflected in our consolidated statement of operations:

	YEAR ENDED MARCH 31,		NINE MONTH FISCAL PERIOD ENDED DECEMBER 31,	SIX MONTHS ENDED JUNE 30,	
	1998	1999	1999	1999	2000
Revenue	100%	100%	100%	100%	100%
Costs and expenses:					
Cost of products sold	40	39	40	38	39
Research and development	13	17	17	17	14
Selling, general and administrative	16	18	19	18	15
In-process research and development	--	--	33	78	--
Amortization of intangible assets	--	--	17	4	15
Total costs and expenses	69	74	126	155	83
Income (loss) from operations	31	26	(26)	(55)	17
Gain on appreciation of foundry investments	--	--	--	--	56
Other income (expense), net	4	5	(2)	4	(1)
Income (loss) before provision (benefit) for income taxes	35	31	(28)	(51)	72
Provision (benefit) for income taxes	12	10	(11)	(16)	26
Income (loss) before extraordinary item	23	21	(17)	(35)	46
Extraordinary item, net of income taxes	--	--	(1)	--	--
Net income (loss)	23%	21%	(18)%	(35)%	46%

THREE AND SIX MONTHS ENDED JUNE 30, 2000 COMPARED TO THREE AND SIX MONTHS ENDED JUNE 30, 1999

REVENUE. Revenue for the second quarter and first six months of 2000 increased $80.1 million and $152.4 million or 134% and 134% as compared to the same calendar periods of 1999, respectively. In addition to our acquisition of Vantis, the revenue increases are attributable to increased sales of high density products in all geographic areas.

Overall average selling prices increased slightly in the second quarter and first six months of 2000 as compared to the same calendar periods of 1999. Fluctuations in overall average selling prices were due primarily to product mix changes. Although selling prices of mature products generally decline over time, this decline is at times offset by higher selling prices of new products. Our ability to achieve revenue growth is in large part dependent on the continued development, introduction and market acceptance of new products. See "Risk Factors".

GROSS MARGIN. Gross margin as a percentage of revenue was 61.7% and 61.2% in the second quarter and first six months of 2000 as compared to 61.7% and 61.6% in the same calendar periods of 1999, respectively. The gross margin improvement in the second quarter of 2000 compared to recent prior periods is primarily due to reductions in our manufacturing costs and improvements in our product

mix while the decline in gross margin when comparing the first six months of 2000 to the comparable calendar period of 1999 is due to the acquisition of Vantis on June 15, 1999. The decline was partially offset by an improvement in product mix and reductions in our manufacturing costs. Reductions in manufacturing costs resulted primarily from yield improvements, migration of products to more advanced technologies and smaller die sizes, and wafer price reductions.

RESEARCH AND DEVELOPMENT. Research and development ("R&D") expenses increased by approximately 96% and 101%, in the second quarter and first six months of 2000 when compared to the same calendar periods in 1999, respectively. In addition to the acquisition of Vantis, spending increases resulted primarily from the development of new products. We believe that a continued commitment to research and development is essential in order to maintain product leadership of our existing product families and to provide innovative new product offerings, and therefore we expect to continue to make significant future investments in research and development.

SELLING, GENERAL AND ADMINISTRATIVE EXPENSE. Selling, general and administrative ("SG&A") expenses increased 84% and 94%, in the second quarter and first six months of 2000 when compared to the same calendar periods of 1999, respectively. This increase was primarily due to our Vantis acquisition, and to a lesser extent, increased variable costs associated with higher revenue levels.

IN-PROCESS RESEARCH AND DEVELOPMENT COSTS. In-process research and development costs of approximately $89.0 million were recorded on June 15, 1999 in connection with the acquisition of Vantis, and are further described in Note 3 to the unaudited Consolidated Financial Statements for the period ended June 30, 2000 in our Form 10-Q, filed July 20, 2000, which is incorporated herein by reference.

AMORTIZATION OF INTANGIBLE ASSETS. Amortization of intangible assets acquired in the Vantis acquisition were $20.7 million and $41.1 million for the second quarter and first six months of 2000, respectively, compared to $4.2 million for each of the comparable calendar periods of calendar 1999, respectively. The estimated weighted average useful life of the intangible assets for current technology, assembled workforce, customer lists, trademarks, patents and residual goodwill, created as a result of the acquisition, is approximately five years.

GAIN ON APPRECIATION OF FOUNDRY INVESTMENTS. The gain on appreciation of foundry investments in the first half of 2000 was recorded on January 3, 2000 and represents appreciation of foundry investments made in two Taiwanese companies, UICC and Utek (see Note 10 to the unaudited Consolidated Financial Statements for the period ended June 30, 2000 in our Form 10-Q, filed July 20, 2000).

OTHER INCOME (EXPENSE), NET. Other income (expense), net decreased by approximately $2.8 million and $6.8 million in the second quarter and first six months of 2000 as compared to the same periods of calendar 1999, respectively. This was primarily due to interest expense and amortization of debt issuance costs of approximately $3.5 million and $7.1 million in the three and six month periods ended June 30, 2000, respectively, from acquisition related debt and reduced interest income resulting from lower cash and investment balances related to our acquisition of Vantis.

PROVISION FOR INCOME TAXES. The provision (benefit) for income taxes for the second quarter and first six months of 2000 results in effective tax rates of 33.6% and 36.8% of pretax income, as compared to (32.0)% and (31.8%) for the same calendar periods of 1999, respectively. The tax benefit in the second quarter and first six months of 1999 is attributable to the tax effect of the In-process Research and Development cost recognized on June 15, 1999 resulting from the Vantis acquisition. The declining tax rate in the second quarter as compared to the first six months of 2000 is attributable to the application of our marginal tax rate on the unrealized gain on appreciation of foundry investments on January 3, 2000. The effective rate for the second quarter of 2000 of 33.6% is lower than the statutory rate primarily because of tax exempt investment income and tax credits.

FISCAL PERIOD ENDED DECEMBER 31, 1999, FISCAL YEAR 1999 AND FISCAL YEAR 1998

REVENUE. Revenue was $269.7 million in fiscal period 1999, an increase of 35% from fiscal year 1999. Fiscal year 1999 revenue of $200.1 million represented a decrease of 19% from the $245.9 million recorded in fiscal year 1998.

In addition to our acquisition of Vantis, the revenue increase in fiscal period 1999 as compared to fiscal year 1999 was attributable to increased sales of ISP products and recovering demand from Asia. Fiscal year 1999 revenue as compared to fiscal 1998 was negatively impacted by a decline in demand from Asia due to the economic crisis in that region. Furthermore, revenue in all geographic areas was negatively impacted by a decline in demand for our non-ISP product families.

Our sales by geographic area were as follows:

	YEAR ENDED MARCH 31,		NINE MONTH FISCAL PERIOD ENDED DECEMBER 31,
	1998	1999	1999
	(IN THOUSANDS)		
United States	$120,278	$100,778	$126,333
Export sales:			
Europe	61,243	53,649	70,641
Asia	55,853	34,680	55,003
Other	8,520	10,965	17,722
	$245,894	$200,072	$269,699

Revenue from export sales as a percentage of total revenue was approximately 53% for fiscal period 1999, 50% for fiscal year 1999 and 51% for fiscal year 1998. We expect export sales to continue to represent a significant portion of revenue.

The average selling price of our products decreased slightly in fiscal period 1999 as compared to fiscal year 1999. The average selling price of our products was flat in fiscal year 1999 as compared to fiscal year 1998. The decrease in fiscal period 1999 was due primarily to changes in product mix. Although selling prices of mature products generally decline over time, this decline is at times offset by higher selling prices of new products. Our ability to maintain or increase the level of our average selling price is dependent on the continued development, introduction and market acceptance of new products.

GROSS MARGIN. Our gross margin as a percentage of revenue was 60% for fiscal period 1999, 61% for fiscal year 1999 and 60% for fiscal year 1998. The gross margin decline in fiscal period 1999 as compared to fiscal year 1999 is attributable to our acquisition of Vantis on June 15, 1999. The decline was partially offset by an improvement in product mix and reductions in our manufacturing costs. The improvement in fiscal year 1999 as compared to fiscal year 1998 was primarily due to an improvement in product mix and reductions in our manufacturing costs. Reductions in manufacturing costs resulted primarily from yield improvements, migration of products to more advanced technologies and smaller die sizes, and wafer price reductions.

RESEARCH AND DEVELOPMENT. Research and development expense was $45.9 million in fiscal period 1999, $33.2 million in fiscal year 1999 and $32.0 million in fiscal year 1998. For fiscal period 1999, in addition to our acquisition of Vantis, spending increases resulted primarily from the increased development of new products. Spending increases in fiscal year 1999 as compared to fiscal year 1998 resulted primarily from the increased development of new products. We believe that a continued commitment to research and development is essential in order to maintain product leadership in our existing product families and provide innovative new product offerings, and therefore we expect to continue to make significant future investments in research and development.

SELLING, GENERAL AND ADMINISTRATIVE. Selling, general and administrative expense was $50.7 million in fiscal period 1999, $36.8 million in fiscal year 1999 and $39.9 million in fiscal year 1998. The increase in the 1999 fiscal period as opposed to fiscal year 1999 was primarily due to our Vantis acquisition and to a lesser extent attributable to increased variable costs associated with higher revenue levels. The decrease in fiscal year 1999 expense as compared to fiscal year 1998 was primarily due to decreased variable costs associated with lower revenue levels.

IN-PROCESS RESEARCH AND DEVELOPMENT. On June 15, 1999, we bought from AMD all of the outstanding capital stock of Vantis Corporation for approximately $500 million in cash in a transaction accounted for under the purchase method of accounting. Including liabilities assumed and purchase accounting reserves established, the total purchase cost was $583.1 million, of which $511.6 million was allocated to intangible assets. A portion of the intangible asset value was in-process research and development, or IPR&D, with a value of approximately $89 million which was charged to expense on the acquisition date as required by generally accepted accounting principles. The remaining $422.6 million of intangible asset value consisting of existing technology, assembled workforce, customer lists, patents, trademarks and goodwill, is being amortized to operations over 5 years using the straight-line method.

AMORTIZATION OF INTANGIBLE ASSETS. Amortization of intangible assets acquired in the Vantis acquisition was $45.8 million for fiscal period 1999. The estimated weighted average useful life of the intangible assets for current technology, assembled workforce, customer lists, trademarks, patents and residual goodwill, created as a result of the acquisition, is approximately five years.

OTHER INCOME (EXPENSE), NET. Other income (expense), net, was ($4.1) million for fiscal period 1999, a $14.8 million decrease as compared to fiscal year 1999. This was primarily due to interest expense of approximately $9.7 million from acquisition related debt and reduced interest income resulting from lower cash and investment balances in conjunction with the acquisition. Other income (expense), net, was approximately flat for fiscal year 1999 as compared to fiscal year 1998, as higher cash and investment balances were offset by lower interest rates for invested balances, particularly in the second half of the fiscal year.

PROVISION FOR INCOME TAXES. The benefit for income taxes for fiscal period 1999 was 37.6% of the loss before benefit for income taxes. This reflects the estimated rate at which income taxes would be recoverable if a loss tax return were filed. The loss before benefit for income taxes is attributable to the IPR&D charge during the period of approximately $89.0 million and intangible asset amortization of $45.8 million. If these charges were not present, we would have had taxable income and an income tax rate of approximately 36.5%. Our effective tax rate was 32.5% for fiscal year 1999 and 34.0% for fiscal year 1998. The rate change in fiscal year 1999 as compared to fiscal year 1998 was due primarily to changes in the proportion of tax-exempt interest income included in our overall net income. The fiscal 1999 tax rate was also favorably impacted by reduced state taxes resulting from the increased realization of tax credits.

EXTRAORDINARY ITEM, NET OF INCOME TAXES. The extraordinary item, net of income taxes, represents the writeoff of unamortized loan fees related to the $220 million term loan repaid in conjunction with the placement of our 4 3/4% convertible subordinated notes.

QUANTITATIVE AND QUALITATIVE DISCLOSURES ABOUT MARKET RISK

As of June 30, 2000 and December 31, 1999, our investment portfolio consisted of fixed income securities of $227.6 million and $182.1 million, respectively. As with all fixed income instruments, these securities are subject to interest rate risk and will decline in value if market interest rates increase. If market rates were to increase immediately and uniformly by 10% from levels as of June 30, 2000 and December 31, 1999, the decline in the fair value of the portfolio would not be material. Further, we have the ability to hold our fixed income investments until maturity and, therefore, we would not expect to recognize such an adverse impact in income or cash flows.

We have an international subsidiary and branch operations. Additionally, the majority of our silicon wafer purchases are denominated in Japanese yen. We are, therefore, subject to foreign currency rate exposure. To mitigate rate exposure with respect to yen-denominated wafer purchases, we maintain yen-denominated bank accounts and bill our Japanese customers in yen. The yen bank deposits are used to hedge yen-denominated wafer purchases against specific and firm wafer purchases. If the foreign currency rates fluctuate by 10% from rates at June 30, 2000 and December 31, 1999, the effect on our consolidated financial statements would not be material. However, there can be no assurance that there will not be a material impact in the future.

LIQUIDITY AND CAPITAL RESOURCES

As of June 30, 2000, our principal source of liquidity was $253.6 million of cash and short-term investments, an increase of $39.4 million from the balance of $214.1 million at December 31, 1999. The increase was due primarily to cash generated from operations and exercises of stock options. During the first six months of 2000, we generated approximately $22.7 million of cash and cash equivalents from our operating activities as compared with $43.1 million during the first six months of 1999. This change is attributable to working capital accounts as further described below.

Accounts receivable at June 30, 2000 increased by $52.6 million, or 156%, as compared to the balance at December 31, 1999. This increase was primarily due to increased revenue levels and the timing of shipments and collections within the quarter. Inventories at June 30, 2000 increased by $10.6 million, or 41%, as compared to the balance at December 31, 1999 primarily due to increased production in response to higher revenue levels. Prepaid expenses and other current assets at June 30, 2000 increased by $11.4 million, or 109% as compared to the balance at December 31, 1999 primarily due to an increase in the current portion of wafer supply advances. Current deferred income tax assets at June 30, 2000 increased $11.9 million, or 40%, as compared to the balance at December 31, 1999 primarily due to the increase in deferred income on sales to distributors which is recognized currently for income tax purposes, and to a lesser extent the timing of deductions for certain expenses and allowances. Foundry investments, advances and other assets at June 30, 2000 increased by $133.6 million, or 103% as compared to December 31, 1999 primarily due to a gain on appreciation of foundry investments as discussed in Note 10 to the unaudited Consolidated Financial Statements for the period ended June 30, 2000 in our Form 10-Q, filed July 20, 2000. The decrease in non-current deferred income taxes of $39.1 million at June 30, 2000 as compared to December 31, 1999 is due to a reclassification of this balance to non-current deferred tax liabilities. Intangible assets, net, at June 30, 2000 decreased by $45.8 million, or 12% as compared to the balance at December 31, 1999, primarily due to goodwill and other intangibles amortization.

Deferred income on sales to distributors at June 30, 2000 increased by $22.1 million, or 49%, as compared to the balance at December 31, 1999, due primarily to increased billings to distributors associated with higher revenue levels. The $3.9 million, or 31% increase in income taxes payable at June 30, 2000 as compared to the balance at December 31, 1999 is primarily attributable to the timing of tax deductions and payments. Deferred income tax liabilities at June 30, 2000 principally comprise the $57.9 million in taxes provided for the $150.0 million pre-tax gain on appreciation of foundry investments in Taiwan recorded on January 3, 2000 (see Note 10 to the unaudited Consolidated Financial Statements for the period ended June 30, 2000 in our Form 10-Q, filed July 20, 2000), offset by $2.2 million in tax benefit for the subsequent market depreciation of non-restricted foundry shares (see Note 10 to the unaudited Consolidated Financial Statements for the period ended June 30, 2000 in our Form 10-Q, filed July 20, 2000), and by $52.2 million in non-current deferred tax assets relating primarily to intangible asset amortization differences. Such deferred tax assets increased by approximately $13.1 million, or 34% as compared to the balance at December 31, 1999, due primarily to the increased cumulative temporary differences for book and tax amortization of intangible assets.

On October 28, 1999, we issued $260 million in 4 3/4% convertible subordinated notes due on November 1, 2006. These notes require that we pay interest semi-annually on May 1 and November 1. Holders of these notes may convert them into shares of our common stock at any time on or before November 1, 2006, at a conversion price of $41.44 per share, subject to adjustment in certain events. Beginning on November 6, 2002 and ending on October 31, 2003, we may redeem the notes in whole or in part at a redemption price of 102.71% of the principal amount. In the subsequent three twelve-month periods, the redemption price declines to 102.04%, 101.36% and 100.68% of principal, respectively. The notes are subordinated in right of payment to all of our senior indebtedness, and are subordinated to all liabilities of our subsidiaries. At June 30, 2000, we had no senior indebtedness and our subsidiaries had $9.7 million of other liabilities. Issuance costs relative to the convertible subordinated notes are included in Other Assets and aggregated approximately $6.9 million and are being amortized to expense over the lives of the notes. Accumulated amortization amounted to approximately $1.2 million at June 30, 2000.

Capital expenditures were approximately $16.6 million in the first six months of 2000. We expect to spend approximately $30 million to $40 million in capital expenditures for the fiscal year ending December 31, 2000.

In March 1997, we entered into an advance payment production agreement with Seiko Epson and its affiliated U.S. distributor, Epson Electronics America, under which we agreed to advance approximately $85 million, payable upon completion of specific milestones, to Seiko Epson to finance construction of an eight-inch sub-micron wafer manufacturing facility. Under the terms of the agreement, the advance is to be repaid with semiconductor wafers over a multi-year period. The agreement calls for wafers to be supplied by Seiko Epson through Epson Electronics America, pursuant to purchase agreements with Epson Electronics America. We also have an option under this agreement to advance Seiko Epson an additional $60 million for additional wafer supply under similar terms. The first payment pursuant to this agreement, approximately $17.0 million, was made during fiscal 1997. During fiscal 1998, we made two additional payments aggregating approximately $34.2 million. The balance of the advance payment is currently anticipated to be made in future installments.

We entered into a series of agreements with UMC in September 1995, pursuant to which we agreed to join UMC and several other companies to form a separate Taiwanese company, UICC, for the purpose of building and operating an advanced semiconductor manufacturing facility in Taiwan. Under the terms of the agreements, we invested approximately $49.7 million for an approximate 10% equity interest in UICC and the right to receive a percentage of the facility's wafer production at market prices.

In October 1996, we entered into an agreement with Utek, a public Taiwanese company in the wafer foundry business that became affiliated with the UMC Group in 1998, pursuant to which we agreed to make a series of equity investments totaling approximately $17.5 million in Utek under specific terms. In exchange for these investments we received the right to purchase a percentage of Utek's wafer production.

On January 3, 2000, UICC and Utek merged into UMC. We own approximately 73 million shares of UMC common stock and have retained our capacity rights. Due to contractual and regulatory restrictions, the majority of our UMC shares may not be sold until July 2000, or later. These regulatory restrictions will gradually expire between July 2000 and January 2004.

In June 1999, as part of our acquisition of Vantis, we entered into a series of agreements with AMD to support the continuing operations of Vantis. AMD has agreed to provide us with finished silicon wafers through September 2003 in quantities based either on a rolling six-month or an annual forecast. We have committed to buy certain minimum quantities of wafers and AMD has committed to supply certain quantities of wafers during this period. Wafers for our products are manufactured in the United States at multiple AMD wafer fabrication facilities. Prices for these wafers will be reviewed and adjusted periodically.

We believe that, regardless of whether we consummate the sale of the stock offered by this prospectus, our existing cash and cash equivalents, expected cash generation from operations and existing credit facilities combined with our ability to borrow additional funds will be adequate to meet our operating and capital requirements and obligations for at least the next 12 months.

In an effort to secure additional wafer supply, we may from time to time consider various financial arrangements including joint ventures, equity investments, advance purchase payments, loans, or similar arrangements with independent wafer manufacturers in exchange for committed wafer capacity. To the extent that we pursue any such additional wafer financing arrangements, additional debt or equity financing may be required. We may in the future seek new or additional sources of funding. There can be no assurance that such additional financing will be available when needed or, if available, will be on favorable terms. Any future equity financing will decrease existing stockholders' equity percentage ownership and may, depending on the price at which the equity is sold, result in dilution.

Lattice Semiconductor Corporation designs, develops and markets high performance programmable logic devices, or PLDs, and related software. We are the world's leading supplier of in-system programmable, or ISP, logic devices. Programmable logic devices are widely-used semiconductor components that can be configured by the end customer as specific logic circuits, and enable the end customer to shorten design cycle times and reduce development costs. Our end customers are primarily original equipment manufacturers in the markets of data communications and telecommunications, as well as computing, industrial and military systems. During the June 2000 quarter, we derived approximately 66% of our $139.9 million in revenue from the communications market and approximately 20% from the computing market.

In June 1999, we acquired Vantis Corporation, the programmable logic device subsidiary of Advanced Micro Devices. This acquisition has increased our share of the PLD market, accelerated development of new products and technologies and expanded our penetration into new and existing customers.

PLD MARKET BACKGROUND

Three principal types of digital integrated circuits are used in most electronic systems: microprocessors, memory and logic. Microprocessors are used for control and computing tasks, memory is used to store programming instructions and data, and logic is employed to manage the interchange and manipulation of digital signals within a system. Logic contains interconnected groupings of simple logical "and" and logical "or" functions, commonly described as "gates." Typically, complex combinations of individual gates are required to implement the specialized logic functions required for systems applications. While system designers use a relatively small number of standard architectures to meet their microprocessor and memory needs, they require a wide variety of logic circuits in order to achieve end product differentiation.

Logic circuits are found in a wide range of today's digital electronic equipment including communication, computing, industrial and military systems. According to World Semiconductor Trade Statistics, a semiconductor industry association, logic accounted for approximately 27% of the estimated $130 billion worldwide digital integrated circuit market in 1999. The logic market encompasses, among other segments, standard logic, custom-designed application specific integrated circuits, or ASICs, which include conventional gate-arrays, standard cells and full custom logic circuits, and PLDs.

Manufacturers of electronic equipment are increasingly challenged to bring differentiated products to market quickly. These competitive pressures often preclude the use of custom-designed ASICs, which generally entail significant design risks and time delay. Standard logic products, an alternative to custom-designed ASICs, limit a manufacturer's flexibility to adequately customize an end system. PLDs address this inherent dilemma. PLDs are standard products, purchased by systems manufacturers in a "blank" state, that can be custom configured into a virtually unlimited number of specific logic functions by programming the device with electrical signals. PLDs give system designers the ability to quickly create custom logic functions to provide product differentiation without sacrificing rapid time to market. Certain PLD products, including our own, are reprogrammable, meaning that the logic configuration can be modified, if needed, after the initial programming. ISP PLDs, pioneered by us, extend the flexibility of standard reprogrammable PLDs by allowing the system designer to configure and reconfigure the logic functions of the PLD with standard 5-volt or 3.3-volt power supplies without removing the PLD from the system board.

According to Dataquest, the PLD market in 1999 was approximately $2.6 billion. The PLD market has two primary segments: low-density PLDs, with fewer than 1,000 logic gates, and high-density PLDs, with more than 1,000 logic gates. High-density PLD devices include devices based on both the CPLD and

field programmable gate array, or FPGA, architectures. In 1999, Dataquest estimated that the CPLD market was $0.8 billion and the FPGA market was $1.6 billion.

Products based on these alternative high density PLD architectures are generally optimal for different types of logic functions, although many logic functions can be implemented using either architecture. CPLDs are characterized by a regular building block structure of wide-input logic cells, called macrocells, and use of a centralized logic interconnect scheme. FPGAs are characterized by a narrow-input logic cell and use a distributed interconnect scheme. Although CPLDs and FPGAs are better suited for use in different types of logic applications, we believe that a substantial portion of high-density PLD customers utilize both CPLD and FPGA architectures within a single system design, partitioning logic functions across multiple devices to optimize overall system performance and cost.

A growing percentage of the PLD market is made up of devices which operate using 3.3-volt and 2.5-volt power supplies. Lower voltage PLDs benefit end users by consuming less power and providing compatibility with other advanced electronic components. We believe that our innovative low-voltage CPLD products provide us a competitive advantage in the emerging market for low voltage PLDs.

TECHNOLOGY

We believe that our proprietary E2CMOS technology is the preferred process technology for PLD products due to its inherent performance, reprogrammability and testability benefits. E2CMOS technology, through its fundamental ability to be programmed and erased electronically, serves as the foundation for our ISP products.

We pioneered the development of in-system programmability which has become an industry standard feature in the PLD market. Our ISP devices use either 5-volt or 3.3-volt programming signals and, as a result, can be configured and reconfigured by a system designer without being removed from the printed circuit board. Standard E2CMOS PLDs require a 12-volt programming signal and therefore must be removed from the printed circuit board and programmed using specialized hardware. Our ISP devices offer enhanced flexibility compared to standard PLDs and provide significant benefits to our customers. Our ISP devices can allow customers to reduce design cycle times, accelerate time to market, reduce prototyping costs, reduce manufacturing costs and lower inventory requirements. Our ISP devices can also provide customers the opportunity to perform simplified and cost-effective field reconfiguration through a data file transferred by computer disk or serial data signal.

PRODUCTS

We strive to offer innovative and differentiated programmable solutions based on our proprietary technology.

HIGH DENSITY CPLD PRODUCTS

Since 1992, we have focused on developing an industry leading portfolio of high density products and increasing the percentage of our overall revenue derived from this attractive market. At present we offer the broadest range of ISP products in the marketplace. During 1999, approximately 68% of our revenues were derived from high density products, as compared to 49% in 1996. In the future, we plan to continue to introduce new families of innovative, high performance and higher density programmable products, as well as improve the performance and reduce the manufacturing cost of our existing product families based on market needs.

The key features of our CPLD product families are described in the table below:

	SPEED (MHZ)	PROPAGATION DELAY (NANOSECONDS)	GATES	SURFACE MOUNT PINS
ispLSI-Registered Trademark- 1000/E/EA.....	200	4.0	2,000- 8,000	44-128
ispLSI 2000E/VE.....	225	3.5	1,000- 8,000	44-208
ispLSI 3000/E.....	125	7.5	7,000-20,000	160-432
ispLSI 5000V.....	125	7.5	12,000-24,000	208-388
ispLSI 8000/V.....	125	8.5	25,000-50,000	272-492
MACH-Registered Trademark- 1/2.....	180	5.0	1,000- 5,000	44-100
ispMACH-TM- 4/LV/A.....	180	5.0	1,000-10,000	44-256
MACH 5/LV.....	180	5.5	5,000-20,000	100-352

Our newest product families, the ispMACH 4A, ispLSI 2000VE, ispLSI 5000V and ispLSI 8000V, use new innovative architectures and are targeted towards the emerging low voltage portion of the CPLD market.

ISPGDX-REGISTERED TRADEMARK-/V. We recently introduced two new high density product families, ispGDX and ispGDXV, that target a unique aspect of the programmable logic market. These families extend in-system programmability to the circuit board level using an innovative digital cross-point switch architecture. Offered with propagation delays as low as 3.5 nanoseconds, up to 160 input/output pins and complete pin-to-pin signal routing, both the 5-volt ispGDX and the 3.3-volt ispGDXV are targeted towards digital signal interconnect and interface applications.

MIXED SIGNAL PRODUCTS

We have recently added mixed signal products to our portfolio as we believe these devices provide an opportunity to extend our proprietary technology to an untapped potential market.

ISPPAC-REGISTERED TRADEMARK- PRODUCTS. First introduced in 1999, this three device family extends in-system programmability to the analog market. The innovative architecture of the ispPAC allows designers to quickly and easily program resistor and capacitor values, gain and signal polarity and circuit interconnect to implement a wide variety of analog circuits. The initial ispPAC products are targeted towards filtering and signal conditioning applications and can replace numerous discrete analog components. ispPAC designs are implemented and programmed via a personal computer using our software development tool, PAC-Designer-Registered Trademark-.

SOFTWARE DEVELOPMENT TOOLS

All Lattice ISP products are supported by ispDesignEXPERT-TM-, our fourth generation software development tool suite. Supporting both the PC and UNIX platforms, ispDesignEXPERT allows a customer to enter, verify and synthesize a design, perform logic simulation and timing analysis, assign input/output pins and critical speed paths, debug and floorplan a design, execute automatic place and route tasks and download a program to an ISP device. Seamlessly integrated with third-party electronic design automation, or EDA, environments, ispDesignEXPERT leverages customers' prior investments in products offered by Aldec, Cadence, Innoveda, Mentor Graphics, OrCAD, Synopsys, Synplicity and Veribest. In the future, we plan to continue to enhance and expand the capability of our software development tool suite.

We also provide a variety of software algorithms that support in-system programming of our ISP devices via multiple formats and mechanisms. These software products include ispCODE-Registered Trademark-, Turbo ispDOWNLOAD-Registered Trademark-, ispREMOTE-TM-, ispATE-Registered Trademark-, ispSVF-TM- and ispVM-TM-.

LOW DENSITY PLD PRODUCTS

We offer the industry's broadest line of low-density CMOS PLDs based on our 22 families of GAL-Registered Trademark- and PALCE-TM- products offered in over 200 speed, power, package and temperature range combinations. PALCE products were originally introduced by Vantis and are generally compatible with GAL products. GAL and PALCE devices range in complexity from approximately 200 to 1,000 logic gates and are typically assembled in 20-, 24- and 28-pin standard dual in-line packages and in 20- and 28-pin standard plastic leaded chip carrier packages. We offer standard 610, 16V8, 20V8 and 22V10 architectures in a variety of speed grades, with propagation delays as low as 3.5 nanoseconds, the highest performance in the industry. In addition, we offer several proprietary extension architectures, the isp22V10, 6001/2, 16VP8, 16V8Z, 18V10, 20VP8, 20V8Z, 22V10Z, 24V10, 29M16, 20RA10, 20XV10 and 26V12, each of which is optimized for specific applications. We also offer a full range of 3.3-volt standard architectures, the isp22LV10, 16LV8, 20LV8, 22LV10 and 26CLV12, in a variety of speed grades, with propagation delays as low as 3.5 nanoseconds, the highest performance in the industry.

PRODUCT DEVELOPMENT

We place substantial emphasis on new product development and believe that continued investment in this area is required to maintain our competitive position. Our product development activities emphasize new proprietary ISP products, enhancement of existing products and process technologies and improvement of software development tools. Product development activities occur in Hillsboro, Oregon; Silicon Valley, California; Austin, Texas; Colorado Springs, Colorado; Corsham, England; and Shanghai, China.

Research and development expenses were $32.0 million in fiscal year 1998, $33.2 million in fiscal year 1999 and $45.9 million for fiscal period 1999. We expect to continue to make significant future investments in research and development.

OPERATIONS

We do not manufacture our own silicon wafers. We maintain strategic relationships with large semiconductor manufacturers to source our finished silicon wafers. This strategy allows us to focus our internal resources on product, process and market development, and eliminates the fixed cost of owning and operating manufacturing facilities. We are also able to take advantage of the ongoing advanced process technology dedicated development efforts of semiconductor manufacturers. In addition, all of our assembly operations are performed by outside suppliers. We perform certain test operations and reliability and quality assurance processes internally. We have achieved an ISO 9001 quality certification, an indication of our high internal operational standards.

WAFER FABRICATION

The majority of our silicon wafer requirements have historically been supplied by Seiko Epson in Japan pursuant to an agreement with Epson Electronics America, an affiliated U.S. distributor of Seiko Epson. We negotiate wafer volumes, prices and terms with Seiko Epson and Epson Electronics America on a periodic basis. We also receive silicon wafers from the UMC Group in Taiwan pursuant to a series of agreements entered into in 1995. Wafer prices and other purchase terms related to this commitment are subject to periodic adjustment. Currently, the majority of the silicon wafers for our MACH and PALCE products are manufactured by AMD pursuant to an agreement first entered into in 1996 and subsequently amended and restated at the time of our acquisition of Vantis.

ASSEMBLY

After wafer fabrication and initial testing, we ship wafers to independent subcontractors for assembly. During assembly, wafers are separated into individual die and encapsulated in plastic or ceramic

packages. Presently, we have qualified long-term assembly partners in Hong Kong, Malaysia, the Philippines, Singapore, South Korea, Taiwan and Thailand.

TESTING

We electrically test the die on each wafer prior to shipment for assembly. Following assembly, prior to customer shipment, each product undergoes final testing and quality assurance procedures. Final testing on certain products is performed by independent contractors in Malaysia, the Philippines, South Korea, Taiwan, Thailand and the United States.

MARKETING, SALES AND CUSTOMERS

We sell our products directly to end customers through a network of independent manufacturers' representatives and indirectly through a network of independent distributors. We also employ a direct sales management and field applications engineering organization to support our end customers and indirect sales resources. Our end customers are primarily original equipment manufacturers in the fields of communication, computing, industrial and military systems.

At July 2, 2000, we used 23 manufacturers' representatives and three distributors in North America. Arrow Electronics and Avnet provide full distribution coverage. We have also established export sales channels in over 30 foreign countries through a network of over 30 sales representatives and distributors. Approximately one-half of our North American sales and the majority of our export sales are made through distributors.

We protect each of our North American distributors and some of our foreign distributors against reductions in published prices, and expect to continue this policy in the foreseeable future. We also allow returns from these distributors of unsold products under certain conditions. For these reasons, we do not recognize revenue until products are resold by these distributors to an end customer.

We provide technical and marketing support to our end customers with engineering staff based at our headquarters, design centers and selected field sales offices. We maintain numerous domestic and international field sales offices in major metropolitan areas.

Export sales as a percentage of our total revenue were 51% in fiscal year 1998, 50% in fiscal year 1999 and 53% in fiscal period 1999. Both export and domestic sales are denominated in U.S. dollars, with the exception of sales to Japan, which are dominated in yen. If our export sales decline significantly there would be a material adverse impact on our business.

Our products are sold to a large and diverse group of customers. Revenue from one customer, the contract manufacturer Solectron, accounted for approximately 10% of total revenues for the first quarter of 2000. No individual end customer accounted for more than 10% of total revenue in fiscal year 1998 or 1999 or fiscal period 1999.

COMPETITION

The semiconductor industry is intensely competitive and characterized by rapid rates of technological change, product obsolescence and price erosion. Our current and potential competitors include a broad range of semiconductor companies from large, established companies to emerging companies, many of which have greater financial, technical, manufacturing, marketing and sales resources.

The principal competitive factors in the PLD market include product features, price, customer support, and sales, marketing and distribution strength. The availability of competitive software development tools is also critical. In addition to product features such as density, speed, power consumption, reprogrammability, design flexibility and reliability, competition in the PLD market occurs on the basis of price and market acceptance of specific products and technology. We believe that we

compete favorably with respect to each of these factors. We intend to continue to address these competitive factors by working to continually introduce product enhancements and new products, by seeking to establish our products as industry standards in their respective markets, and by working to reduce the manufacturing cost of our products.

In the high density CPLD market, we directly compete primarily with Altera and Xilinx, both of whom offer competing products. We also indirectly compete with other PLD suppliers as well as other semiconductor companies who provide non-PLD based logic solutions. Although to date we have not experienced significant competition from companies located outside the United States, such companies may become a more significant competitive factor in the future. Competition may also increase as we and our current competitors seek to expand our markets. Any such increases in competition could have a material adverse effect on our operating results.

PATENTS

We seek to protect our products and wafer fabrication process technologies primarily through patents, trade secrecy measures, copyrights, mask work protection, trademark registrations, licensing restrictions, confidentiality agreements and other approaches designed to protect proprietary information. There can be no assurance that others may not independently develop competitive technology not covered by our intellectual property rights or that measures we take to protect our technology will be effective.

We hold numerous domestic, European and Japanese patents and have patent applications pending in the United States, Japan and Europe. There can be no assurance that pending patent applications or other applications that may be filed will result in issued patents, or that any issued patents will survive challenges to their validity. Although we believe that our patents have value, there can be no assurance that our patents, or any additional patents that may be issued in the future, will provide meaningful protection from competition. We believe that our success will depend primarily upon the technical expertise, experience, creativity and the sales and marketing abilities of our personnel.

Patent and other proprietary rights infringement claims are common in our industry. There can be no assurance that, with respect to any claim made against us, we could obtain a license on terms or under conditions that would not harm our business.

LICENSES AND AGREEMENTS

SEIKO EPSON/EPSON ELECTRONICS AMERICA

Epson Electronics America, an affiliated U.S. distributor of Seiko Epson, has agreed to provide us with manufactured wafers in quantities based on six-month rolling forecasts. We have committed to buy certain minimum quantities of wafers per month. Wafers for our products are manufactured in Japan at Seiko Epson's wafer fabrication facilities and are delivered to us by Epson Electronics America. Prices for the wafers obtained from Epson Electronics America are reviewed and adjusted periodically.

In March 1997, we entered into an advance production payment agreement with Seiko Epson and Epson Electronics America under which we agreed to advance approximately $85.0 million, payable upon completion of specific milestones, to Seiko Epson to finance construction of an eight-inch sub-micron semiconductor wafer manufacturing facility. The timing of the payments is related to certain milestones in the development of the facility. Under the terms of the agreement, the advance is to be repaid with semiconductor wafers over a multi-year period. The agreement calls for wafers to be supplied by Seiko Epson through Epson Electronics America pursuant to purchase agreements concluded with Epson Electronics America. We also have an option under the agreement to advance Seiko Epson an additional $60.0 million for additional wafer supply under similar terms. The first payment under this agreement,

approximately $17.0 million, was made during fiscal 1997. During fiscal 1998, we made two additional payments aggregating approximately $34.2 million.

UMC GROUP

In September 1995, we entered into a series of agreements with UMC pursuant to which we agreed to join UMC and several other companies to form a separate Taiwanese company, UICC, for the purpose of building and operating an advanced semiconductor manufacturing facility in Taiwan. Under the terms of the agreement, we invested approximately $49.7 million between fiscal 1996 and fiscal 1998 for an approximate 10% equity interest in UICC and the right to purchase a percentage of the facility's wafer production at market prices.

In October 1996, we entered into an agreement with Utek Corporation, a public Taiwanese company in the wafer foundry business that became affiliated with the UMC Group in 1998, pursuant to which we agreed to make a series of equity investments, totaling approximately $17.5 million, in Utek under specific terms. In exchange for these investments we received the right to purchase a percentage of Utek's wafer production.

On January 3, 2000 UICC and Utek merged into UMC. We own approximately 73 million shares of UMC common stock and have retained our capacity rights. Due to contractual and regulatory restrictions, the majority of our UMC shares may not be sold until July 2000. These regulatory restrictions will gradually expire between July 2000 and January 2004.

AMD

In June 1999, as part of our acquisition of Vantis, we entered into a series of agreements with AMD to support the continuing operations of Vantis. AMD has agreed to provide us with finished silicon wafers through September 2003 in quantities based either on a rolling six-month or an annual forecast. We have committed to buy certain minimum quantities of wafers and AMD has committed to supply certain quantities of wafers during this period. Wafers for our products are manufactured in the United States at multiple AMD wafer fabrication facilities. Prices for these wafers will be reviewed and adjusted periodically.

We have also entered into an agreement with AMD pursuant to which we have cross-licensed Vantis patents with AMD patents, having an effective filing date on or before June 15, 1999, related to PLD products. This cross-license was made on a worldwide, non-exclusive and royalty-free basis.

As part of our acquisition of Vantis Corporation, we have acquired certain third-party license rights held by Vantis prior to the acquisition. Included are rights to use certain Xilinx patents to manufacture, market and sell products.

LEGAL PROCEEDINGS

In connection with our acquisition of Vantis, we have agreed to assume both the claims against Altera and the claims by Altera against AMD in the case captioned ADVANCED MICRO DEVICES, INC. V. ALTERA CORPORATION (CASE NO. C-94-20567-RMW) proceeding in the United States District Court for the Northern District of California. This litigation, which began in 1994, involves multiple claims and counterclaims for patent infringement relating to Vantis and Altera programmable logic devices and both parties are seeking damages and injunctive relief.

In April 1999, the United States Court of Appeals for the Federal Circuit reversed earlier jury and District Court decisions and held that Altera is not licensed to the eight AMD patents-in-suit. These eight AMD patents were subsequently assigned to Vantis. Also in April 1999, following the decision of the Court of Appeals, Altera filed a petition for rehearing. In June 1999, the Court of Appeals denied Altera's petition for rehearing.

On May 31, 2000, Altera Corporation filed a complaint against us in U.S. District Court in the Northern District of California, alleging infringement of certain Altera patents by unspecified Lattice products. On June 22, 2000, we answered Altera's complaint denying any infringement by Lattice, and simultaneously brought a series of counterclaims alleging infringement by Altera of certain Lattice patents.

Although there can be no assurance as to the results of litigation, based upon information presently known to management, we do not believe that the ultimate resolution of lawsuits will have a material adverse effect on our business. The foregoing statement constitutes a forward-looking statement and the actual results may differ materially depending on a number of factors, including new court decisions and additional counterclaims made by other parties to such litigation.

Except as described above, we are not currently a party to any material legal proceedings.

The following table sets forth certain information regarding our executive officers and directors:

NAME	AGE	POSITION
Cyrus Y. Tsui	54	President, Chief Executive Officer and Chairman of the Board
Steven A. Laub	41	Senior Vice President and Chief Operating Officer
Stephen A. Skaggs	37	Senior Vice President, Chief Financial Officer and Secretary
Frank J. Barone	60	Corporate Vice President, Product Operations
Stephen M. Donovan	49	Corporate Vice President, Sales
Jonathan K. Yu	59	Corporate Vice President, Business Development
Martin R. Baker	44	Vice President and General Counsel
Randy D. Baker	41	Vice President, Manufacturing
Albert L. Chan	51	Vice President and General Manager, Lattice Silicon Valley
Thomas J. Kingzett	53	Vice President, Reliability and Quality Assurance
Stanley J. Kopec	49	Vice President, Corporate Marketing
Andrew D. Robin	47	Vice President, New Venture Business
Rodney F. Sloss	57	Vice President, Finance
James V. Tortolano	50	Vice President and Co-General Counsel
Kenneth K. Yu	52	Vice President and Managing Director, Lattice Asia
Mark O. Hatfield	78	Director
Daniel S. Hauer	63	Director
Harry A. Merlo	75	Director
Larry W. Sonsini	59	Director

CYRUS Y. TSUI joined Lattice in September 1988 as President, Chief Executive Officer and Director, and in March 1991 was named Chairman of the Board. From 1987 until he joined, Mr. Tsui was Corporate Vice President and General Manager of the Programmable Logic Division of AMD. He was Vice President and General Manager of the Commercial Products Divisions of Monolithic Memories Incorporated (MMI) from 1983 until its merger with AMD in 1987. Mr. Tsui has held technical and managerial positions in the semiconductor industry for over 30 years. He has worked in the programmable logic industry since its inception.

STEVEN A. LAUB joined Lattice in June 1990 as Vice President and General Manager. He was elected Senior Vice President and Chief Operating Officer in August 1996.

STEPHEN A. SKAGGS joined Lattice in December 1992 as Director, Corporate Development. He was elected Senior Vice President, Chief Financial Officer and Secretary in August 1996.

FRANK J. BARONE joined Lattice in June 1999 as a Corporate Vice President as a result of the Vantis acquisition. From September 1997 until he joined, Mr. Barone was Chief Operating Officer of Vantis. Prior thereto, Mr. Barone held various technical and managerial positions at AMD. He has worked in the programmable logic industry since 1978.

STEPHEN M. DONOVAN joined Lattice in October 1989 and has served as Director of Marketing and Director of International Sales. He was elected Vice President, International Sales in August 1993. He was elected Corporate Vice President, Sales, in May 1998. Mr. Donovan has worked in the programmable logic industry since 1982.

JONATHAN K. YU joined Lattice in February 1992 as Vice President, Operations. He was elected Corporate Vice President, Business Development in August 1996. Mr. Yu has held technical and managerial positions in the semiconductor industry for over 30 years.

MARTIN R. BAKER joined Lattice in January 1997 as Vice President and General Counsel. From 1991 until he joined, Mr. Baker held legal positions with Altera Corporation.

RANDY D. BAKER joined Lattice in April 1985 as Manager, Manufacturing and was promoted in 1988 to Director, Manufacturing. He was elected Vice President, Manufacturing in August 1996.

ALBERT L. CHAN joined Lattice in May 1989 as California Design Center Manager and was promoted in 1991 to Director, California Product Development Center. He was elected Vice President, California Product Development in August 1993. He was elected Vice President and General Manager, Lattice Silicon Valley, in August 1997. Mr. Chan has worked in the programmable logic industry since 1983.

THOMAS J. KINGZETT joined Lattice in July 1992 as Director, Reliability and Quality Assurance. He was elected Vice President, Reliability and Quality Assurance in May 1998. Mr. Kingzett has worked in the semiconductor industry for over 25 years.

STANLEY J. KOPEC joined Lattice in August 1992 as Director, Marketing. He was elected Vice President, Corporate Marketing in May 1998. Mr. Kopec has worked in the programmable logic industry since 1985.

ANDREW D. ROBIN joined Lattice in June 1999 as Vice President, New Venture Business as a result of the Vantis acquisition. From March 1998 until he joined, Mr. Robin was Vice President, Marketing at Vantis. Prior thereto, Mr. Robin held various marketing and managerial positions at AMD and MMI. Mr. Robin has worked in the programmable logic industry since 1984.

RODNEY F. SLOSS joined Lattice in May 1994 as Vice President, Finance.

JAMES V. TORTOLANO joined Lattice in June 1999 as a Vice President as a result of the Vantis acquisition. From November 1998 until he joined, Mr. Tortolano was Vice President, General Counsel of Vantis. Prior thereto, Mr. Tortolano held various legal positions at AMD. He has worked in the semiconductor industry since 1983. Mr. Tortolano has informed us that he intends to resign on August 4, 2000.

KENNETH K. YU joined Lattice in January 1991 as Director of Process Technology. He has served as Managing Director, Lattice Asia since November 1992 and was elected Vice President, Lattice Asia in August 1993. Mr. Yu has held technical and managerial positions in the semiconductor industry for over 25 years.

MARK O. HATFIELD has been a member of our board of directors since 1997. Mr. Hatfield is a former U.S. Senator from Oregon.

DANIEL S. HAUER has been a member of our board of directors since 1987. Mr. Hauer is the former Chairman and Chief Executive Officer of Epson Electronics America.

HARRY A. MERLO has been a member of our board of directors since 1983. Mr. Merlo is the President of Merlo Corporation and is the former President and Chairman of Louisiana-Pacific Corporation.

LARRY W. SONSINI has been a member of our board of directors since 1991. Mr. Sonsini is Chairman of the Executive Committee of Wilson Sonsini Goodrich & Rosati, Professional Corporation, a law firm based in Palo Alto, California.

DESCRIPTION OF CAPITAL STOCK

Our authorized capital stock consists of 300,000,000 shares of common stock, $0.01 par value and 10,000,000 shares of preferred stock, $0.01 par value. As of June 30, 2000, there were 49,446,405 shares of common stock outstanding and no shares of preferred stock outstanding.

COMMON STOCK

The holders of common stock are entitled to one vote per share on all matters to be voted upon by the stockholders. Subject to preferences applicable to any outstanding preferred stock, the holders of common stock are entitled to receive ratably such dividends as may be declared from time to time by our board of directors out of funds legally available for distribution and in the event of liquidation, dissolution, or winding up of Lattice, the holders of common stock are entitled to share in all assets remaining after payment of liabilities. The common stock has no preemptive or conversion rights and is not subject to further calls or assessments by Lattice. There are no redemption or sinking fund provisions applicable to the common stock. The common stock currently outstanding is validly issued, fully paid and nonassessable.

CERTAIN CHARTER PROVISIONS

Our restated certificate of incorporation, as amended, and bylaws, as amended, contain certain procedural provisions that could have the effect of delaying, deferring or preventing a change in control of Lattice. These include:

- a provision classifying the board of directors into three classes; and

- a provision requiring that the affirmative vote of two-thirds of the outstanding voting shares of our capital stock is required to approve certain business combinations.

PREFERRED STOCK

Our board of directors has the authority to issue the preferred stock in one or more series and to fix the rights, preferences and privileges, including dividend rights, conversion rights, liquidation rights, voting rights, and the number of shares constituting any series or the designation of such series of preferred stock, without any further vote or action by the stockholders. As of March 31, 2000, there were no outstanding shares of preferred stock or options to purchase preferred stock other than the Preferred Shares Rights Agreement described below. Although it has no present intention to do so, our board of directors may, without stockholder approval, issue preferred stock with voting and conversion rights which could adversely affect the voting power of the holders of common stock. The issuance of preferred stock may have the effect of delaying, deferring or preventing a change of control of Lattice.

RIGHTS AGREEMENT

Effective September 1991, our board of directors approved a Preferred Shares Rights Agreement and declared a dividend distribution payable November 14, 1991 of one Preferred Share Purchase Right (called "rights") for each share of its common stock outstanding on November 14, 1991 and each share of its common stock issued thereafter (subject to certain limitations).

Currently, the rights trade with the shares of common stock. When the rights become exercisable, each Right will entitle the holder to buy one-thousandth of a share of Series A Participating Preferred Stock, $0.01 par value, at an exercise price of $60 per one one-thousandth of a share. The rights will become exercisable and will trade separately from the common stock (unless postponed by action of the disinterested directors of Lattice) on the earlier of (i) ten (10) days following a public announcement that a person or group has acquired, or obtained the right to acquire, beneficial ownership of 20% or more of our outstanding common stock or (ii) ten (10) days following the commencement or announcement of a

tender offer or exchange offer which, if consummated, would result in the beneficial ownership by a person or group of 20% or more of our outstanding common stock.

In general, if any person or group acquires 20% or more of our common stock without approval of our board of directors, each right not held by the acquiring person will entitle its holder to purchase $120 worth of our common stock for an effective purchase price of $60. If, after any person or group acquires 20% or more of our common stock without the approval of our board of directors, we are acquired in a merger or other business combination transaction, each right not held by the acquiring person would entitle its holder to purchase $120 worth of the common stock of the acquiring company for $60. Under certain conditions, we may elect to redeem the rights for $0.01 per right or cause the exchange of each right not held by the acquiring person for one share of our common stock. Additionally, the exercise price, number of rights, and the number of shares of Series A Participating Preferred or common stock that may be acquired for the exercise price are subject to adjustment from time to time to prevent dilution.

The rights are designed to protect and maximize the value of the outstanding equity interests in Lattice in the event of an unsolicited attempt by an acquiror to take over Lattice in a manner or on terms not approved by the board of directors. Takeover attempts frequently include coercive tactics to deprive a corporation's board of directors and its stockholders of any real opportunity to determine the destiny of the corporation. The rights expire on September 11, 2001, unless previously exchanged or redeemed as described above, or terminated in connection with the acquisition of Lattice by consolidation or merger approved by the board of directors and satisfying certain conditions.

The rights are not intended to prevent a takeover of Lattice and will not do so. Nevertheless, the rights may have the effect of rendering more difficult or discouraging an acquisition of Lattice deemed undesirable by the board of directors. The rights may cause substantial dilution to a person or group that attempts to acquire Lattice on terms or in a manner not approved by our board of directors, except pursuant to an offer conditioned upon the negation, purchase or redemption of the rights. The rights have been declared by the board of directors in order to deter such tactics, including a gradual accumulation of shares in the open market of a 20% or greater position to be followed by a merger or a partial or two-tier tender offer that does not treat all stockholders equally.

The description above is qualified in its entirety by reference to the Preferred Shares Rights Agreement dated as of September 11, 1991.

DELAWARE TAKEOVER STATUTE

We are subject to the provisions of Section 203 of the Delaware General Corporation Law, which prohibits a publicly-held Delaware corporation from engaging in any "business combination" with an "interested stockholder" for three years following the date that such stockholder became an interested stockholder, unless:

- prior to such date, the board of directors of the corporation approved either the business combination or the transaction that resulted in the stockholder becoming an interested stockholder;

- upon consummation of the transaction that resulted in the stockholder becoming an interested stockholder, the interested stockholder owned at least 85% of the voting stock of the corporation outstanding at the time the transaction commenced, excluding, for purposes of determining the number of shares outstanding, those shares owned (a) by persons who are directors and also officers and (b) by employee stock plans in which employee participants do not have the right to determine confidentially whether shares held subject to the plan will be tendered in a tender or exchange offer; or

- on or subsequent to such date, the business combination is approved by the board of directors and authorized at an annual or special meeting of stockholders, and not by written consent, by the affirmative vote of at least 66 2/3% of the outstanding voting stock not owned by the interested stockholder.

Generally, a "business combination" includes a merger, asset or stock sale, or other transaction resulting in a financial benefit to the stockholders. An "interested stockholder" is a person who, together with affiliates and associates, owns (or within three years prior did own) 15% or more of the corporation's voting stock.

TRANSFER AGENT AND REGISTRAR

The Transfer Agent and Registrar for the common stock is ChaseMellon Shareholder Services, L.L.C. Its address is 520 Pike Street, Suite 1220, Seattle, Washington 98101 and its telephone number is (206) 674-3034.

UNDERWRITING

Lattice and the underwriters for the offering named below have entered into an underwriting agreement for the shares being offered. Subject to certain conditions, each underwriter has severally agreed to purchase the number of shares indicated in the following table. Goldman, Sachs & Co., Morgan Stanley & Co. Incorporated and Prudential Securities Incorporated are the representatives of the underwriters.

Underwriters	Number of Shares
Goldman, Sachs & Co.	1,700,000
Morgan Stanley & Co. Incorporated	1,700,000
Prudential Securities Incorporated	600,000
Total	4,000,000

If the underwriters sell more shares than the total number in the table above, the underwriters have an option to buy up to an additional 600,000 shares from Lattice to cover these sales. They may exercise that option for 30 days. If any shares are purchased under this option, the underwriters will severally purchase shares in approximately the same proportion as set forth in the table above.

The following table shows the per share and total underwriting discounts and commissions to be paid to the underwriters by Lattice. Such amounts are shown assuming both no exercise and full exercise of the underwriters' option to purchase additional shares.

	Paid by Lattice	
	No Exercise	Full Exercise
Per Share	$ 2.47	$ 2.47
Total	$9,880,000	$11,362,000

Shares sold by the underwriters to the public will initially be offered at the public offering price on the cover of this prospectus. Any shares sold by the underwriters to securities dealers may be sold at a discount of up to $1.49 per share from the public offering price. Any of these securities dealers may resell any shares purchased from the underwriters to other brokers or dealers at a discount of up to $0.10 per share from the public offering price. If all the shares are not sold at the offering price, the representatives may change the offering price and the other selling terms.

Lattice and its executive officers and directors have agreed with the underwriters not to dispose of or hedge any of their common stock or any securities convertible into or exchangeable for shares of common stock during the period from the date of this prospectus continuing through the date 90 days after the date of this prospectus without the prior written consent of Goldman, Sachs & Co. Lattice may, however, without the prior written consent of Goldman, Sachs & Co.:

- issue and sell the shares offered hereby;
- issue stock upon the exercise of options or warrants or upon conversion or exchange of any convertible or exchangeable securities outstanding on the date hereof;
- grant options or issue and sell stock upon the exercise of outstanding stock options or otherwise pursuant to Lattice's and Vantis' stock option or employee stock purchase plans; and
- issue, or agree to issue, securities of Lattice as consideration in connection with any future acquisitions or strategic investments of Lattice or securities of Lattice issuable upon exercise or conversion of the foregoing securities.

In addition, Lattice's executive officers and directors may, without the prior written consent of Goldman, Sachs & Co., dispose of or hedge up to 350,000 shares in the aggregate, but not more than 125,000 shares individually.

In connection with the offering, the underwriters may purchase and sell shares of common stock in the open market. These transactions may include short sales, stabilizing transactions and purchases to cover positions created by short sales. Short sales involve the sale by the underwriters of a greater number of shares than they are required to purchase in the offering. Covered short sales are sales made in an amount not greater than the underwriters' option to purchase additional shares from Lattice in the offering. The underwriters may close out any covered short position by either exercising their option to purchase additional shares or purchasing shares in the open market. Naked short sales are any sales in excess of the underwriters' option to purchase additional shares from Lattice. The underwriters must close out any naked short position by purchasing shares on the open market. A naked short position is more likely to be created if the underwriters are concerned that there may be downward pressure on the price of the common stock in the open market after pricing that could adversely affect investors who purchase in the offering. Stabilizing transactions consist of various bids for or purchases of common stock made by the underwriters in the open market prior to the completion of the offering.

The underwriters also may impose a penalty bid. This occurs when a particular underwriter repays to the underwriters a portion of the underwriting discount received by it because the representatives have repurchased shares sold by or for the account of such underwriter in stabilizing or short covering transactions.

Purchases to cover a short position and stabilizing transactions may have the effect of preventing or retarding a decline in the market price of Lattice's stock, and together with the imposition of the penalty bid, may stabilize, maintain or otherwise affect the market price of the common stock. As a result, the price of the common stock may be higher than the price that otherwise might exist in the open market. If these activities are commenced, they may be discontinued at any time. These transactions may be effected on the Nasdaq National Market, in the over-the-counter market or otherwise.

Lattice's common stock is quoted on the Nasdaq National Market under the symbol "LSCC".

A prospectus in electronic format may be made available on the web sites maintained by one or more underwriters. The underwriters may agree to allocate a number of shares to underwriters for sale to their online brokerage account holders. Internet distributions will be allocated by the lead managers to underwriters that may make Internet distributions on the same basis as other allocations.

Lattice estimates that its share of the total expenses of the offering, excluding underwriting discounts and commissions, will be approximately $400,000. The underwriters have agreed to reimburse Lattice for various expenses, including allocable corporate expenses.

Lattice has agreed to indemnify the several underwriters against certain liabilities, including liabilities under the Securities Act of 1933.

VALIDITY OF COMMON STOCK

The validity of the issuance of the common stock in this offering will be passed upon for us by Wilson Sonsini Goodrich & Rosati, Professional Corporation, Palo Alto, California, and for the underwriters by Davis Polk & Wardwell, Menlo Park, California. Larry W. Sonsini, one of our directors and a partner of Wilson Sonsini Goodrich & Rosati, beneficially owned 31,680 shares of our common stock at June 30, 2000, including 27,000 shares subject to options exercisable within 60 days of that date.

EXPERTS

The consolidated financial statements incorporated in this prospectus by reference to the Annual Report on Form 10-K for the transition period ended December 31, 1999 have been so incorporated in reliance on the report of PricewaterhouseCoopers LLP, independent accountants, given on the authority of said firm as experts in auditing and accounting. The consolidated financial statements of Vantis Corporation as of December 27, 1998 and December 28, 1997, and for the three years in the period ended December 27, 1998, appearing in our current report on Form 8-K filed on June 25, 1999, amended on August 20, 1999 (Form 8-K/A), have been so incorporated in reliance on the report of Ernst & Young LLP, Independent Auditors, given on the authority of said firm as experts in accounting and auditing.

WHERE YOU MAY FIND ADDITIONAL INFORMATION

We file reports, proxy statements and other information with the Securities and Exchange Commission, or SEC, as required by the Securities Exchange Act of 1934. You may read and copy the reports, proxy statements and other information filed by us at the SEC's public reference room at 450 Fifth Street, N.W., Washington, D.C. 20549. Please call the SEC at 1-800-SEC-0330 for information on the operation of the public reference room.

The SEC allows us to incorporate by reference into this prospectus information that we have filed with the SEC. This means that we can disclose important information by referring you to those documents. The information incorporated by reference is considered to be a part of this prospectus. Information that we file later with the SEC will automatically update and supersede previously filed information. We incorporate by reference the documents listed below and any future filings made by us with the SEC under Sections 13(a), 13(c), 14 or 15(d) of the Securities Exchange Act of 1934 until our offering is complete:

- Our annual report on Form 10-K, as amended, for the transition period beginning April 4, 1999 and ending January 1, 2000, filed on March 30, 2000;

- Our quarterly reports on Form 10-Q for the quarter ended April 1, 2000 and for the quarter ended July 1, 2000, filed on May 15, 2000 and July 20, 2000, respectively;

- Our current report on Form 8-K filed on June 25, 1999, and amended on August 20, 1999;

- Our current report on Form 8-K filed on July 11, 2000;

- The description of our common stock contained in our registration statement on Form 8-A, filed on September 27, 1989, including any amendments or reports filed for the purpose of updating such description; and

- All of our filings pursuant to the Securities Exchange Act of 1934 made after the date of the original filing of the registration statement of which this prospectus is a part and prior to the effectiveness of the registration statement.

You may request a copy of these filings, at no cost, by writing or telephoning us at the following address: Investor Relations Department, Lattice Semiconductor Corporation, 5555 N.E. Moore Court, Hillsboro, Oregon 97124-6421, telephone: (503) 268-8000.

No dealer, salesperson or other person is authorized to give any information or to represent anything not contained in this prospectus. You must not rely on any unauthorized information or representations. This prospectus is an offer to sell only the shares offered hereby, but only under circumstances and in jurisdictions where it is lawful to do so. The information contained in this prospectus is current only as of its date.

TABLE OF CONTENTS

4,000,000 Shares

LATTICE SEMICONDUCTOR CORPORATION

Common Stock

[LOGO]

JOINT BOOKRUNNING MANAGERS

GOLDMAN, SACHS & CO.

MORGAN STANLEY DEAN WITTER

PRUDENTIAL VOLPE TECHNOLOGY
a unit of Prudential Securities