LATTICE SEMICONDUCTOR CORPORATION 2002 ANNUAL REPORT

EVOLUTION, ADAPTATION AND DIFFERENTIATION

CORPORATE PROFILE

Lattice Semiconductor Corporation designs, develops and markets high performance programmable logic devices, or PLDs, and related system software. Programmable logic devices are widely-used semiconductor components that can be configured by the end customer as specific logic circuits, and enable the end customer to shorten design cycle times and reduce development costs. Our end customers are primarily original equipment manufacturers in the communications, computing, industrial, automotive, medical, consumer and military end markets.

FINANCIAL HIGHLIGHTS[1]

(In thousands, except per share data)	2002	2001	2000
Revenue	$ 229,126	$ 295,326	$ 567,759
Gross profit	$ 137,580	$ 183,828	$ 349,929
Operating (loss) income	$ (99,563)	$ (25,227)	$ 109,917
Net (loss) income	$ (175,235)	$ (109,519)	$ 167,887
Basic net (loss) income per share	$ (1.59)	$ (1.01)	$ 1.65
Diluted net (loss) income per share	$ (1.59)	$ (1.01)	$ 1.47
Non-GAAP operating income	$ 3,705	$ 59,122	$ 191,790
Non-GAAP earnings (loss)	$ 23,998	$ (40,990)	$ 233,167
Non-GAAP earnings (loss) per share	$ 0.21	$ (0.38)	$ 2.02
Cash and short-term investments	$ 276,880	$ 531,566	$ 535,408
Total assets	$ 941,263	$ 1,185,192	$ 1,295,884
Convertible notes	$ 208,061	$ 260,000	$ 260,000
Stockholders' equity	$ 661,135	$ 839,770	$ 855,655

(1) Includes $150.0 million gain ($92.1 million after tax) on equity market appreciation of our UMC common shares recorded in the first quarter of 2000 and subsequent $152.8 million loss ($94.9 million after-tax) recorded in the third quarter of 2001 related to the market depreciation of these shares. Other unusual and infrequently occurring items that are excluded in Non-GAAP earnings are noted below and explained in Notes 1, 4, 5, 6 and 9 to our Consolidated Financial Statements.

2002 Quarterly Information

	December 2002	September 2002	June 2002	March 2002
Revenue	$ 57,710	$ 56,072	$ 56,466	$ 58,878
Gross profit	$ 34,691	$ 33,643	$ 33,974	$ 35,272
Operating loss	$ (18,207)	$ (23,315)	$ (17,247)	$ (40,794)
Net loss	$ (127,100)	$ (14,371)	$ (8,147)	$ (25,617)
Basic net loss per share	$ (1.14)	$ (0.13)	$ (0.07)	$ (0.23)
Diluted net loss per share	$ (1.14)	$ (0.13)	$ (0.07)	$ (0.23)
Non-GAAP operating income	$ 592	$ 408	$ 676	$ 2,029
Non-GAAP earnings	$ 6,355	$ 6,597	$ 7,028	$ 4,018
Non-GAAP earnings per share	$ 0.06	$ 0.06	$ 0.06	$ 0.04

Annual Reconciliation of GAAP to Non-GAAP Earnings per share**

	2002	2001	2000
Net (loss) income	$ (1.59)	$ (1.01)	$ 1.47
Add:			
Amortization of intangible assets	$ 0.40	$ 0.49	$ 0.46
In-process research and development[1]	$ 0.19	--	--
Valuation allowance for deferred tax assets[2]	$ 1.01	--	--
Tax shield[3]	$ 0.15	$ 0.10	$ 0.09
Difference in effective tax rate[4]	$ 0.05	$ 0.04	--
Non-GAAP earnings (loss)	$ 0.21	$ (0.38)	$ 2.02

Quarterly Reconciliation of GAAP to Non-GAAP Earnings per share**

	December 2002	September 2002	June 2002	March 2002
Net loss	$ (1.14)	$ (0.13)	$ (0.07)	$ (0.23)
Add:				
Amortization of intangible assets	$ 0.12	$ 0.10	$ 0.09	$ 0.10
In-process research and development[1]	--	$ 0.04	--	$ 0.13
Valuation allowance for deferred tax assets[2]	$ 1.00	--	--	--
Tax shield[3]	$ 0.04	$ 0.04	$ 0.04	$ 0.03
Difference in effective tax rate[4]	$ 0.04	$ 0.01	--	$ 0.01
Non-GAAP earnings	$ 0.06	$ 0.06	$ 0.06	$ 0.04

** Notes:

(1) Represents write-off of in-process research and development in conjunction with our August 26, 2002 acquisition of Cerdelinx Technologies, Inc. and our January 18, 2002 acquisition of the FPGA business of Agere Systems, Inc.

(2) In the quarter ended December 31, 2002, we recorded a tax charge of $118.6 million, representing a 100% valuation allowance on our recorded deferred tax assets, in accordance with the provisions of Statement of Financial Accounting Standards No. 109.

(3) Tax shield represents the current period tax benefit available from amortizing gross goodwill and other intangible assets (approximately $750 million as of December 31, 2002) over 15 years on a straight line basis using a 34% tax rate.

(4) The effective tax rate is the ratio of income tax expense to pretax income. The rates for all periods presented in the non-GAAP information presentation are different from the rates in our Statement of Operations, due to the difference in the proportion of taxable income derived from operations. For 2001, further differences in the effective tax rate are attributable to a change in the estimated rate at which tax benefits related to pretax losses will be recovered.

"Nothing, not even the wind that blows, is so unstable as the variety of life on Earth. No species is so perfectly adapted to the physical conditions under which they live that they could not be improved. Species having any advantage over others have the best chance of surviving. And any variation in the least degree injurious is rigidly destroyed. This preservation of favorable variations and the rejection of injurious variations I call Natural Selection. This process works solely by and for the good of each being. Corporeal and mental endowments tend to progress toward perfection."

—Charles Darwin, The Origin of Species

In nature, differentiation is not an option. All species must develop unique characteristics suited to their environment, or die.

Charles Darwin first observed this phenomenon, which he called natural selection. Today we understand that, due to the vagaries of genetics, species invariably mutate. Depending on the specific environment, these mutations are either helpful or harmful. Helpful mutations are naturally propagated. On the other hand, harmful mutations are dispassionately destroyed. Simply stated, survival of the fittest. Through his extensive field research, Darwin discovered this most basic law of the jungle. Over the long run, within a stable environment, natural selection results in the coexistence of unique species.

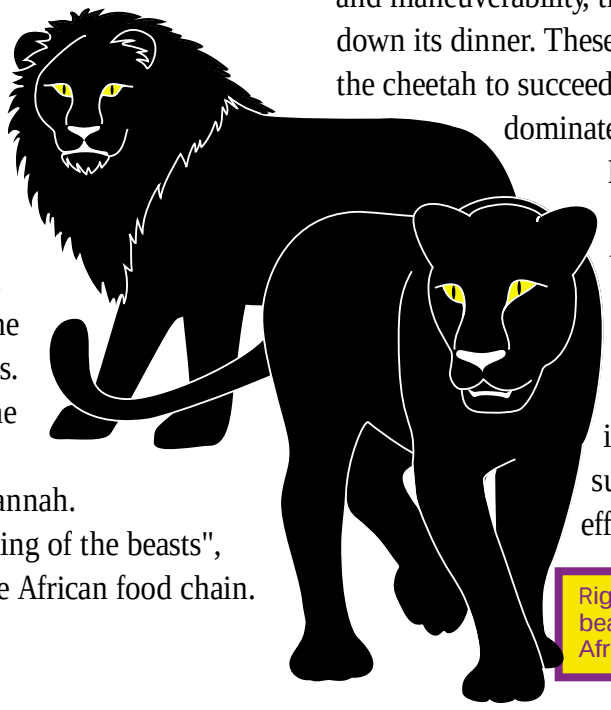
Consider the lion and the cheetah, two well-known predators of the African savannah.

Rightly known as the "king of the beasts", the lion sits proudly atop the African food chain. Owing to its powerful body, broad shoulders and imposing teeth and jaws, the lion eats whatever and whenever it chooses. Lions also exhibit unique social behavior, living in prides and hunting cooperatively. These traits allow lions the luxury of sleeping most of the time, a necessity to digest the large daily intake of meat they require to sustain their muscle mass.

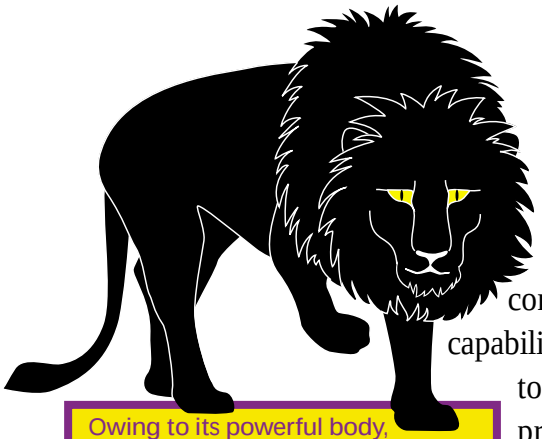
Despite the lion's physical and behavioral advantages, the solitary cheetah competes successfully for scarce game within the same environment. In fact, a single cheetah is a more effective predator than a team of lions, killing with unmatched efficiency. That's because the cheetah's differentiated physiology allows it to make a living alongside the lion.

Unlike any other creature on land, the cheetah is built for speed. With its flexible spine acting as a spring and non-retractable claws firmly gripping the ground, the cheetah accelerates far faster than any other mammal. After reaching top speed, its small aerodynamic head and long tail maintain balance and provide maneuverability. Because no animal can match its unique combination of speed, acceleration and maneuverability, the cheetah can simply run down its dinner. These differentiated traits allow the cheetah to succeed on the savannah, territory dominated by the lion.

Business is no different than nature. Our jungle is the free market. In this environment competition for the customer's dollar is fierce and natural selection is at work. Corporate survivors are those who can effectively assess market trends,



Rightly known as the "king of the beasts," the lion sits proudly atop the African food chain.



Owing to its powerful body, broad shoulders and imposing teeth and jaws, the lion eats whatever and whenever it chooses.

customer needs and competitive capabilities in order to develop products and services that are differentiated.

At Lattice Semiconductor we are keenly aware of this reality. Although our corporation was originally endowed with a less than enviable market position, we have a long and successful history of competing based on innovation and differentiation. This ability has allowed us to build a sustainable position in the highly competitive PLD market.

The free market is just like nature in that it experiences cycles of bounty followed by periods of famine. Unfortunately, last year the PLD environment was especially harsh. During 2002, the semiconductor market suffered the second year of a downturn that is now unprecedented in both magnitude and duration. Our own financial results, though better than most, continue to be negatively impacted by these adverse market conditions.

Revenue for 2002 was $229.1 million, a decline of 22 percent from the $295.3 million reported in 2001. For the year, we reported a net loss of $175.2 million ($1.59 per share). However, these results include a non-cash, non-recurring charge of $118.6 million to eliminate all of our deferred tax assets and $103.3 million of non-cash, acquisition related, charges to write-off in-process research and development and amortize intangible assets. On a non-GAAP basis, we reported net income of $24.0 million ($0.21 per share). We also ended the year with $277 million of cash and a healthy and liquid balance sheet.

In January 2002 we utilized $250 million of our substantial cash reserves to acquire the field programmable gate array (FPGA) business of Agere Systems and entered this attractive segment of the PLD market. The ORCA® family of field programmable system chips (FPSCs), and subsequent internally developed FPSC extension products, address the attractive embedded FPGA market. These devices, combining fixed logic and high-speed input/output (I/O) blocks on a single programmable chip, are differentiated by a more efficient implementation of complex system requirements than generic FPGAs. Our FPSC products also embed leadership serialization-deserialization (SERDES) technology at an unmatched performance level of 3.7 gigabits per second per channel. FPSC devices are ideal for helping customers meet emerging design challenges in their 10-gigabit ethernet and SONET-based systems. Our August 2002 acquisition of Cerdelinx Technologies, a privately held company, provides us with a strong technical team to extend our SERDES technology to higher performance levels. We look for these and future products to be instrumental in allowing us to differentiate our offerings and penetrate the FPGA market.

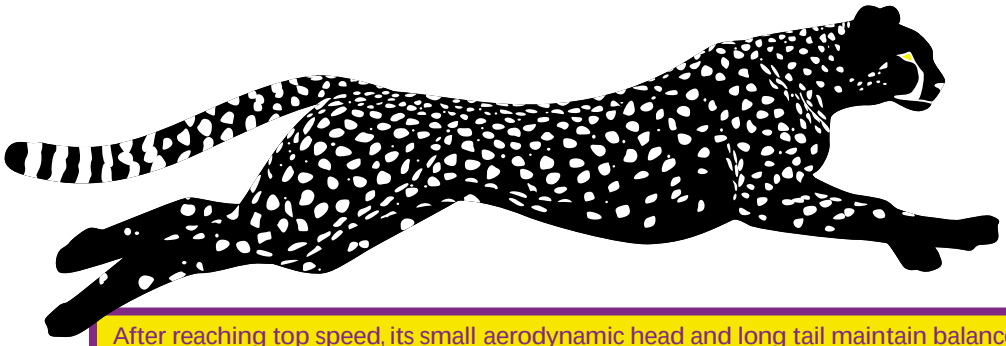
With its flexible spine acting as a spring and non-retractable claws firmly gripping the ground, the cheetah accelerates far faster than any other land animal.

In 2002, we also brought to market the first new innovation in programming technology since our introduction of in-system programmability (ISP™) in 1992. Our extended programmability (XP™) technology and products offer a new alternative for PLD customers. Programmable semiconductors based on XP technology are both infinitely reconfigurable and non-volatile. Today's mainstream programming technologies require customers to choose between these two key attributes. For this reason, we believe that XP products can bring increased value to a significant portion of PLD users. During the second half of 2002, we introduced two new product families, the ispXPLD™ and ispXPGA™, based on our differentiated XP technology.

Continuing our quest for technological innovation, we introduced the ispPAC® POWR family in early 2003. The world's first mixed signal PLD, these products combine programmable logic and programmable analog on a single chip. Based on an intuitive silicon architecture and easy to use software, this device allows designers to easily meet the challenges of sequencing and managing the multiple power supplies prevalent within today's advanced systems. We believe the unique technology underlying the ispPAC POWR will be instrumental in opening new markets for programmable products and for Lattice.

Within our core complex PLD (CPLD) business, accounting for 69 percent of 2002 revenue, we extended and enhanced our position of product leadership in the market. During 2002, we completed the release of our third generation big, fast and wide (BFW) products and initiated the roll-out of our fourth generation. At present, we feature three leadership product families. The ispMACH® 4000V/B/C family offers the world's fastest CPLDs. The innovative ispMACH 5000B family, the world's widest CPLDs, allows customers to implement complex designs at high performance. And our newest family, the ispMACH 4000Z, offers the world's lowest power CPLDs. Our goal for these competitively differentiated products is straightforward: continue to win new customer designs and grow our CPLD market share.

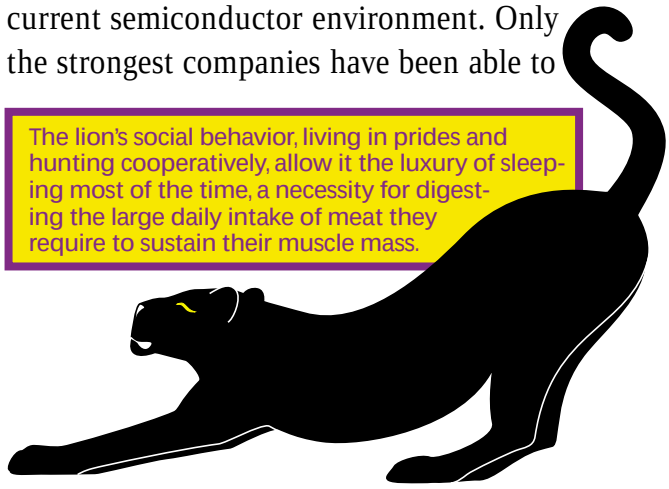
Due to our continued ability to maintain strong gross margins and generate positive operating cash flow, we have made a purposeful decision to sustain investment in new product development throughout the industry downturn. Consequently, last year we spent a record $85.8 million on research and development activities, a 20 percent increase from 2001. In order to support this level of research and development investment we have reduced our annual selling, general and administrative expenses by $33.0 million, or 41 percent, since 2000. Notably, this reduction was accomplished without implementing a layoff. Our relative financial strength has allowed us to make this investment in our business during a time when others have to focus on survival. Fundamentally, we believe the PLD market will be more attractive in the future. And to maximize our competitive success when our



After reaching top speed, its small aerodynamic head and long tail maintain balance and provide maneuverability.

market recovers, we invest to attain a stronger and more differentiated product portfolio.

Just as Darwin observed, the most hostile environments serve to accelerate adaptation and differentiation. This has also been the case in the current semiconductor environment. Only the strongest companies have been able to



retain their full engineering staff and hence their full ability to innovate and expand their product position. We believe our continued commitment to and investment in product development has been a sound strategy. And as a result, our product portfolio is now the most innovative and differentiated in our history.

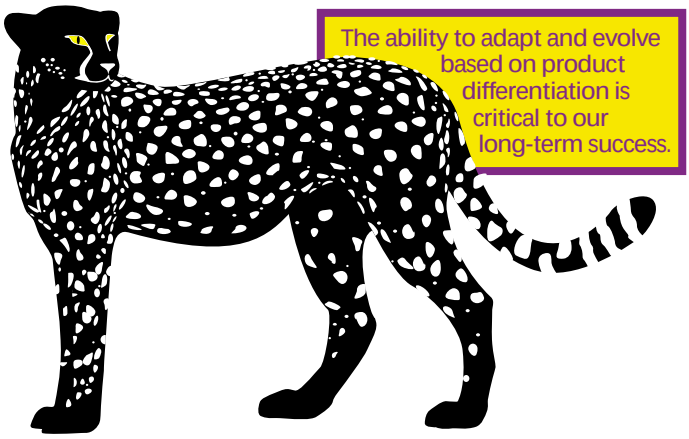
Last year marked the completion of a ten-year evolutionary journey for Lattice. Just over a decade ago, our market participation was confined to the simple PLD (SPLD) segment. Today, if we still relied solely on SPLD products, our reach would be limited to approximately five percent of the market. During the 1990's, we successfully used our differentiated ISP products to enter and build a strong position in the fast growing CPLD segment. Last year we completed our corporate evolution, accomplishing a long-term strategic goal, as we successfully entered the largest segment of the market via the acquisition and internal development of several families of FPGA products. Today, for the first time in our history, we offer products that cover the entire PLD market. Our addressable market is effectively quadruple what it was in 2001. And with our recent introduction of programmable mixed signal products, we are poised to start the cycle anew.

Clearly, we now have a broad line of products. These unique products are positioned in areas that matter to our customers and with attributes that are different than the competitive alternatives. We are pleased with the customer reception and market prospects for these differentiated new products. Like the cheetah, we are positioned to eat where our competitors cannot.

Today we find ourselves in an improved position within our market. However, I am most pleased by the process by which we arrived. We have continuously improved our product line in a manner that is both different from our competitors and advantageous to our customers. This ability to adapt and evolve based on product differentiation is critical to our long-term success. For only through this ability will we be able to both endure bad times and profit from the good times that inevitably follow.

Thank you for your continued support,

Cyrus Tsui
Chairman and Chief Executive Officer



UNITED STATES
SECURITIES AND EXCHANGE COMMISSION

Washington, D.C 20549

FORM 10-K

(Mark one)

[X] ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934 FOR THE FISCAL YEAR ENDED DECEMBER 28, 2002,

or

[ ] TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934 FOR THE TRANSITION PERIOD FROM _____ TO _____

Commission File Number: 000-18032

LATTICE SEMICONDUCTOR CORPORATION

(Exact name of Registrant as specified in its Charter)

Delaware	93-0835214
(State of Incorporation)	(I.R.S Employer Identification No.)
5555 NE Moore Court, Hillsboro, Oregon	97124-6421
(Address of principal executive offices)	(Zip Code)

Registrant's telephone number, including area code: (503) 268-8000

Securities registered pursuant to Section 12(b) of the Act: None
Securities registered pursuant to Section 12(g) of the Act:

Title of Class
Common Stock, $.01 par value

Indicate by check mark whether the Registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the Registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days.

Yes [X] No [ ]

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of the Registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K. [ ]

Indicate by check mark whether the registrant is an accelerated filer (as defined in Rule 12b-2 of the Act).

Yes [X] No [ ]

As of June 29, 2002, the aggregate market value of the shares of voting stock of the Registrant held by non-affiliates was approximately $441.3 million based on the last sales price of our Common Stock on the Nasdaq National Market on such date. Shares of Common Stock held by each officer and director and by each person who owns 5% or more of the outstanding Common Stock have been excluded in that such persons may be deemed affiliates. This determination of affiliate status is not necessarily a conclusive determination for other purposes.

As of March 13, 2003, 112,476,208 shares of the Registrant's common stock were outstanding.

DOCUMENTS INCORPORATED BY REFERENCE

Portions of the definitive proxy statement of the Registrant to be filed pursuant to Regulation 14A for the 2003 Annual Meeting of Stockholders to be held on May 6, 2003 are incorporated by reference in Part III hereof.

FORM 10-K
ANNUAL REPORT
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Item 1. Business.

Lattice Semiconductor Corporation designs, develops and markets high performance programmable logic devices, or PLDs, and related software. Programmable logic devices are widely-used semiconductor components that can be configured by end customers as specific logic circuits, and thus enable shorter design cycle times and reduced development costs. Our end customers are primarily original equipment manufacturers in the communications, computing, industrial, automotive, medical, consumer and military end markets.

In January 2002, we acquired the field programmable gate array ("FPGA") business of Agere Systems, Inc. ("Agere"). This acquisition increased our share of the PLD market, accelerated our entry into the FPGA segment and provided us with additional technical employees and intellectual property.

We report based on a 52 or 53 week year ending on the Saturday closest to December 31. For ease of presentation, we have adopted the convention of using March 31, June 30, September 30 and December 31 as period end dates for all financial statement information.

PLD Market Background

Three principal types of digital integrated circuits are used in most electronic systems: microprocessors, memory and logic. Microprocessors are used for control and computing tasks, memory is used to store programming instructions and data, and logic is employed to manage the interchange and manipulation of digital signals within a system. Logic contains interconnected groupings of simple logical "and" and logical "or" functions, commonly described as "gates." Typically, complex combinations of individual gates are required to implement the specialized logic functions required for systems applications. While system designers use a relatively small variety of standard products to meet their microprocessor and memory needs, they require a wide variety of logic products in order to achieve end product functionality and differentiation.

Logic circuits are found in a wide range of today's digital electronic equipment including communication, computing, industrial, automotive, medical, consumer and military systems. According to World Semiconductor Trade Statistics, a semiconductor industry association, logic accounted for approximately 26% of the estimated $121 billion worldwide digital integrated circuit market in 2002. The logic market encompasses, among other segments, standard logic, custom-designed application specific integrated circuits, or ASICs, which include conventional gate-arrays, standard cells and full custom logic circuits, and PLDs.

Manufacturers of electronic equipment are challenged to bring differentiated products to market quickly. These competitive pressures often preclude the use of custom-designed ASICs, which generally entail significant design risks, non-recurring costs and time delays. Standard logic products, an alternative to custom-designed ASICs, limit a manufacturer's flexibility to adequately customize an end system. PLDs address this inherent dilemma. PLDs are standard products, purchased by systems manufacturers in a "blank" state, that can be custom configured into a virtually unlimited number of specific logic functions by programming the device with electrical signals. PLDs give system designers the ability to quickly create custom logic functions to provide product differentiation without sacrificing rapid time to market. Certain PLD products, including our own, are reprogrammable, meaning that the logic configuration can be modified, if needed, after the initial programming. ISP™ and XP™ PLDs, pioneered by us, extend the flexibility of standard reprogrammable PLDs by allowing the system designer to configure and reconfigure logic functions using system power supplies and without removing the PLD from the system board.

The PLD market was approximately $2.3 billion in 2002. Within this market there are two main segments, complex PLD ("CPLD") and FPGA, each representing a distinct silicon architectural approach. In 2002, CPLD was a $0.5 billion market while FPGA was a $1.8 billion market.

Products based on the two alternative PLD architectures are generally optimal for different types of logic functions, although many logic functions can be implemented using either architecture. CPLDs are characterized by a regular building block structure of wide-input logic cells, called macrocells, and use of a centralized logic interconnect scheme. FPGAs are characterized by a narrow-input logic cell and use a distributed interconnect scheme. FPGAs may also contain dedicated blocks of fixed circuits such as memory, high-speed interface logic or processing engines. Although CPLDs and FPGAs are typically suited for use in distinct types of logic applications, we believe that a substantial portion of PLD customers utilize both CPLD and FPGA architectures within a single system design, partitioning logic functions across multiple devices to optimize overall system performance and cost.

Technology

We believe that our proprietary E²CMOS® technology is the preferred process technology for CPLD products due to its inherent performance, reprogrammability and testability benefits. E²CMOS technology, through its fundamental ability to be programmed and erased electronically, serves as the foundation for our ISP and XP products.

We pioneered the development of in-system programmability (ISP™), which has become an industry standard feature in the PLD market. Our ISP devices can be configured and reconfigured by a system designer without being removed from the printed circuit board. These ISP devices can also provide customers the opportunity to perform simplified and cost-effective field reconfiguration through a data file transferred by computer disk or serial data signal.

Recently, we pioneered the development of XP, or extended programmability, technology. Traditional PLDs have been based on either volatile SRAM technology, which is infinitely reconfigurable, or non-volatile E2/flash technology, which is reprogrammable but not infinitely reconfigurable. Both these technologies require compromises on the part of the customer. XP technology, based on an embedded flash process, is the only programming technology that enables a programmable logic device to be both non-volatile and infinitely reconfigurable.

Products

We strive to offer innovative and differentiated programmable solutions based on our proprietary technology.

CPLD Products

Since 1992, we have focused on developing a leadership portfolio of CPLD products and increasing the percentage of our overall revenue derived from this attractive market. During 2002, approximately 69% of our revenue was derived from CPLD products, as compared to 76% in 2000 and essentially zero in 1992. At present, we offer the industry's broadest line of CPLDs based on our numerous families of ispLSI® and ispMACH® products. In the future, we plan to continue to introduce new families of innovative CPLD products, as well as improve the performance and reduce the manufacturing cost of our existing product families based on market needs.

Our newest CPLD product families use innovative architectures and are targeted towards the low voltage portion of the market. We believe that our multiple families of leadership CPLD products provide us a competitive advantage in this market. The key features of these families are described in the table below:

CPLD FAMILY	OPERATING VOLTAGE	MAXIMUM SPEED (MHZ)	MINIMUM PROP DELAY (NANOSECONDS)	LOGIC (MACROCELLS)	I/O PINS
ispMACH 4000V/B/C	3.3/2.5/1.8	400	2.5	32 – 512	30-208
ispMACH 5000VG/B	3.3/2.5	275	3.0	128 – 1024	92-384
ispMACH 4000Z	1.8	265	3.5	32 – 128	32-92

In addition to high performance, the ispMACH 4000Z family features a new architecture optimized to ensure ultra-low power consumption. Devices within this new family, targeted towards handheld and portable equipment, operate using a maximum static current consumption of 20-30 microamps.

FPGA Products

In 2002, we entered the FPGA market as a result of our acquisition of the FPGA business of Agere and the introduction of an internally developed product family. At present we offer four FPGA product families. These products are targeted toward the mainstream FPGA market. In the future, we plan to introduce new families of innovative, high performance and higher density FPGAs. Key features of our currently available FPGA families are described in the table below:

FPGA FAMILY	OPERATING VOLTAGE	LOGIC (LUTs)	LOGIC (GATES)	MAX RAM (kB)	I/O PINS
ORCA 2	5.0/3.3	400 – 3,600	5K – 100K	58	44-128
ORCA 3	5.0/3.3/2.5	1,152 – 11,552	18K – 340K	185	44-208
ORCA 4	1.5	4,992 – 16,192	260K – 1.1M	404	128-388

In addition, we currently offer a family of field programmable system chips ("FPSC"). FPSCs, which combine generic FPGAs with embedded intellectual property cores on a single programmable chip, offer customers the ability to quickly implement complex system-level designs in a flexible manner. Currently, we offer four FPSC devices, the ORT82G5, ORT8850L, ORLI10G and ORSO82G5, based on our ORCA 4 FPGA platform. These devices incorporate high-speed interface protocols, offering up to 3.7 Gbs SERDES, and other application-specific circuit blocks that allow customers to develop high performance designs to implement 10 Gigabit ethernet and SONET applications within advanced communications systems.

We also offer an additional product family, ispGDX, that targets a unique aspect of the programmable logic market. This family extends in-system programmability to the circuit board level using an innovative digital cross-point switch architecture. Offered with propagation delays as low as 3.5 nanoseconds, up to 240 input/output pins and complete pin-to-pin signal routing, ispGDX products are targeted towards digital signal interconnect and interface applications.

XP Products

Recently we introduced two new product families based on our innovative XP, or extended programmability technology. The ispXPLD family, based on a hybrid architecture, combines the benefits of a wide-input CPLD logic cell with the availability of abundant memory resources. Offering up to 1,024 logic macrocells, propagation delays as low as 4 nanoseconds and up to 512 Kb of memory, the ispXPLD offers customers a new alternative for high density logic designs. The ispXPGA family, based on a mainstream FPGA architecture, offers densities of up to 1.25 million logic gates and brings the benefits of XP technology to the FPGA marketplace.

Other Products

During 1999, we added programmable analog products to our portfolio as we believe these devices provide an opportunity to extend our proprietary technology to an untapped potential market. Our five device ispPAC® family extends in-system programmability to the analog market. The innovative architecture of our ispPAC products allows designers to quickly and easily program resistor and capacitor values, gain and signal polarity and circuit interconnect to implement a wide variety of analog functions. Our initial ispPAC products are targeted towards filtering and signal conditioning applications and can replace numerous discrete analog components. ispPAC designs are implemented and programmed via a personal computer using our software development tool, PAC-Designer®.

Software Development Tools

All of our digital products are supported by our ispLEVER™ 3.0 software development tool suite. This latest version of ispLEVER software supports our CPLD product families, our acquired Agere FPGA and FPSC product families and our newest XP product families. Supporting both the PC and UNIX platforms, ispLEVER allows our customers to enter, verify and synthesize a design, perform logic simulation and timing analysis, assign input/output pins, designate critical paths, debug, execute automatic timing-driven place and route tasks and download a program to one of our ISP devices. Seamlessly integrated with third-party electronic design automation environments, ispLEVER provides a front-to-back design flow that leverages a customer's prior investment in tools offered by Aldec, Cadence, Mentor Graphics, Synopsys and Synplicity. In the future, we plan to continue to enhance and expand the capability of our software development tool suite.

We also provide a variety of software algorithms that support in-system programming of our ISP devices through an interface cable or directly from a system microprocessor.

Low Density PLD Products

We offer the industry's broadest line of low-density CMOS PLDs based on our 18 families of GAL® products offered in over 200 speed, power, package and temperature range combinations. These devices range in complexity from approximately 200 to 1,000 logic gates and are typically assembled in 20-, 24- and 28-pin standard dual in-line packages and in 20- and 28-pin standard plastic leaded chip carrier packages. We offer the standard 16V8, 20V8 and 22V10 architectures in a variety of speed grades, with propagation delays as low as 3.5 nanoseconds, the highest performance in the industry. In addition, we offer several proprietary extension architectures, the isp22V10, 6001/2, 16VP8, 16V8Z, 18V10, 20VP8, 20V8Z, 20RA10, 20XV10 and 26V12, each of which is optimized for specific applications. We also offer a full range of 3.3-volt standard architectures, the isp22LV10, 16LV8, 20LV8, 22LV10 and 26CLV12, in a variety of speed grades, with propagation delays as low as 3.5 nanoseconds, the highest performance in the industry.

Product Development

We place substantial emphasis on new product development and believe that continued investment in this area is required to maintain our competitive position. Our product development activities emphasize new proprietary products, enhancement of existing products and process technologies and improvement of software development tools. Product development activities occur in Hillsboro, Oregon; San Jose, California; Broomfield, Colorado; Naperville, Illinois; Bethlehem, Pennsylvania; Austin, Texas; Salt Lake City, Utah; Shanghai, China; and Corsham, England.

Research and development expenses were $77.1 million in 2000, $71.7 million in 2001 and $85.8 million in 2002. We expect to continue to make significant future investments in research and development.

Operations

We do not manufacture our own silicon wafers. We maintain strategic relationships with large semiconductor foundries to source our finished silicon wafers. This strategy allows us to focus our internal resources on product, process and market development, and eliminates the fixed cost of owning and operating manufacturing facilities. We are also able to take advantage of the ongoing advanced process technology development efforts of semiconductor foundries. In addition, all of our assembly operations and most of our test operations are performed by outside suppliers. We perform certain test operations and reliability and quality assurance processes internally. We have achieved an ISO 9001 quality certification, which is an indication of our high internal operational standards.

Wafer Fabrication

We source silicon wafers from our foundry partners, Seiko Epson in Japan, United Microelectronics Corporation ("UMC") in Taiwan and Chartered Semiconductor Manufacturing, Ltd. ("Chartered Semiconductor") in Singapore, pursuant to agreements with each company and their respective affiliates. We negotiate wafer volumes, prices and other terms with our foundry partners and their respective affiliates on a periodic basis. We also source a very small portion of our wafer requirements from Agere in order to support ongoing manufacturing requirements for certain of our mature FPGA product lines that we obtained as a result of our acquisition.

Assembly

After wafer fabrication and initial testing, we ship wafers to independent subcontractors for assembly. During assembly, wafers are separated into individual die and encapsulated in plastic or ceramic packages. Presently, we have qualified long-term assembly partners in China, Malaysia, the Philippines, South Korea, and Taiwan.

Testing

We electrically test the die on each wafer prior to shipment for assembly. Following assembly, prior to customer shipment, each product undergoes final testing and quality assurance procedures. Final testing on certain products is performed by independent contractors in China, Malaysia, the Philippines, South Korea, and Taiwan and at our Oregon facility.

Marketing, Sales and Customers

We sell our products directly to end customers through a network of independent manufacturers' representatives and indirectly through a network of independent distributors. We also employ a direct sales management and field applications engineering organization to support our end customers and indirect sales resources. Our end customers are primarily original equipment manufacturers in the communication, computing, industrial, automotive, medical, consumer and military end markets.

As of December 2002, we used 18 manufacturers' representatives and two distributors, Arrow Electronics, Inc. and Avnet Inc., in North America. We have also established export sales channels in over 30 foreign countries through a network of over 30 sales representatives and distributors. Approximately one-half of our North American sales and the majority of our export sales are made through distributors.

We protect each of our North American distributors and some of our foreign distributors against reductions in published prices, and expect to continue this policy in the foreseeable future. We also allow returns from these distributors of unsold products under certain conditions. For these reasons, we do not recognize revenue until products are resold by these distributors to an end customer.

We provide technical and marketing support to our end customers with engineering staff based at our headquarters, product development centers and selected field sales offices. We maintain numerous domestic and international field sales offices in major metropolitan areas.

Export sales as a percentage of our total revenue were 57% in 2000, 54% in 2001 and 60% in 2002. Both export and domestic sales are denominated in U.S. dollars, with the exception of sales to Japan, which are dominated in yen. If our export sales decline significantly there would be a material adverse impact on our business and results of operations.

Our products are sold to a large and diverse group of customers. No individual end customer accounted for more than 10% of total revenue in 2000, 2001 or 2002. No export sales to any given country accounted for more than 10% of total revenue in 2000, 2001 or 2002.

Backlog

Our backlog of scheduled and released orders as of December 31, 2002 was approximately $37.2 million as compared to approximately $25.8 million as of December 31, 2001. This backlog consists of direct customer and distributor orders scheduled for delivery within the next 90 days. Distributor orders accounted for the majority of the backlog in both periods. Direct customer orders may be changed, rescheduled or cancelled under certain circumstances without penalty prior to shipment. Additionally, distributor orders generally may be changed, rescheduled or cancelled without penalty prior to shipment. Furthermore, distributor shipments are subject to rights of return and price adjustment. Revenue associated with distributor shipments is not recognized until the product is resold to an end customer. Typically, the majority of our revenue results from orders placed and filled within the same period. Such orders are referred to as "turns orders." By definition, turns orders are not captured in a backlog measurement made at the beginning of a period. We do not anticipate a significant change in this business pattern. For all these reasons, backlog as of any particular date should not be used as a predictor of revenue for any future period.

Competition

The semiconductor industry is intensely competitive and characterized by rapid rates of technological change, product obsolescence and price erosion. Our current and potential competitors include a broad range of semiconductor companies from emerging companies to large, established companies, many of which have greater financial, technical, manufacturing, marketing and sales resources than we do.

The principal competitive factors in the PLD market include product features, price, customer support, and sales, marketing and distribution strength. The availability of competitive software development tools is also critical. In addition to product features such as density, speed, power consumption, reprogrammability, design flexibility and reliability, competition in the PLD market occurs on the basis of price and market acceptance of specific products and technology. We believe that we compete favorably with respect to each of these factors. We intend to continue to address these competitive factors by working to continually introduce product enhancements and new products, by seeking to establish our products as industry standards in their respective markets, and by working to reduce the manufacturing cost of our products.

In the PLD market, we directly compete primarily with Actel Corporation, Altera Corporation and Xilinx Inc., all of whom offer competing products. We also indirectly compete with other semiconductor companies who provide non-PLD based logic solutions. Although to date we have not experienced significant competition from companies located outside the United States, such companies may become a more significant competitive factor in the future. Competition may also increase if other semiconductor companies seek to expand into our market. Any such increases in competition could have a material adverse effect on our operating results.

Patents

We seek to protect our products and wafer fabrication process technologies primarily through patents, trade secrecy measures, copyrights, mask work protection, trademark registrations, licensing restrictions, confidentiality agreements and other approaches designed to protect proprietary information. There can be no assurance that others may not independently develop competitive technology not covered by our intellectual property rights or that measures we take to protect our technology will be effective.

We hold numerous domestic, European and Asian patents and have patent applications pending in the United States, Asia and Europe. There can be no assurance that pending patent applications or other applications that may be filed will result in issued patents, or that any issued patents will survive challenges to their validity. Although we believe that our patents have value, there can be no assurance that our patents, or any additional patents that may be issued in the future, will provide meaningful protection from competition. We believe that our success will depend primarily upon the technical expertise, experience, creativity and the sales and marketing abilities of our personnel.

Patent and other proprietary rights infringement claims are common in our industry. There can be no assurance that, with respect to any claim made against us, we could obtain a license on terms or under conditions that would not harm our business.

Licenses and Agreements

Seiko Epson/Epson Electronics America

Epson Electronics America ("EEA"), an affiliated U.S. distributor of Seiko Epson, has agreed to provide us with manufactured wafers in quantities based on six-month rolling forecasts. We have committed to buy certain minimum quantities of wafers per month. Prices for the wafers obtained from EEA are reviewed and adjusted periodically. Wafers for our products are manufactured in Japan at Seiko Epson's wafer fabrication facilities and are delivered to us by EEA.

In 1997, and as subsequently amended in January 2002, we entered into an advance production payment agreement with Seiko Epson and EEA under which we agreed to advance up to approximately $69 million, payable upon completion of specific milestones, to Seiko Epson to finance construction of an eight-inch sub-micron semiconductor wafer manufacturing facility. The timing of the payments is related to certain milestones in the development of the facility. Under the terms of the agreement, the advance is to be repaid with semiconductor wafers over a multi-year period. The agreement calls for wafers to be supplied by Seiko Epson through EEA pursuant to purchase agreements concluded with EEA. Payments of approximately $51.3 million have been made under this agreement. Cumulatively, approximately $13.3 million of these payments have been repaid to us in the form of semiconductor wafers. We do not anticipate making additional payments under this agreement.

UMC Group

Beginning in 1995, we entered into a series of agreements with UMC pursuant to which we agreed to make several equity investments in entities now directly owned by UMC. Under the terms of these agreements, we invested approximately $68.5 million for the right to purchase a percentage of UMC's wafer production at market prices.

As of December 31, 2002, we owned 88.2 million shares of UMC of which 23.3 million were restricted from sale for more than one year by the terms of our agreements with UMC. Under the terms of our agreements, if we sell any of these restricted shares, our rights to guaranteed wafer capacity at UMC may be reduced on a pro-rata basis based on the number of shares that we sell. If we sell over 10.1 million of these restricted shares, we may lose all of our rights to guaranteed wafer capacity at UMC.

Chartered Semiconductor

In 2002, in order to support our acquired and subsequently developed FPGA products, Chartered Semiconductor and its affiliates agreed to provide us with manufactured wafers in quantities based on six-month rolling forecasts. We have committed to buy certain minimum quantities of wafers per month. Prices for wafers obtained are reviewed and adjusted periodically. Wafers for our products are manufactured at the facilities of Chartered and its affiliates in Singapore.

Advanced Micro Devices

In 1999, as part of our acquisition of Vantis Corporation, a wholly-owned subsidiary of Advanced Micro Devices, Inc. ("AMD"), we entered into an agreement with AMD pursuant to which we have cross-licensed Vantis patents with AMD patents, having an effective filing date on or before June 15, 1999, related to PLD products. This cross-license was made on a worldwide, non-exclusive and royalty-free basis.

Additionally, as part of our acquisition of Vantis, we acquired certain third-party license rights held by Vantis prior to the acquisition. Included are rights to use certain Xilinx patents to manufacture, market and sell products.

Agere Systems

In January 2002, as part of our acquisition of the FPGA business of Agere, we entered into an intellectual property agreement with Agere and Agere Systems Guardian Corporation. Pursuant to this agreement, these Agere companies assigned or licensed to us certain FPGA and FPSC patents, trademarks, software and other intellectual property rights and technology, and we licensed back rights in these same assets. These cross-licenses were made on a worldwide and royalty-free basis.

Altera

In July 2001, we entered into a comprehensive, royalty-free patent cross-license agreement and a multi-year patent peace agreement with Altera.

Employees

As of December 31, 2002 we had 1,073 full-time employees. We believe that our future success will depend, in part, on our ability to continue to attract and retain highly skilled technical and management personnel. None of our employees is subject to a collective bargaining agreement. We have never experienced a work stoppage and consider our employee relations good.

EXECUTIVE OFFICERS AND DIRECTORS OF THE REGISTRANT

The following individuals currently serve as our executive officers and directors:

NAME	AGE	POSITION
Cyrus Y. Tsui	57	Chief Executive Officer and Chairman of the Board
Steven A. Laub	44	President and Director
Stephen A. Skaggs	40	Senior Vice President, Chief Financial Officer and Secretary
Frank J. Barone	63	Corporate Vice President, Product Operations
Stephen M. Donovan	51	Corporate Vice President, Sales
Jonathan K. Yu	62	Corporate Vice President, Business Development
Martin R. Baker	47	Vice President and General Counsel
Jan Johannessen	47	Vice President, Investments
Rodney F. Sloss	59	Vice President, Finance
Kenneth K. Yu	55	Vice President and Managing Director, Lattice Asia
Mark O. Hatfield	80	Director
Daniel S. Hauer	66	Director
Soo Boon Koh	52	Director
Harry A. Merlo	77	Director
Larry W. Sonsini	61	Director

Cyrus Y. Tsui joined Lattice in September 1988 as President and Chief Executive Officer and in March 1991 was named Chairman of the Board. From 1987 until he joined, Mr. Tsui was Corporate Vice President and General Manager of the Programmable Logic Division of AMD. He was Vice President and General Manager of the Commercial Products Divisions of Monolithic Memories Incorporated (MMI) from 1983 until its merger with AMD in 1987. Mr. Tsui has held technical and managerial positions in the semiconductor industry for over 30 years and worked in the programmable logic industry since its inception.

Steven A. Laub joined Lattice in June 1990 as Vice President and General Manager. He was elected Senior Vice President and Chief Operating Officer in August 1996. In October 2001, he was promoted to President and elected to our Board of Directors.

Stephen A. Skaggs joined Lattice in December 1992 as Director, Corporate Development. He was elected Senior Vice President, Chief Financial Officer and Secretary in August 1996.

Frank J. Barone joined Lattice in June 1999 as a Corporate Vice President as a result of our Vantis acquisition. From September 1997 until he joined our company, Mr. Barone was Chief Operating Officer of Vantis. Prior thereto, Mr. Barone held various technical and managerial positions at AMD. He has worked in the programmable logic industry since 1978.

Stephen M. Donovan joined Lattice in October 1989 and has served as Director of Marketing and Director of International Sales. He was elected Vice President, International Sales in August 1993. He was promoted to Corporate Vice President, Sales, in May 1998. Mr. Donovan has worked in the programmable logic industry since 1982.

Jonathan K. Yu joined Lattice in February 1992 as Vice President, Operations. He was elected Corporate Vice President, Business Development in August 1996. Mr. Yu has held technical and managerial positions in the semiconductor industry for over 30 years.

Martin R. Baker joined Lattice in January 1997 as Vice President and General Counsel. From 1991 until he joined Lattice, Mr. Baker held legal positions with Altera Corporation.

Jan Johannessen rejoined Lattice in October 2001 as Vice President, Investments. Since 1993 he worked as an independent venture capitalist. He originally joined Lattice in 1983 and served as Vice President and Chief Financial Officer between 1987 and 1993.

Rodney F. Sloss joined Lattice in May 1994 as Vice President, Finance.

Kenneth K. Yu joined Lattice in January 1991 as Director of Process Technology. He has served as Managing Director, Lattice Asia since November 1992 and was elected Vice President, Lattice Asia in August 1993. Mr. Yu has held technical and managerial positions in the semiconductor industry for over 25 years.

Mark O. Hatfield has been a member of our board of directors since 1997. Mr. Hatfield is a former U.S. Senator from Oregon. He currently serves as a professor at Portland State University, Lewis & Clark College and George Fox University.

Daniel S. Hauer has been a member of our board of directors since 1987. Mr. Hauer is the former Chairman and Chief Executive Officer of Epson Electronics America.

Soo Boon Koh joined our board of directors in August 2000. Ms. Koh is a managing partner of Partners Fund, L.P., a venture capital firm located in Singapore and the United States.

Harry A. Merlo was a founding member of our board of directors in 1983. Mr. Merlo is the President of Merlo Corporation and is the former founding President and Chairman of Louisiana-Pacific Corporation.

Larry W. Sonsini has been a member of our board of directors since 1991. Mr. Sonsini is a member of Wilson Sonsini Goodrich and Rosati, Professional Corporation, a law firm, and Chairman of the firm's Executive Management Committee.

Available Information

We file electronically with the Securities and Exchange Commission ("SEC") our annual, quarterly and current reports, proxy statements and other information pursuant to Section 13(a) or 15(d) of the Securities Exchange Act of 1934. Publicly available documents filed with the SEC may be read or copied at the SEC's Public Reference Room located at 450 Fifth Street, N.W., Washington, D.C. 20549. You may obtain information on the operation of the Public Reference Room by calling the SEC at 1-800-SEC-0330. The SEC maintains an Internet site that contains reports, proxy and information statements, and other information regarding issuers that file electronically with the SEC. The address of that site is http://www.sec.gov.

Our website is www.latticesemi.com. We make available free of charge through our website, via a link to the SEC's website at http://www.sec.gov, our annual reports on Form 10-K, quarterly reports on Form 10-Q and current reports on Form 8-K and amendments to those reports as soon as reasonably practicable after such materials are electronically filed with, or furnished to, the SEC. You may also obtain free copies of these materials by contacting our Investor Relations Department at 5555 N.E. Moore Court, Hillsboro, Oregon 97124-6421, telephone (503) 268-8000.

Item 2. Properties.

Our corporate headquarters consists of land and 200,000 square feet of buildings we own in Hillsboro, Oregon. We also own two research and development facilities, totaling 29,000 square feet and approximately 6,000 square feet of dormitory facilities in Shanghai, China. We lease (through 2008) a 133,000 square foot research and development facility in San Jose, California. We also lease, on a short-term basis, research and development facilities in Colorado, Illinois, Pennsylvania, Texas, Utah and the United Kingdom. We also lease, on a short-term basis, office facilities in multiple metropolitan locations, for our domestic and international sales staff. Additionally, we lease (through 2006) an 80,000 square foot facility in Sunnyvale, California which has been subleased to a third party through the end of the lease term.

Item 3. Legal Proceedings.

We are not currently a party to any material legal proceedings.

Item 4. Submission of Matters to a Vote of Security Holders.

Not applicable.

PART II

Item 5. Market for the Registrant's Common Stock and Related Stockholder Matters.

Our common stock is traded on the over-the-counter market and prices are quoted on the Nasdaq National Market under the symbol "LSCC." The following table sets forth the low and high sale prices for our common stock for the last two fiscal years and for the period since December 31, 2002, as reported by the Nasdaq National Market. On March 13, 2003, the last reported sale price of our common stock was $7.18. As of March 13, 2003, we had approximately 535 stockholders of record.

	LOW	HIGH
2001:		
First Quarter	$16.76	$27.25
Second Quarter	15.88	27.64
Third Quarter	14.04	25.85
Fourth Quarter	14.36	22.65
2002:		
First Quarter	$17.06	$24.14
Second Quarter	6.94	18.49
Third Quarter	5.35	9.36
Fourth Quarter	4.08	10.79
2003:		
First Quarter (through March 13, 2003)	$ 6.47	$10.30

The payment of dividends on our common stock is within the discretion of our Board of Directors. We intend to retain earnings to finance the growth of our business. We have never paid cash dividends.

Recent Sales of Unregistered Securities

On May 7, 2002, we issued a warrant to purchase 119,074 shares of our common stock to Bain & Company, Inc., in connection with consulting services provided to us. The warrant has an exercise price of $10.70 per share, and vests at a rate of 9,922.83 shares on the first day of each month, beginning March 1, 2002, subject to Bain's continued service as a consultant to us. On April 23, 2002, we issued 206,200 shares of unregistered Lattice common stock to Bain upon the exercise of previously issued warrants, for an aggregate purchase price of $2,835,250. The foregoing transactions were exempt from registration under the Securities Act of 1933, as amended, pursuant to Section 4(2) thereof on the basis that the transactions did not involve a public offering.

Following our acquisition of Cerdelinx Technologies, Inc. in August 2002 and prior to the end of fiscal 2002, we issued an aggregate of 27,124 shares of unregistered Lattice common stock to five former directors and consultants of Cerdelinx upon the exercise of certain options assumed in connection with the Cerdelinx acquisition, for an aggregate purchase price of $11,120.84. The foregoing transactions were exempt from registration under the Securities Act of 1933, as amended, pursuant to Section 4(2) thereof on the basis that the transactions did not involve a public offering.

Item 6. Selected Financial Data.

	YEAR ENDED			NINE MONTHS ENDED	YEAR ENDED
	DEC. 31, 2002	DEC. 31, 2001	DEC. 31, 2000	DEC. 31, 1999	MAR. 31, 1999
	(In thousands, except per share data)				
STATEMENT OF OPERATIONS DATA:					
Revenue	$ 229,126	$ 295,326	$ 567,759	$269,699	$200,072
Costs and expenses:					
Cost of products sold	91,546	111,498	217,830	108,687	78,440
Research and development	85,776	71,679	77,057	45,903	33,190
Selling, general and administrative	48,099	53,027	81,082	50,676	36,818
In-process research and development	29,853	—	—	89,003	—
Amortization of intangible assets[1]	73,415	84,349	81,873	45,780	—
	328,689	320,553	457,842	340,049	148,448
(Loss) income from operations	(99,563)	(25,227)	109,917	(70,350)	51,624
(Loss) gain on foundry investments	—	(152,795)	149,960	—	—
Interest and other income (expense), net	6,194	4,056	2,194	(6,787)	10,668
(Loss) income before provision (benefit) for income taxes	(93,369)	(173,966)	262,071	(77,137)	62,292
Provision (benefit) for income taxes	81,866	(64,447)	94,184	(28,991)	20,246
Net (loss) income	$(175,235)	$ (109,519)	$ 167,887	$ (48,146)	$ 42,046
Basic net (loss) income per share	$ (1.59)	$ (1.01)	$ 1.65	$ (0.50)	$ 0.45
Diluted net (loss) income per share	$ (1.59)	$ (1.01)	$ 1.47	$ (0.50)	$ 0.44
Shares used in per share calculations:					
Basic	110,193	108,814	101,716	95,428	93,948
Diluted	110,193	108,814	120,321	95,428	95,276
BALANCE SHEET DATA:					
Cash and short-term investments	$ 276,880	$ 531,556	$ 535,408	$214,140	$319,434
Total assets	$ 941,263	$1,185,982	$1,295,884	$916,155	$540,896
Convertible notes	$ 208,061	$ 260,000	$ 260,000	$260,000	$ —
Stockholders' equity	$ 661,135	$ 839,770	$ 855,655	$482,773	$483,734

[1] Includes $2,962 and $397 of amortization of deferred stock compensation expense for the year ended December 31, 2002 and December 31, 2001, respectively, attributable to Research and Development activities.

All share and per share amounts have been adjusted retroactively to reflect two-for-one stock splits effected in the form of stock dividends and paid on October 11, 2000 and September 16, 1999.

	2002				2001			
	DEC.	SEPT.	JUNE	MAR.	DEC.	SEPT.	JUNE	MAR.
UNAUDITED QUARTERLY DATA:								
Revenue	$ 57,710	$ 56,072	$56,466	$ 58,878	$ 52,108	$ 58,038	$74,082	$111,098
Gross profit	$ 34,691	$ 33,643	$33,974	$ 35,272	$ 32,286	$ 36,043	$46,311	$ 69,188
Net (loss) income	$(127,100)	$(14,371)	$ (8,147)	$(25,617)	$(12,517)	$(104,601)	$ (3,677)	$ 11,276
Basic net (loss) income per share	$ (1.14)	$ (0.13)	$ (0.07)	$ (0.23)	$ (0.11)	$ (0.96)	$ (0.03)	$ 0.10
Diluted net (loss) income per share	$ (1.14)	$ (0.13)	$ (0.07)	$ (0.23)	$ (0.11)	$ (0.96)	$ (0.03)	$ 0.10

Item 7. Management's Discussion and Analysis of Financial Condition and Results of Operations.

This Annual Report on Form 10-K contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933, as amended, and Section 21E of the Exchange Act. Any statements about our expectations, beliefs, plans, objectives, assumptions or future events or performance are not historical facts and may be forward-looking. We use words or phrases such as "anticipates," "believes," "estimates," "expects," "intends," "plans," "projects," "may," "will," "should," "continue," "ongoing," "future," "potential" and similar words or phrases to identify forward-looking statements.

Forward-looking statements involve estimates, assumptions, risks and uncertainties that could cause actual results to differ materially from those expressed in them. Among the key factors that could cause our actual results to differ materially from the forward-looking statements are delay in product or technology development, change in economic conditions of the various markets we serve, lack of market acceptance or demand for our new products, dependencies on silicon wafer suppliers and semiconductor assemblers, the impact of competitive products and pricing, opportunities or acquisitions that we pursue, the availability and terms of financing, and the other risks that are described herein and that are otherwise described from time to time in our filings with the Securities and Exchange Commission, including but not limited to the items discussed in "Factors Affecting Future Results" set forth in "Management's Discussion and Analysis of Financial Condition and Results of Operations" in Item 7 of this report. You should not unduly rely on forward-looking statements because our actual results could materially differ from those expressed in any forward-looking statements made by us. Further, any forward-looking statement applies only as of the date on which it is made. We are not required to update any forward-looking statement or statements to reflect events or circumstances after the date on which such statement is made or to reflect the occurrence of unanticipated events.

Lattice Semiconductor Corporation designs, develops and markets high performance programmable logic devices, or PLDs, and related software. Programmable logic devices are widely-used semiconductor components that can be configured by the end customer as specific logic circuits, and enable the end customer to shorten design cycle times and reduce development costs. Our end customers are primarily original equipment manufacturers in the communications, computing, industrial, automotive, medical, consumer and military end markets.

Results of Operations

The following table sets forth, for the periods indicated, the percentage of revenue represented by selected items reflected in our Consolidated Statement of Operations:

	YEAR ENDED DEC. 31, 2002	YEAR ENDED DEC. 31, 2001	YEAR ENDED DEC. 31, 2000
Revenue	100%	100%	100%
Costs and expenses:			
Cost of products sold	40	38	38
Research and development	38	24	14
Selling, general and administrative	21	18	14
In-process research and development	13	—	—
Amortization of intangible assets	32	29	15
Total costs and expenses	144	109	81
(Loss) income from operations	(44)	(9)	19
Other income (expense), net	3	(50)	27
(Loss) income before provision (benefit) for income taxes	(41)	(59)	46
Provision (benefit) for income taxes	36	(22)	16
Net (loss) income	(76)%	(37)%	30%

Acquisitions. On August 26, 2002, we completed the stock for stock acquisition of Cerdelinx Technologies, Inc. ("Cerdelinx") for 2.6 million shares valued at $8.30 per share. This transaction was accounted for as an asset purchase, and accordingly, the results of operations for Cerdelinx and estimated fair value of assets acquired and liabilities assumed are included in our consolidated financial statements beginning August 26, 2002. In estimating the fair value of the assets acquired, management considered various factors, including an appraisal. In-process research and development (IPR&D) costs were appraised at $5.7 million and charged to operations on the acquisition date. Remaining intangible asset costs are being amortized to operations over a period averaging five years. See note 4 to our Consolidated Financial Statements.

On January 18, 2002, we completed the acquisition of the field-programmable gate array ("FPGA") business ("Agere FPGA") of Agere Systems Inc. ("Agere") for $250 million in cash. This transaction was accounted for as a purchase, and accordingly, the results of operations for Agere FPGA and estimated fair value of assets acquired and liabilities assumed are included in our consolidated financial statements beginning January 18, 2002. In estimating the fair value of the assets acquired, management considered various factors, including an appraisal. In-process research and development (IPR&D) costs were appraised at $24.2 million and charged to operations on the acquisition date. Remaining intangible asset costs are being amortized to operations over 6.3 years. See note 5 to our Consolidated Financial Statements.

R*evenue.* Revenue was $229.1 million in 2002, a decrease of 22% from 2001. Revenue was $295.3 million in 2001, a decrease of 48% from 2000. The composition of our revenue by product family for the years presented was as follows:

	YEAR ENDED DEC. 31, 2002	YEAR ENDED DEC. 31, 2001	YEAR ENDED DEC. 31, 2000
FPGA	12%	0%	0%
CPLD	69%	76%	76%
SPLD	19%	24%	24%

Prior to the acquisition of Agere FPGA, we had no revenue from FPGA products.

During 2001, the semiconductor and PLD markets experienced a significant downturn, which continued through 2002. Our revenue decrease in 2002 as compared to 2001 and our revenue decrease in 2001 as compared to 2000, was a result of this downturn and the resultant decrease in demand for our products. Revenue declined across all geographies, and demand across most end markets remains weak.

Our sales by geographic region were as follows:

	YEAR ENDED DEC. 31, 2002	YEAR ENDED DEC. 31, 2001	YEAR ENDED DEC. 31, 2000
		(in thousands)	
United States	$ 92,086	$135,832	$245,882
Export sales:			
Europe	58,871	81,177	158,591
Asia	67,324	62,582	120,285
Other	10,845	15,735	43,001
	137,040	159,494	321,877
	$229,126	$295,326	$567,759

Revenue from export sales as a percentage of total revenue was approximately 60% for 2002, 54% for 2001 and 57% for 2000. We expect export sales to continue to represent a significant portion of revenue.

During 2002, total units sold decreased by 19% and our overall average selling prices decreased by three percent when compared to 2001. Both units sold and average selling price were adversely impacted by the continued downturn in the semiconductor and PLD markets. During 2001, total units sold decreased by 47% while the average selling price of our products was approximately flat when compared to 2000. Although selling prices of mature products generally decline over time, this decline is at times offset by higher selling prices of new products. Our ability to maintain or increase the level of our average selling price is dependent on the continued development, introduction and market acceptance of new products. See "Factors Affecting Future Results."

Gross Margin. Our gross margin percentage was 60% for 2002, 62% for 2001, and 62% for 2000. The decrease in gross margin percentage in 2002 was primarily due to the increased proportion of fixed manufacturing costs due to a decline in production volume. Reductions in our overall manufacturing costs and improvements in our product mix generally offset an increased proportion of fixed manufacturing costs in 2001. Product mix in 2001 was favorably affected by a higher ratio of previously deferred income compared to income from direct customer sales. Reductions in manufacturing costs resulted primarily from on-going yield improvements, migration of products to more advanced technologies and smaller die sizes.

Research and Development. Research and development expense was $85.8 million for 2002, $71.7 million for 2001, and $77.1 million in 2000. Research and development expenses consist primarily of labor, masks, prototype wafers, third-party design automation software and assembly tooling and qualification expenses. The increase in 2002 when compared to 2001 was primarily due to increased headcount and related spending due to our acquisition of Agere FPGA (see note 5 to our Consolidated Financial Statements). The decrease in 2001 when compared to 2000 was attributable to a decrease in discretionary spending which more than offset headcount increases. We believe that a continued commitment to research and development is essential in order to maintain product leadership and provide innovative new product offerings, and therefore we expect to continue to make significant future investments in research and development.

Selling, General and Administrative. Selling, general and administrative expense was $48.1 million in 2002, $53.0 million in 2001, and $81.1 million in 2000. The decrease in 2002 when compared to 2001 was primarily due to reduced revenue and associated reductions in variable costs and reductions in discretionary spending. The decrease in 2001 when compared to 2000 was primarily due to lower variable costs associated with reduced revenue, reductions in discretionary spending and, to a lesser extent, the reversal in the third quarter of 2001 of $2.8 million of reserves established in the Vantis acquisition related to litigation settled in 2001.

In-Process Research and Development. IPR&D consists of those products obtained through acquisition that are not yet proven to be technologically feasible but have been developed to a point where there is value associated with them in relation to potential future revenue. Because technological feasibility was not yet proven and no alternative future uses are believed to exist for the in-process technologies, the assigned value was expensed immediately upon the closing date of the acquisitions. IPR&D recorded in 2002 resulted from the completion of the Agere FPGA and Cerdelinx acquisitions described below:

Agere FPGA

The fair value underlying the $24.2 million assigned to acquired IPR&D in the Agere FPGA acquisition was determined by identifying research projects in areas for which technological feasibility had not been established and there was no alternative future use. Projects in the IPR&D category are the ORCA 4 FPGA family, the next generation FPGA family and the FPSC field-programmable system chips. The following is a brief description of these projects. The ORCA 4 FPGA family project, increasing speed and density and enhancing yields, was approximately 85% complete and estimated to be completed by 2003 at an estimated cost of $1.5 million. This project was completed during 2002 with no material change in cost. The next generation FPGA family project, increasing speed and density while reducing die size, was approximately 50% complete and estimated to be completed by 2004 at an estimated cost of $2 million. There has been no material change in the schedule or estimated cost of this project. The future development of FPSC field-programmable system chips (field-programmable system chips which combine embedded pre-defined logic circuits with an FPGA platform) was approximately 25% to 90% complete, and estimated to be completed by 2004 at an estimated cost of $2 million. There has been no material change in the schedule or estimated cost of this project. The IPR&D value of $24.2 million was determined by an income approach where fair value is the present value of projected free cash flows that will be generated by the products incorporating the acquired technologies under development, assuming they are successfully completed. The estimated net free cash flows generated by the products over 5-7 year periods were discounted at rates ranging from 23 to 25 percent in relation to the stage of completion and the technical risks associated with achieving technological feasibility. The net cash flows for such projects were based on management's estimates of revenue, expenses and asset requirements. Any delays or failures in the completion of these projects could impact our expected return on investment and future results. In addition, our financial condition would be adversely affected if the value of other intangible assets acquired became impaired.

All of these projects have completion risks related to silicon functionality, architecture performance, process technology availability, packaging technology, continued availability of key technical personnel, product reliability and availability of software support. To the extent that estimated completion dates are not met, the risk of competitors' product introductions is greater and revenue opportunity may be permanently lost.

Cerdelinx

The fair value underlying the $5.7 million assigned to acquired IPR&D from the Cerdelinx acquisition was determined by identifying research projects in areas for which technological feasibility had not been established and there were no alternative future uses. The acquired IPR&D consists of low-power CMOS transceivers and backplane interfaces with embedded high-speed SERDES I/O. These products were approximately 60% complete and are estimated to be completed in 2003 at an estimated cost of approximately $2 million. There has been no material change in the schedule or estimated cost of this project.

The fair value was determined by an income approach where fair value is the present value of projected free cash flows that will be generated by the products incorporating the acquired technologies under development, assuming they are successfully completed. The estimated net free cash flows generated by the products over six year periods were discounted at rates ranging from 15 to 17 percent in relation to the stage of completion and the technical risks associated with achieving technological feasibility. The net cash flows for such projects were based on management's estimates of revenue, expenses and asset requirements.

All of these projects have completion risks related to silicon functionality, architecture performance, process technology availability, packaging technology, continued availability of key technical personnel and product reliability. To the extent that estimated completion dates are not met, the risk of competitive product introduction is greater and revenue opportunity may be permanently lost.

Amortization of Intangible Assets. Amortization of intangible assets is related to our 2002 acquisitions, discussed above, our 1999 Vantis acquisition and our 2001 acquisition of Integrated Intellectual Property, Inc. ("I2P"). Amortization expense was $73.4 million in 2002, $84.3 million in 2001, and $81.9 million in 2000. The decrease in amortization for 2002 compared to 2001 was due to the cessation of amortizing goodwill in 2002 (see note 1 to our Consolidated Financial Statements) which more than offset the increased amortization of intangible assets related to our acquisitions of Agere FPGA and Cerdelinx. The increase in amortization for 2001 as compared to 2000 was primarily due to the I2P acquisition.

(Loss) Gain on Foundry Investments. The gain on foundry investments recorded in the first quarter of 2000 and the loss on foundry investments recorded in the third quarter of 2001 represent equity market appreciation and subsequent impairment loss on our UMC common shares. In the September 2001 quarter, the carrying value of the UMC shares was reduced as we recorded a $152.8 million loss representing a decline in the market value of our UMC shares. In each quarter that the market value of the UMC investment is below carrying value, we evaluate whether the investment is other than temporarily impaired. We recorded the unrealized loss on our UMC investment in the September 30, 2001 Statement of Operations. At that time, we believed the investment was other than temporarily impaired for the following reasons:

- it was becoming increasingly likely that the stock price would not recover based on the increasing size of the unrealized loss, the extended time period during which the stock price had continued to decline without a trend reversal, and the dampening volatility, which indicated to us that the stock price was becoming more stable;
- UMC's financial performance had weakened relative to earlier quarters;
- the opinion of many industry observers and analysts regarding the semiconductor downturn had become significantly more negative;
- the events of September 11, 2001 further exacerbated market conditions;
- we had previously believed that UMC would initiate an ADR conversion program that would enable us to sell our shares at a premium on the New York Stock Exchange, but such a program was never initiated; and
- although we still had the intent and ability to hold the shares for an indefinite period, we concluded this fact did not overcome the negative factors associated with the shares.

Interest Income. Interest income was $5.4 million in 2002, $17.7 million in 2001, and $16.2 million in 2000. The decrease in 2002 when compared to 2001 was due to lower invested balances as a result of our acquisition of Agere FPGA (see note 5 to our Consolidated Financial Statements) and lower interest rates on invested balances. The increase in 2001 when compared to 2000 was attributable to overall increased cash balances generated from our follow-on stock offering, completed in July 2000, which more than offset lower interest rates on invested balances in 2001.

Interest Expense. Interest expense was approximately $12.6 million in 2002 and $14.0 million in both 2001 and 2000. Substantially all interest expense resulted from the debt issued to partially fund our Vantis acquisition. The decrease in 2002 when compared to 2001 and 2000 is due to the extinguishment of approximately $51.9 million of our convertible notes during the year (see note 10 to our Consolidated Financial Statements).

Other Income. Other income, net, was $13.4 million in 2002, $0.3 million in 2001 and insignificant in 2000. For 2002, the amount recorded consists primarily of a $9.3 million gain in conjunction with the extinguishment of a portion of our convertible notes (see note 10 to our Consolidated Financial statements), and a $4.0 million gain in conjunction with the sale of a portion of our UMC shares (see note 7 to our Consolidated Financial Statements).

Provision (Benefit) for Income Taxes. The provision for income taxes for 2002 of $81.9 million is primarily the result of a $118.6 million charge to income tax expense recorded in the fourth quarter of 2002, representing a full valuation allowance for our recorded deferred tax assets (see note 9 to our Consolidated Financial Statements). Absent this charge, the benefit for income taxes in 2002 would have resulted in an effective tax rate of (39.0%), as compared to a benefit for income taxes for 2001 resulting in an effective tax rate of (37.0%) and as compared to 35.9% effective tax rate in 2000. The tax benefit in 2002 before recording the valuation allowances and the tax benefit in 2001 is the result of the pretax loss reported in the period. The effective tax rate for 2002, prior to recording the valuation allowances, is higher than the benefit rate for 2001 due to less tax-exempt income resulting from the use of cash for our acquisition of Agere FPGA (see note 5 to our Consolidated Financial Statements) and lower interest rates on the invested balances. The rate associated with the tax benefit in 2001 is higher than the provision rate in 2000 because of the proportional impact of our marginal tax rate applied to the unrealized gain in 2000 and subsequent impairment loss in 2001 related to our foundry investments (see note 7 to our Consolidated Financial Statements) in comparison to taxes on operating income and non-taxable investment income. The effective rates in 2001 and 2000 are lower than the combined federal and state statutory rates primarily because of tax-exempt investment income and tax credits.

Factors Affecting Future Results

A continuing downturn in the communications equipment and computing end markets has caused a reduction in demand for our products and limited our ability to maintain or increase revenue levels and operating results.

A significant portion of our revenue is derived from customers in the communications equipment and computing end markets. A downturn in the overall global economy or in the economies of the countries where we derive significant revenue could lead to a contraction of capital spending on information technology. This in turn could lead to a reduction in the demand for communications or computing equipment and for our products.

Due to a deterioration in overall economic conditions and a significant reduction in information technology capital spending, the communications and computing end markets are currently experiencing significant and prolonged downturns. In addition, the abrupt transition from an environment of rapid growth to the current environment in these end equipment markets resulted in an excess of inventory within our end customers. At present and in the future when these or other similar conditions exist, there is likely to be an adverse effect on our operating results.

The cyclical nature of the semiconductor industry may limit our ability to maintain or increase revenue levels and operating results during current or future industry downturns.

The semiconductor industry is highly cyclical, to a greater extent than other less dynamic or less technology-driven industries. Our financial performance has periodically been negatively affected by downturns in the semiconductor industry. Factors that contribute to these industry downturns include:

- the cyclical nature of the demand for the products of semiconductor customers;
- general reductions in inventory levels by customers;

- excess production capacity;
- general decline in end-user demand; and
- accelerated declines in average selling prices.

Beginning in 2001, the semiconductor industry experienced a significant downturn. At present and in the future when these or other similar conditions exist, there is likely to be an adverse effect on our operating results.

We may experience unexpected difficulties integrating the field programmable gate array, or FPGA, business which we recently purchased from Agere.

On January 18, 2002, we acquired the FPGA business of Agere Systems and are currently in the process of completing the integration of this business with our operations. If our integration is unsuccessful, more difficult or more time consuming than originally planned, we may incur unexpected disruptions to our ongoing business. These disruptions could harm our operating results. Further, the following specific factors may adversely affect our ability to integrate the FPGA business of Agere:

- we may experience unexpected losses of key employees or customers;
- we may not achieve expected levels of revenue growth;
- we may not be able to coordinate our new product and process development in a way which permits us to bring future new products to the market in a timely manner; and
- we may discover unexpected liabilities.

In addition, as part of our acquisition, we entered into agreements with Agere to obtain certain manufacturing support and services and future intellectual property. These support agreements with Agere do not have a material impact upon costs. However, in the event that Agere fails to provide this support and service, or provides such support and service at a level of quality and timeliness inconsistent with the historical delivery of such support and service, our ability to integrate the FPGA business will be hampered and our operating results may be harmed.

We may be unsuccessful in defining, developing or selling new products required to maintain or expand our business.

As a semiconductor company, we operate in a dynamic environment marked by rapid product obsolescence. Our future success depends on our ability to introduce new or improved silicon and software products that meet customer needs while achieving acceptable margins. If we fail to introduce these new products in a timely manner or these products fail to achieve market acceptance, our operating results would be harmed.

The introduction of new silicon and software products in a dynamic market environment presents significant business challenges. Product development commitments and expenditures must be made well in advance of product sales. The market reception of new products depends on accurate projections of long-term customer demand, which by their nature are uncertain.

Our future revenue growth is dependent on market acceptance of our new silicon and software product families and the continued market acceptance of our current products. The success of these products is dependent on a variety of specific technical factors including:

- successful product definition;
- timely and efficient completion of product design;
- timely and efficient implementation of wafer manufacturing and assembly processes;
- product performance; and
- the quality and reliability of the product.

If, due to these or other factors, our new silicon and software products do not achieve market acceptance, our operating results would be harmed.

Our products may not be competitive if we are unsuccessful in migrating our manufacturing processes to more advanced technologies or alternative fabrication facilities.

To develop new products and maintain the competitiveness of existing products, we need to migrate to more advanced wafer manufacturing processes that use larger wafer sizes and smaller device geometries. We also may need to use additional foundries. Because we depend upon foundries to provide their facilities and support for our process technology development, we may experience delays in the availability of advanced wafer manufacturing process technologies at existing or new wafer fabrication facilities. As a result, volume production of our advanced process technologies at the fabs of Seiko Epson, UMC, Chartered Semiconductor or future foundries may not be achieved. This could harm our operating results.

In late 2001, UMC informed us that as part of an overall capacity rationalization they were planning to close certain of their fabrication facilities. We were developing an advanced wafer manufacturing process at one of the UMC fabs that has been closed. With UMC's support, we have transferred this process to another UMC fab. However, as a result, our new product introduction schedules were delayed. This could harm our operating results.

Our marketable securities, which we hold for strategic reasons, are subject to equity price risk and their value may fluctuate.

Currently we hold substantial equity in UMC, which we acquired as part of a strategic investment to obtain certain manufacturing rights. The market price and valuation of these equity shares has fluctuated widely due to market and other conditions over which we have little control. During the year ended December 31, 2001, we recorded a $152.8 million pre-tax impairment loss related to this investment. In the future, UMC shares may continue to experience significant price volatility. In the second quarter of 2002, we sold a portion of our UMC shares, but have otherwise not attempted to reduce or eliminate this equity price risk through hedging or similar techniques and hence substantial, sustained changes in the market price of UMC shares could impact our financial results. To the extent that the market value of our UMC shares experiences a significant decline for an extended period of time, our net income could be reduced.

Our future quarterly operating results may fluctuate and therefore may fail to meet expectations.

Our quarterly operating results have fluctuated and may continue to fluctuate. Consequently, our operating results may fail to meet the expectations of analysts and investors. As a result of industry conditions and the following specific factors, our quarterly operating results are more likely to fluctuate and are more difficult to predict than a typical non-technology company of our size and maturity:

- general economic conditions in the countries where we sell our products;
- conditions within the end markets into which we sell our products;
- the cyclical nature of demand for our customers' products;
- excessive inventory accumulation by our end customers;
- the timing of our and our competitors' new product introductions;
- product obsolescence;
- the scheduling, rescheduling and cancellation of large orders by our customers;
- our ability to develop new process technologies and achieve volume production at the fabs of Seiko Epson, UMC, Chartered Semiconductor or at other foundries;
- changes in manufacturing yields;
- adverse movements in exchange rates, interest rates or tax rates; and
- the availability of adequate supply commitments from our wafer foundries and assembly and test subcontractors.

As a result of these factors, our past financial results are not necessarily a good predictor of our future results.

Our stock price may continue to experience large fluctuations.

In recent years, the price of our common stock has fluctuated greatly. These price fluctuations have been rapid and severe and have left investors little time to react. The price of our common stock may continue to fluctuate greatly in the future due to a variety of company specific factors, including:

- quarter-to-quarter variations in our operating results;
- shortfalls in revenue or earnings from levels expected by securities analysts; and
- announcements of technological innovations or new products by other companies.

Presently, our stock price is trading near our consolidated book value. A sustained decline in our stock price may result in a write-off of goodwill (see note 1 to our Consolidated Financial Statements).

Our wafer supply may be interrupted or reduced, which may result in a shortage of finished products available for sale.

We do not manufacture finished silicon wafers. Currently, substantially all of our silicon wafers are manufactured by Seiko Epson in Japan, UMC in Taiwan, and Chartered Semiconductor in Singapore. If Seiko Epson, through its U.S. affiliate, Epson Electronics America, UMC or Chartered significantly interrupts or reduces our wafer supply, our operating results could be harmed.

In the past, we have experienced delays in obtaining wafers and in securing supply commitments from our foundries. At present, we anticipate that our supply commitments are adequate. However, these existing supply commitments may not be sufficient for us to satisfy customer demand in future periods. Additionally, notwithstanding our supply commitments we may still have difficulty in obtaining wafer deliveries consistent with the supply commitments. We negotiate wafer prices and supply commitments from our suppliers on at least an annual basis. If any of Seiko Epson, Epson Electronics America, UMC or Chartered Semiconductor were to reduce its supply commitment or increase its wafer prices, and we cannot find alternative sources of wafer supply, our operating results could be harmed.

Many other factors that could disrupt our wafer supply are beyond our control. Since worldwide manufacturing capacity for silicon wafers is limited and inelastic, we could be harmed by significant industry-wide increases in overall wafer demand or interruptions in wafer supply. Additionally, a future disruption of Seiko Epson's, UMC's or Chartered Semiconductor's foundry operations as a result of a fire, earthquake or other natural disaster could disrupt our wafer supply and could harm our operating results.

If our foundry partners experience quality or yield problems, we may face a shortage of finished products available for sale.

We depend on our foundries to deliver reliable silicon wafers with acceptable yields in a timely manner. As is common in our industry, we have experienced wafer yield problems and delivery delays. If our foundries are unable for a prolonged period to produce silicon wafers that meet our specifications, with acceptable yields, our operating results could be harmed.

The majority of our revenue is derived from products based on a specialized silicon wafer manufacturing process technology called E^2CMOS®. The reliable manufacture of high performance E^2CMOS semiconductor wafers is a complicated and technically demanding process requiring:

- a high degree of technical skill;
- state-of-the-art equipment;
- the absence of defects in the masks used to print circuits on a wafer;
- the elimination of minute impurities and errors in each step of the fabrication process; and
- effective cooperation between us and the wafer supplier.

As a result, our foundries may experience difficulties in achieving acceptable quality and yield levels when manufacturing our silicon wafers.

If our assembly and test subcontractors experience quality or yield problems, we may face a shortage of finished products available for sale.

We rely on subcontractors to assemble and test our devices with acceptable quality and yield levels. As is common in our industry, we have experienced quality and yield problems in the past. If we experience prolonged quality or yield problems in the future, our operating results could be harmed.

The majority of our revenue is derived from semiconductor devices assembled in advanced packages. The assembly of advanced packages is a complex process requiring:

- a high degree of technical skill;
- state-of-the-art equipment;
- the absence of defects in lead frames used to attach semiconductor devices to the package;
- the elimination of raw material impurities and errors in each step of the process; and
- effective cooperation between us and the assembly subcontractor.

As a result, our subcontractors may experience difficulties in achieving acceptable quality and yield levels when assembling and testing our semiconductor devices.

Deterioration of conditions in Asia may disrupt our existing supply arrangements and result in a shortage of finished products available for sale.

All three of our major silicon wafer suppliers operate fabs located in Asia. Our finished silicon wafers are assembled and tested by independent subcontractors located in China, Malaysia, the Philippines, South Korea and Taiwan. A prolonged interruption in our supply from any of these subcontractors could harm our operating results.

Economic, financial, social and political conditions in Asia have historically been volatile. Financial difficulties, governmental actions or restrictions, prolonged work stoppages or any other difficulties experienced by our suppliers may disrupt our supply and could harm our operating results.

Our wafer purchases from Seiko Epson are denominated in Japanese yen. The value of the dollar with respect to the yen fluctuates. Substantial deterioration of dollar-yen exchange rates could harm our operating results.

Export sales account for a substantial portion of our revenues and may decline in the future due to economic and governmental uncertainties.

Our export sales are affected by unique risks frequently associated with foreign economies including:

- changes in local economic conditions;
- exchange rate volatility;
- governmental controls and trade restrictions;
- export license requirements and restrictions on the export of technology;
- political instability or terrorism;
- changes in tax rates, tariffs or freight rates;
- interruptions in air transportation; and
- difficulties in staffing and managing foreign sales offices.

For example, our export sales have historically been affected by regional economic crises. Significant changes in the economic climate in the foreign countries where we derive our export sales could harm our operating results.

We may not be able to successfully compete in the highly competitive semiconductor industry.

The semiconductor industry is intensely competitive and many of our direct and indirect competitors have substantially greater financial, technological, manufacturing, marketing and sales resources. If we are unable to compete successfully in this environment, our future results will be adversely affected.

The current level of competition in the programmable logic market is high and may increase in the future. We currently compete directly with companies that have licensed our technology or have developed similar products. We also compete indirectly with numerous semiconductor companies that offer products and solutions based on alternative technologies. These direct and indirect competitors are established multinational semiconductor companies as well as emerging companies. We also may experience significant competition from foreign companies in the future.

We may fail to retain or attract the specialized technical and management personnel required to successfully operate our business.

To a greater degree than most non-technology companies or larger technology companies, our future success depends on our ability to attract and retain highly qualified technical and management personnel. As a mid-sized company, we are particularly dependent on a relatively small group of key employees. Competition for skilled technical and management employees is intense within our industry. As a result, we may not be able to retain our existing key technical and management personnel. In addition, we may not be able to attract additional qualified employees in the future. If we are unable to retain existing key employees or are unable to hire new qualified employees, our operating results could be adversely affected.

If we are unable to adequately protect our intellectual property rights, our financial results and competitive position may suffer.

Our success depends in part on our proprietary technology. However, we may fail to adequately protect this technology. As a result, we may lose our competitive position or face significant expense to protect or enforce our intellectual property rights.

We intend to continue to protect our proprietary technology through patents, copyrights and trade secrets. Despite this intention, we may not be successful in achieving adequate protection. Claims allowed on any of our patents may not be sufficiently broad to protect our technology. Patents issued to us also may be challenged, invalidated or circumvented. Finally, our competitors may develop similar technology independently.

Companies in the semiconductor industry vigorously pursue their intellectual property rights. If we become involved in protracted intellectual property disputes or litigation we may utilize substantial financial and management resources, which could have an adverse effect on our operating results.

Our industry is characterized by frequent claims regarding patents and other intellectual property rights of others. We have been, and from time-to-time expect to be, notified of claims that we are infringing the intellectual property rights of others. If any third party makes a valid claim against us, we could face significant liability and could be required to make material changes to our products and processes. In response to any claims of infringement, we may seek licenses under patents that we are alleged to be infringing. However, we may not be able to obtain a license on favorable terms or without our operating results being adversely affected.

Critical Accounting Policies

Critical Accounting Policies are those "that are both most important to the portrayal of a company's financial condition and results and require management's most difficult, subjective and complex judgements, often as a result of the need to make estimates about the effect of matters that are inherently uncertain." A description of our critical accounting policies follows.

Use of Estimates. The preparation of financial statements in conformity with generally accepted accounting principles requires management to make estimates and assumptions that affect the reported amounts of assets, such as accounts receivable, inventory and deferred income taxes and liabilities, such as accrued liabilities, income taxes and deferred income, disclosure of contingent assets and liabilities at the date of the financial statements and the reported amounts of revenues and expenses during the fiscal periods presented. Actual results could differ from those estimates.

Revenue recognition. Revenue from direct customers is recognized upon shipment provided that persuasive evidence of a sales arrangement exists, the price is fixed, title has transferred, collection of resulting receivables is probable, there are no customer acceptance requirements and no remaining significant obligations. Certain of our sales are made to distributors under agreements providing price protection and right of return on unsold merchandise. Revenue and costs relating to such distributor sales are deferred until the product is sold by the distributor and related revenue and costs are then reflected in income.

Deferred income. In determining the amount of deferred income related to sales to distributors, we make estimates regarding sales prices and margins to be earned by our distributors upon sales to our end customers.

Inventory. We value inventory at the lower of cost or market on a quarterly basis. In addition, we write down unproven, excess and obsolete inventories to net realizable value. To value our inventory, we make a number of estimates and assumptions including future price declines and forecasted demand for our products.

Long-Lived Assets. We account for our long-lived assets, primarily Property and equipment and amortizable Intangible assets, in accordance with Statement of Financial Accounting Standards No. 144 (SFAS 144), "Accounting for the Disposal of Long-Lived Assets," which requires us to review the impairment of long-lived assets whenever events or changes in circumstances indicate that the carrying amount of an asset may not be recoverable. Impairment is measured by comparing the estimated undiscounted cash flows to the carrying amount. A loss is recorded if the carrying amount of the asset exceeds the estimated undiscounted cash flows. Intangible assets are generally being amortized over five years, and fifteen years for income tax purposes, on a straight-line basis.

Accounting for income taxes. To report income tax expense related to operating results, we record current and deferred income tax assets and liabilities in our balance sheet. In determining the value of our deferred tax assets, we make estimates of future taxable income. As of December 31, 2002, we have recorded full valuation allowances for all of our deferred tax assets due to uncertainties regarding their realization.

New Accounting Pronouncements

In June 2001, the FASB issued SFAS 142, which supersedes APB Opinion No. 17, "Intangible Assets." SFAS 142, among other things, establishes new standards for intangible assets acquired in a business combination, eliminates amortization of goodwill and sets forth requirements to periodically evaluate goodwill for impairment. We adopted this statement during the first quarter of 2002 and thus goodwill and certain intangibles with indefinite lives are no longer being amortized. Accordingly, approximately $8 million of previous quarterly amortization is no longer being recorded. To apply SFAS 142, a company is divided into separate "reporting units," each representing groups of products that are separately managed. For this purpose, we have one reporting unit. To determine whether or not goodwill may be impaired, a test is required comparing the book value of the "reporting unit" to its trading price. Similar tests are required in the future, at least annually, and more often where there is a change in circumstances that could result in an impairment of goodwill. If the trading price of our common stock is below the book value for a sustained period, a goodwill impairment test will be performed by comparing book value to estimated market value (trading price plus a control premium). The excess of book value over estimated market value will then be subtracted from the goodwill account with a resulting charge to operations. Subsequent unrealized recoveries in market value, if any, will not be recorded. We completed an initial goodwill impairment assessment as of January 1, 2002 to determine if a transition impairment charge should be recognized under SFAS 142. Upon assessment, no transition impairment charge was recorded. We also completed our annual goodwill impairment assessment in December 2002, upon which no impairment charge was recorded.

The following table presents the impact of SFAS 142 on our net income and our net income per share had the new standard been in effect for the years ended December 31, 2001 and 2000:

	YEAR ENDED DEC. 31, 2001	YEAR ENDED DEC. 31, 2000
	(In thousands, except per share amounts)	
Net (loss) income -as reported	$ (109,519)	$167,887
Adjustments:		
Amortization of goodwill	32,949	30,997
Income tax effect	(12,206)	(11,140)
Net adjustments	20,743	19,857
Net (loss) income — as adjusted	$ (88,776)	$187,744
Basic net (loss) income per share — as reported	$ (1.01)	$ 1.65
Basic net (loss) income per share — adjusted	$ (.82)	$ 1.85
Diluted net (loss) income per share — as reported	$ (1.01)	$ 1.47
Diluted net (loss) income per share — adjusted	$ (.82)	$ 1.64

The following tables present details of the Company's total purchased intangible assets:

DECEMBER 31, 2002	GROSS	ACCUMULATED AMORTIZATION	NET
		(In millions)	
Current technology	$273.6	$(160.3)	$113.3
Core technology	7.3	(.5)	6.8
Licenses	10.2	(1.4)	8.8
Non-compete agreements	14.2	(4.4)	9.8
Workforce	4.7	(.3)	4.4
Backlog	1.4	(1.4)	—
Customer list	17.4	(12.3)	5.1
Patents and trademarks	26.8	(19.0)	7.8
Total	$355.6	$(199.6)	$156.0

DECEMBER 31, 2001	GROSS	ACCUMULATED AMORTIZATION	NET
		(In millions)	
Current technology	$210.2	$(106.8)	$103.4
Customer list	17.4	(8.9)	8.5
Patents and trademarks	26.8	(13.6)	13.2
Total	$254.4	$(129.3)	$125.1

The estimated future amortization expense of purchased intangible assets as of December 31, 2002 is as follows:

FISCAL YEAR:	AMOUNT (In millions)
2003	$ 71.4
2004	43.8
2005	14.4
2006	10.8
2007	9.8
Later years	5.8
	$156.0

The estimated future amortization expense of deferred stock compensation attributable to Research and Development activities as of December 31, 2002 is approximately $4.2 million annually for 2003 and 2004, and $3.1 million for 2005.

In October 2001, the FASB issued SFAS 144, "Accounting for the Disposal of Long-Lived Assets," which supersedes SFAS 121, "Accounting for the Impairment Of Long-Lived Assets and for Long-Lived Assets to be Disposed of." SFAS 144 retains the fundamental provisions of SFAS 121 regarding the recognition and measurement of the impairment of long-lived assets to be held and used and the measurement of long-lived assets to be disposed of by sale, but provides additional definition and measurement criteria for determining when an impairment has occurred. Goodwill and financial instruments are excluded from the scope of SFAS 144, however amortizable intangible assets fall within its scope. The adoption of this statement in the first quarter of 2002 did not have a material impact on our results of operations, financial position or cash flows.

In May 2002, the FASB issued SFAS 145, "Rescission of FAS Nos. 4, 44, and 64, Amendment of FAS 13, and Technical Corrections." Among other things, SFAS 145 rescinds various pronouncements regarding early extinguishment of debt and allows extraordinary accounting treatment for early extinguishment only when the provisions of Accounting Principles Board Opinion No. 30, "Reporting the Results of Operations — Reporting the Effects of Disposal of a Segment of a Business, and Extraordinary, Unusual and Infrequently Occurring Events and Transactions" are met. SFAS 145 provisions regarding early extinguishment of debt are generally effective for fiscal years beginning after May 15, 2002. Management adopted this pronouncement during the second quarter of 2002.

During 2002, we extinguished approximately $51.9 million face value of our 4¾% convertible notes for approximately $42.8 million in cash, including accrued interest. We recognized a gain of approximately $9.3 million in connection with these transactions (see note 10). As specified in SFAS 145, this gain was recorded in "Other income, net" in the accompanying Consolidated Statement of Operations.

In July 2002, the FASB issued SFAS 146, "Accounting for Costs Associated with Exit or Disposal Activities." SFAS 146 requires that a liability for a cost associated with an exit or disposal activity be recognized when the liability is incurred. SFAS 146 eliminates the definition and requirement for recognition of exit costs in Emerging Issues Task Force (EITF) Issue No. 94-3 where a liability for an exit cost was recognized at the date of an entity's commitment to an exit plan. This statement is effective for exit or disposal activities initiated after December 31, 2002. We do not believe that the adoption of this statement will have a material impact on our results of operations, financial position or cash flows.

In December 2002, the FASB issued SFAS 148, "Accounting for Stock-Based Compensation — Transition and Disclosure." This statement provides alternative methods of transition for a voluntary change to the fair value method of accounting for stock-based employee compensation. In addition, it amends the disclosure requirements of SFAS 123 to require prominent disclosure in both annual and interim financial statements about the method of accounting for stock-based employee compensation and the effect of the method used on reporting results. This statement is generally effective for fiscal years ending after December 15, 2002 and for the interim periods beginning after December 15, 2002. As we continue to report stock-based employee compensation costs using the intrinsic value method as defined by APB 25, adoption of the provisions of the new statement affects only our disclosure of these costs, which is presented in note 1 to our Consolidated Financial Statements.

Liquidity and Capital Resources

As of December 31, 2002, our principal source of liquidity was $276.9 million of cash and short-term investments, a $254.7 million decrease from the balance of $531.6 million at December 31, 2001. Working capital decreased to $348.8 million at December 31, 2002 from $629.2 million at December 31, 2001. These decreases were primarily due to cash used for the acquisition of Agere FPGA (see note 5 to our Consolidated Financial Statements). During 2002, we generated approximately $46.0 million of cash and cash equivalents from our operations compared with $7.0 million during 2001. This increase in cash generation was driven primarily by refunds of federal income taxes previously paid due to net losses in 2001 and 2002.

Accounts receivable at December 31, 2002 increased by $6.9 million, or 36%, as compared to the balance of the prior year. This increase was primarily due to increased revenue levels in the fourth quarter of 2002 as compared to the fourth quarter of 2001 and the timing of receipts. Inventories decreased by $8.7 million, or 13%, as compared to the balance of the prior year primarily due to reduced starts and receipts of wafers in response to lower revenue levels. Prepaid expenses and other current assets decreased by approximately $5.7 million, or 14%, as compared to the balance of the prior year. This decrease is due primarily to a decrease in refundable income taxes. Current deferred tax assets decreased by approximately $31.6 million, or 100%, as compared to the balance of the prior year. This decrease was due to the recognition of a 100% valuation allowance on our deferred tax assets in accordance with SFAS 109 (see note 9 to our Consolidated Financial Statements). Foundry investments, advances and other assets decreased by approximately $57.9 million, or 36% as compared to the balance of the prior year. During 2002, we recorded a $36.1 million unrealized loss ($24.9 million net of tax and reflected in Accumulated Other Comprehensive Income), reflecting the decline in market value of our UMC shares since December 31, 2001. Additionally, during 2002, we sold approximately 7.6 million of our UMC shares at a gain of $4.0 million (see note 7 to our Consolidated Financial Statements). Net intangible assets increased by $30.9 million, or 25% as compared to the balance of the prior year. This increase was primarily due to approximately $88.8 million of intangible assets recorded in conjunction with the acquisition of Agere FPGA (see note 5 to our Consolidated Financial Statements) and approximately $12.2 million of intangible assets recorded in conjunction with the acquisition of Cerdelinx (see note 4 to our Consolidated Financial Statements), offset by amortization of approximately $70.4 million. Goodwill increased by approximately $142.1 million, or 175%, at December 31, 2002, as compared to the balance of the prior year. This increase is due to goodwill recorded in conjunction with the acquisition of Agere FPGA (see note 5 to our Consolidated Financial Statements). Non-current deferred tax assets, net, decreased by approximately $65.6 million, or 100%, as compared to the balance of the prior year. This decrease was due to the recognition of a 100% valuation allowance for our deferred tax assets in accordance with SFAS 109 (see note 9 to our Consolidated Financial Statements). Deferred income at December 31, 2002 decreased by $6.1 million, or 34%, as compared to the balance of the prior year, due to reductions in distributors' inventories associated with decreased shipments and lower revenue levels.

On October 28, 1999, we issued $260 million in 4 3/4 % convertible subordinated notes due on November 1, 2006. These notes require that we pay interest semi-annually on May 1 and November 1. Holders of these notes may convert them into shares of our common stock at any time on or before November 1, 2006, at a conversion price of $20.72 per share, subject to adjustment in certain events. Beginning on November 6, 2002 and ending on October 31, 2003, we may redeem the notes in whole or in part at a redemption price of 102.71% of the principal amount. In the subsequent three twelve-month periods, the redemption price declines to 102.04%, 101.36% and 100.68% of principal, respectively. The notes are subordinated in right of payment to all of our senior indebtedness, and are subordinated to all liabilities of our subsidiaries. The balance of these convertible notes as of December 31, 2002 decreased by $51.9 million as compared to the balance at December 31, 2001, as during 2002 we extinguished this amount of notes with a corresponding gain of approximately $9.3 million (see note 10 to our Consolidated Financial Statements). During the first quarter of 2003, we have extinguished an additional $32.8 million of our convertible subordinated notes for approximately $29.9 million in cash, resulting in a gain of approximately $2.9 million. We may continue to extinguish further portions of our convertible subordinated notes subject to availability, pricing, market conditions and other factors.

At December 31, 2002, we had no senior indebtedness and our subsidiaries had $2.5 million of other liabilities. Issuance costs relative to the convertible subordinated notes are included in Other assets and aggregated approximately $6.9 million and are being amortized to expense over the life of the notes. Accumulated amortization amounted to approximately $5.3 million at December 31, 2002.

We do not have any financial partnerships with unconsolidated entities, such as entities often referred to as structured finance or special purpose entities, which are often established for the purpose of facilitating off-balance sheet arrangements or other contractually narrow or limited purposes. Accordingly, we are not exposed to any financing, liquidity, market or credit risk that could arise if we had such relationships.

Capital expenditures were approximately $17.5 million, $13.8 million and $25.9 million for 2002, 2001 and 2000, respectively. We expect to spend approximately $15 million to $20 million for the fiscal year ending December 31, 2003.

Certain of our facilities and equipment are leased under operating leases, which expire at various times through 2009. Rental expense under the operating leases was approximately $5,972,000, $5,078,000 and $5,469,000 for 2002, 2001, and 2000, respectively. Future minimum lease commitments (before consideration of sublease receipts discussed below) at December 31, 2002 are as follows (in thousands):

YEAR	AMOUNT
2003	$ 8,897
2004	8,751
2005	7,925
2006	7,905
2007	5,444
Later years	6,087
	$45,009

Included in these amounts are certain properties which are currently subleased. A portion of this sublease income is payable to the property owner. Future minimum sublease receipts, based on agreements in place at December 31, 2002, net of such payments are as follows (in thousands):

YEAR	AMOUNT
2003	$ 2,473
2004	2,555
2005	2,622
2006	886
	$ 8,536

We currently own approximately 88.2 million shares of UMC common stock. Restrictions by UMC and the Taiwan government apply to approximately 26% of these shares. During 2002, we sold approximately 7.6 million of our UMC shares for approximately $9.9 million in cash, resulting in a gain of $4.0 million (see note 7 to our Consolidated Financial Statements). In the future, we may or may not choose to liquidate additional UMC shares.

In December 2000, our Board of Directors authorized management to repurchase up to five million shares of our common stock. As of December 31, 2002, we had repurchased 1,136,000 shares (596,000 in 2001) at an aggregate cost of approximately $20.0 million ($10.6 million in 2001). There were no repurchases of common stock in 2002.

In March 1997 and as subsequently amended in January 2002, we entered into an advance payment production agreement with Seiko Epson and Epson Electronics America, Inc. (“EEA”) under which we agreed to advance up to approximately $69 million, payable upon completion of specific milestones, to Seiko Epson to finance construction of an eight-inch sub-micron semiconductor wafer manufacturing facility. Under the terms of the agreement, the advance is to be repaid with semiconductor wafers over a multi-year period. No interest income is recorded. The agreement calls for wafers to be supplied by Seiko Epson through EEA pursuant to purchase agreements with EEA. Payments of approximately $51.3 million have been made under this agreement. Cumulatively, approximately $13.3 million of these payments have been repaid to us in the form of semiconductor wafers. Approximately $2.4 million of the outstanding advances are expected to be repaid with semiconductor wafers during fiscal year 2002 and are thus reflected as part of Prepaid expenses and other current assets in our Consolidated Balance Sheet. We do not anticipate making additional payments under this agreement.

We believe that our existing liquid resources, expected cash generated from operations and existing credit facilities combined with our ability to borrow additional funds will be adequate to meet our operating and capital requirements and obligations for the next 12 months, including the extinguishment of a portion of our convertible subordinated notes discussed above.

We may in the future seek new or additional sources of funding. In addition, in order to secure additional wafer supply, we may from time to time consider various financial arrangements including joint ventures, equity investments, advance purchase payments, loans, or similar arrangements with independent wafer manufacturers in exchange for committed wafer capacity. To the extent that we pursue any such additional financing arrangements, additional debt or equity financing may be required. There can be no assurance that such additional financing will be available when needed or, if available, will be on favorable terms. Any future equity financing will decrease existing stockholders' equity percentage ownership and may, depending on the price at which the equity is sold, result in dilution.

Item 7(a). Quantitative and Qualitative Disclosures About Market Risk

As of December 31, 2002 and December 31, 2001 our investment portfolio consisted of fixed income securities of $274.4 million and $508.2 million, respectively. As with all fixed income instruments, these securities are subject to interest rate risk and will decline in value if market interest rates increase. If market rates were to increase immediately and uniformly by 10% from levels as of December 31, 2002 and December 31, 2001, the decline in the fair value of our portfolio would not be material. Further, we have the ability to hold our fixed income investments until maturity and, therefore, we would not expect to recognize such an adverse impact in our income or cash flows.

We have international subsidiary and branch operations. Additionally, a portion of our silicon wafer purchases are denominated in Japanese yen. We therefore are subject to foreign currency rate exposure. To mitigate rate exposure with respect to our yen-denominated wafer purchases, we maintain a yen-denominated bank account and bill our Japanese customers in yen. If the foreign currency rates were to fluctuate by 10% from rates at December 31, 2002 and December 31, 2001, the effect on our consolidated financial statements would not be material. However, there can be no assurance that there will not be a material impact in the future.

We are exposed to equity price risk due to our equity investment in UMC (see note 7 to our Consolidated Financial Statements). Neither a 10% increase nor a further 10% decrease in equity price related to this investment would have a material effect on our consolidated financial statements. We have not attempted to reduce or eliminate this equity price risk through hedging or similar techniques. As a result, sustained changes in the market price of UMC shares could impact our financial results. To the extent that the market value of our UMC shares experiences further deterioration for an extended period of time, our net income could be reduced.

Item 8. Financial Statements and Supplementary Data

Index to Consolidated Financial Statements and Consolidated Financial Statement Schedules

CONSOLIDATED BALANCE SHEET

(In thousands, except share and par value amounts)

	DECEMBER 31, 2002	DECEMBER 31, 2001
ASSETS		
Current assets:		
Cash and cash equivalents	$169,475	$ 250,203
Short-term investments	107,405	281,363
Accounts receivable, net	26,374	19,452
Inventories (note 2)	56,241	64,926
Prepaid expenses and other current assets (note 9)	35,033	40,749
Deferred income taxes (note 9)	—	31,591
Total current assets	394,528	688,284
Foundry investments, advances and other assets (note 7)	104,507	162,418
Property and equipment, less accumulated depreciation (note 3)	62,786	63,222
Intangible assets, less accumulated amortization of $199,647 and $129,311 (notes 4, 5 and 6)	155,953	125,081
Goodwill (notes 5 and 6)	223,489	81,387
Deferred income taxes (note 9)	—	65,590
	$941,263	$1,185,982
LIABILITIES AND STOCKHOLDERS' EQUITY		
Current liabilities:		
Accounts payable and accrued expenses	$ 18,860	$ 20,201
Accrued payroll obligations	14,737	18,054
Income taxes payable (note 9)	142	2,751
Deferred income	11,983	18,103
Total current liabilities	45,722	59,109
4¾% Convertible notes due in 2006 (notes 10 and 16)	208,061	260,000
Other long-term liabilities	26,345	27,103
Commitments and contingencies (notes 7, 8, 12 and 13)	—	—
Stockholders' equity (note 11):		
Preferred stock, $.01 par value, 10,000,000 shares authorized; none issued and outstanding	—	—
Common stock, $.01 par value, 300,000,000 shares authorized; 112,358,043 and 109,428,061 shares issued and outstanding	1,124	1,094
Paid-in capital	580,987	548,053
Deferred stock compensation	(11,540)	(2,739)
Other comprehensive (loss) income	(4,631)	22,932
Retained earnings	95,195	270,430
	661,135	839,770
	$941,263	$1,185,982

The accompanying notes are an integral part of this statement

CONSOLIDATED STATEMENT OF OPERATIONS

(In thousands, except per share data)

	YEAR ENDED DECEMBER 31, 2002	YEAR ENDED DECEMBER 31, 2001	YEAR ENDED DECEMBER 31, 2000
Revenue (note 15)	$ 229,126	$ 295,326	$567,759
Costs and expenses:			
Cost of products sold	91,546	111,498	217,830
Research and development	85,776	71,679	77,057
Selling, general and administrative (note 14)	48,099	53,027	81,082
In-process research and development (notes 4 and 5)	29,853	—	—
Amortization of intangible assets[1] (notes 4, 5 and 6)	73,415	84,349	81,873
	328,689	320,553	457,842
(Loss) income from operations	(99,563)	(25,227)	109,917
Other income (expense), net:			
Interest income	5,362	17,733	16,202
Interest expense (note 10)	(12,611)	(13,962)	(14,036)
(Loss) gain on foundry investments (note 7)	—	(152,795)	149,960
Other income, net (notes 7 and 10)	13,443	285	28
	6,194	(148,739)	152,154
(Loss) income before (benefit) provision for income taxes	(93,369)	(173,966)	262,071
Provision (benefit) for income taxes (note 9)	81,866	(64,447)	94,184
Net (loss) income	$(175,235)	$(109,519)	$167,887
Basic net (loss) income per share	$ (1.59)	$ (1.01)	$ 1.65
Diluted net (loss) income per share	$ (1.59)	$ (1.01)	$ 1.47
Shares used in per share calculations:			
Basic	110,193	108,814	101,716
Diluted	110,193	108,814	120,321

[1] Includes $2,962 and $397 of amortization of deferred stock compensation expense for the years ended December 31, 2002 and December 31, 2001, respectively attributable to Research and Development activities.

The accompanying notes are an integral part of this statement

CONSOLIDATED STATEMENT OF CHANGES IN STOCKHOLDERS' EQUITY

(In thousands, except par value)

	COMMON STOCK ($.01 PAR VALUE) SHARES	COMMON STOCK ($.01 PAR VALUE) AMOUNT	PAID-IN CAPITAL	DEFERRED STOCK COMPENSATION	ACCUMULATED OTHER COMPREHENSIVE (LOSS) INCOME	RETAINED EARNINGS	TOTAL
Balances, Dec. 31, 1999	96,571	$ 966	$269,745	$ —	$ —	$ 212,062	$ 482,773
Common stock issued	11,502	114	237,266	—	—	—	237,380
Repurchase of common stock	(540)	(5)	(9,375)	—	—	—	(9,380)
Tax benefit of option exercises	—	—	24,856	—	—	—	24,856
Unrealized loss on foundry investments (net of tax of $30.0 million — note 7)	—	—	—	—	(47,861)	—	—
Net income for 2000	—	—	—	—	—	167,887	—
Total comprehensive income	—	—	—	—	—	—	120,026
Balances, Dec. 31, 2000	107,533	1,075	522,492	—	(47,861)	379,949	855,655
Common stock issued	2,491	25	20,491	—	—	—	20,516
Repurchase of common stock	(596)	(6)	(10,608)	—	—	—	(10,614)
Tax benefit of option exercises	—	—	12,542	—	—	—	12,542
Recognized loss on foundry investments	—	—	—	—	47,861	—	—
Unrealized gain on foundry investments (net of tax of $13.3 million — note 7)	—	—	—	—	24,106	—	—
Deferred stock compensation	—	—	3,136	(3,136)	—	—	—
Amortization of deferred stock compensation	—	—	—	397	—	—	397
Translation adjustments	—	—	—	—	(1,174)	—	—
Net loss for 2001	—	—	—	—	—	(109,519)	—
Total comprehensive loss	—	—	—	—	—	—	(38,726)
Balances, Dec. 31, 2001	109,428	1,094	548,053	(2,739)	22,932	270,430	839,770
Common stock issued	2,930	30	20,287	—	—	—	20,317
Tax benefit of option exercises	—	—	884	—	—	—	884
Unrealized loss on foundry investments (note 7)	—	—	—	—	(24,878)	—	—
Recognized gain on sale of foundry investments previously unrealized (note 7)	—	—	—	—	(3,398)	—	—
Deferred stock compensation	—	—	11,763	(11,763)	—	—	—
Amortization of deferred stock compensation	—	—	—	2,962	—	—	2,962
Translation adjustments	—	—	—	—	713	—	—
Net loss for 2002	—	—	—	—	—	(175,235)	—
Total comprehensive loss	—	—	—	—	—	—	(202,798)
Balances, Dec. 31, 2002	112,358	$1,124	$580,987	$(11,540)	$ (4,631)	$ 95,195	$ 661,135

The accompanying notes are an integral part of this statement

CONSOLIDATED STATEMENT OF CASH FLOWS

(In thousands)

	YEAR ENDED DECEMBER 31, 2002	YEAR ENDED DECEMBER 31, 2001	YEAR ENDED DECEMBER 31, 2000
Cash flow from operating activities:			
Net (loss) income	$ (175,235)	$(109,519)	$167,887
Adjustments to reconcile net (loss) income to net cash provided by operating activities:			
Depreciation and amortization	94,375	106,539	102,213
(Gain) loss on value of foundry investments	(4,017)	152,795	(149,960)
Gain on extinguishment of convertible notes	(9,341)	—	—
Tax benefit of option exercises	884	12,542	24,856
In process research and development	29,853	—	—
Changes in assets and liabilities (net of purchase accounting adjustments):			
Accounts receivable	(6,922)	30,236	(16,012)
Inventories	12,157	(5,433)	(33,457)
Prepaid expenses and other current assets	4,730	(7,327)	(2,842)
Deferred income taxes	110,792	(55,369)	15,092
Foundry investments, advances and other assets	3,562	(11,478)	(359)
Accounts payable and accrued expenses	(3,497)	(53,959)	(10,515)
Accrued payroll obligations	(2,099)	(4,822)	3,970
Income taxes payable	(2,609)	(6,733)	(2,975)
Deferred income	(6,120)	(40,081)	12,996
Other liabilities	(515)	(424)	3,371
Net cash provided by operating activities	45,998	6,967	114,265
Cash flow from investing activities:			
Proceeds from short-term investments	306,923	336,973	299,370
Purchase of short-term investments	(132,965)	(318,828)	(498,562)
Acquisition of Agere FPGA	(254,232)	(2,233)	—
Other acquisition costs	(2,530)	—	—
(Decrease) increase in intangible assets	—	(5,189)	4,886
Proceeds from sale of equity securities	9,930	—	—
Capital expenditures	(17,451)	(13,751)	(25,883)
Net cash used by investing activities	(90,325)	(3,028)	(220,189)
Cash flow from financing activities:			
Extinguishment of convertible notes	(42,077)	—	—
Repurchase of common stock	—	(10,614)	(9,380)
Net proceeds from issuance of common stock	5,676	20,978	237,380
Net cash (used) provided by financing activities	(36,401)	10,364	228,000
Net (decrease) increase in cash and cash equivalents	(80,728)	14,303	122,076
Beginning cash and cash equivalents	250,203	235,900	113,824
Ending cash and cash equivalents	$ 169,475	$ 250,203	$ 235,900
Supplemental disclosure of non-cash investing and financing activities:			
Unrealized (loss) gain on (depreciation) appreciation of foundry investments included in other comprehensive (loss) income	$ (24,878)	$ 24,106	$ (47,861)
Stock and options issued in conjunction with acquisition of Cerdelinx	$ 21,703	$ —	$ —

The accompanying notes are an integral part of this statement

Note 1. Nature of Operations and Significant Accounting Policies:

Nature of Operations

Lattice Semiconductor Corporation designs, develops and markets high performance programmable logic devices, or PLDs, and related software. Programmable logic devices are widely-used semiconductor components that can be configured by the end customer as specific logic circuits, and enable the end customer to shorten design cycle times and reduce development costs. Our end customers are primarily original equipment manufacturers in communications, computing, industrial, automotive, medical, consumer and military end markets.

Fiscal Reporting Period

We report based on a 52 or 53 week year ending on the Saturday closest to December 31. For ease of presentation, we have adopted the convention of using March 31, June 30, September 30 and December 31 as period end dates for all financial statement captions.

Principles of Consolidation

On August 26, 2002, we completed the stock for stock acquisition of Cerdelinx Technologies, Inc. ("Cerdelinx") for 2.6 million shares valued at $8.30 per share. This transaction was accounted for as an asset purchase, and accordingly, the results of operations for Cerdelinx and estimated fair value of assets acquired and liabilities assumed are included in our consolidated financial statements beginning August 26, 2002. This acquisition is discussed further in note 4.

On January 18, 2002, we completed the acquisition of the field-programmable gate array ("FPGA") business ("Agere FPGA") of Agere Systems Inc. ("Agere") for $250 million in cash. This transaction was accounted for as a purchase, and accordingly, the results of operations for Agere FPGA and estimated fair value of assets acquired and liabilities assumed are included in our consolidated financial statements beginning January 18, 2002. This acquisition is discussed further in note 5.

On June 15, 1999, we completed the acquisition of all of the outstanding capital stock of Vantis Corporation ("Vantis") from Advanced Micro Devices, Inc. ("AMD"). The transaction was accounted for as a purchase, and accordingly, the results of operations of Vantis and estimated fair value of assets acquired and liabilities assumed are included in our consolidated financial statements beginning June 16, 1999. This acquisition is discussed further in note 6.

The accompanying consolidated financial statements include the accounts of Lattice Semiconductor Corporation and its subsidiaries, all wholly-owned, after the elimination of all significant intercompany balances and transactions.

Cash Equivalents and Short-Term Investments

We consider all highly liquid investments, which are readily convertible into cash and have original maturities of three months or less, to be cash equivalents. Short-term investments, which are relatively less liquid and have maturities of less than one year, were composed of corporate auction preferred stocks ($43.2 million and $160.0 million), municipal and local government obligations ($64.2 million and $102.1 million) and time deposits ($0 and $19.2 million) at December 31, 2002 and December 31, 2001, respectively.

We account for our short-term investments as held-to-maturity, and state them at amortized cost with corresponding premiums or discounts amortized over the life of the investment as interest income. Amortized cost approximated fair value at December 31, 2002.

Financial Instruments

The carrying value of our financial instruments approximates fair value. We estimate the fair value of cash and cash equivalents, short-term investments, accounts receivable, other current assets and current liabilities based upon existing interest rates related to such assets and liabilities compared to the current market rates of interest for instruments of similar nature and degree of risk.

Derivative Financial Instruments

As of December 31, 2002, 2001 and 2000 and for the years then ended, we had no outstanding derivatives, including foreign exchange contracts for the purchase or sale of foreign currencies. We do not enter into derivative financial instruments for trading purposes.

Note 1. Nature of Operations and Significant Accounting Policies (continued):

Foreign Exchange and Translation of Foreign Currencies

A portion of our silicon wafer purchases are denominated in Japanese yen. We maintain a yen-denominated bank account and bill our Japanese customers in yen. Gains or losses from foreign exchange rate fluctuations on unhedged balances denominated in foreign currencies are reflected in Other income. Realized and unrealized gains or losses were not significant for the years presented. We translate accounts denominated in foreign currencies in accordance with SFAS 52, "Foreign Currency Translation." Translation adjustments related to the consolidation of foreign subsidiary financial statements are reflected in other comprehensive (loss) income in Stockholders' Equity.

Concentrations of Credit Risk

Financial instruments which potentially expose us to concentrations of credit risk consist primarily of short-term investments and trade receivables. We place our investments through several financial institutions and mitigate the concentration of credit risk by placing percentage limits on the maximum portion of the investment portfolio which may be invested in any one investment instrument. Investments consist primarily of A1 and P1 or better rated U.S. commercial paper, U.S. government agency obligations and other money market instruments, "AA" or better rated municipal obligations, money market preferred stocks and other time deposits. Concentrations of credit risk with respect to trade receivables are mitigated by a geographically diverse customer base and our credit and collection process. Accounts receivable are shown net of allowances for doubtful accounts of $1,074,000 and $1,475,000 at December 31, 2002 and 2001, respectively. We perform credit evaluations for all customers and secure transactions with letters of credit or advance payments where necessary. Write-offs for uncollected trade receivables have not been significant to date.

Revenue Recognition

Revenue from sales to OEM customers is recognized upon shipment provided that persuasive evidence of an arrangement exists, the price is fixed, title has transferred, collection of resulting receivables is probable, there are no customer acceptance requirements and no remaining significant obligations. Certain of our sales are made to distributors under agreements providing price protection and right of return on unsold merchandise. Revenue and cost relating to such distributor sales are deferred until the product is sold by the distributor and related revenue and costs are then reflected in income. Revenue from software sales was not material for the years presented.

Inventories

Inventories are stated at the lower of first-in, first-out cost or market.

Long-Lived Assets

We account for our long-lived assets, primarily Property and equipment and amortizable Intangible assets, in accordance with Statement of Financial Accounting Standards No. 144 (SFAS 144), "Accounting for the Disposal of Long-Lived Assets," which requires us to review the impairment of long-lived assets whenever events or changes in circumstances indicate that the carrying amount of an asset may not be recoverable. Impairment is measured by comparing the estimated undiscounted cash flows to the carrying amount. A loss is recorded if the carrying amount of the asset exceeds the estimated undiscounted cash flows. Intangible assets are generally being amortized over five years, and fifteen years for income tax purposes, on a straight-line basis.

Property and Equipment

Property and equipment are stated at cost. Depreciation is computed using the straight-line method for financial reporting purposes over the estimated useful lives of the related assets, generally three to five years for equipment and software and thirty years for buildings. Accelerated methods of computing depreciation are generally used for income tax purposes.

Note 1. Nature of Operations and Significant Accounting Policies (continued):

Goodwill

We assess the initial carrying value of Goodwill recorded in connection with our acquisitions (see notes 5 and 6) by comparing our aggregate purchase price to the fair value of the net tangible assets and intangible assets acquired. We measure the initial carrying value for potential impairment in accordance with SFAS No.142, "Goodwill and Other Intangible Assets." To apply SFAS 142, a company is divided into separate "reporting units," each representing groups of products that are separately managed. For this purpose, we have one reporting unit. To determine whether or not goodwill may be impaired, a test is required comparing the book value of the "reporting unit" to its trading price. Similar tests are required in the future, at least annually, and more often where there is a change in circumstances that could result in an impairment of goodwill. If the trading price of our common stock is below book value for a sustained period, a goodwill impairment test will be performed by comparing book value to estimated market value (trading price plus a control premium). The excess of book value over estimated market value will then be subtracted from the goodwill account with a resulting charge to operations. Subsequent unrealized recoveries in market value, if any, will not be recorded. We completed an initial goodwill impairment assessment as of January 1, 2002 to determine if a transition impairment charge should be recognized under SFAS 142. Upon assessment, no transition impairment charge was recorded. We also completed our annual goodwill impairment assessment in December 2002, upon which no impairment charge was recorded.

Research and Development

Research and development costs are expensed as incurred.

Stock-Based Compensation

We account for our employee and director stock options and employee stock purchase plan in accordance with provisions of Accounting Principles Board Opinion No. 25 ("APB 25"), "Accounting for Stock Issued to Employees." Pro forma disclosures as required under SFAS 123, "Accounting for Stock-Based Compensation," and as amended by SFAS 148, "Accounting for Stock-Based Compensation — Transition and Disclosure," are presented below (also see note 11). Pursuant to FASB Interpretation No. 44 "Accounting for Certain Transactions Involving Stock Based Compensation — an interpretation of APB Opinion No. 25," effective July 1, 2000, the "in the money" portion of stock options granted to employees in connection with acquisitions is accounted for as Deferred stock compensation in Stockholders' Equity and amortized to operations as part of Amortization of Intangible Assets over the vesting periods of the options.

Our pro forma information is as follows (in thousands, except per share data):

	YEAR ENDED DEC. 31, 2002	YEAR ENDED DEC. 31, 2001	YEAR ENDED DEC. 31, 2000
Net (loss) income, as reported	$(175,235)	$(109,519)	$167,887
Deduct: Total stock-based employee compensation expense determined under fair value based method for all awards, net of related tax effects	(31,106)	(22,614)	(20,003)
Pro forma net (loss) income	$(206,341)	$(132,133)	$147,884
Earnings per share:			
Basic — as reported	$ (1.59)	$ (1.01)	$ 1.65
Basic — pro forma	$ (1.87)	$ (1.22)	$ 1.46
Diluted — as reported	$ (1.59)	$ (1.01)	$ 1.47
Diluted — pro forma	$ (1.87)	$ (1.22)	$ 1.31

Note 1. Nature of Operations and Significant Accounting Policies (continued):

Net (Loss) Income Per Share

Net (loss) income per share is computed based on the weighted average number of shares of common stock and potentially dilutive securities assumed to be outstanding during the period using the treasury stock method. Potentially dilutive securities consist of stock options, warrants to purchase common stock and convertible subordinated notes. The most significant difference between basic and diluted net income per share is that basic net income per share does not treat potentially dilutive securities such as convertible subordinated notes, options and warrants as outstanding. For 2000, diluted weighted-average shares outstanding include the effect of stock options, warrants and approximately 12.5 million shares issuable on the assumed conversion of our convertible subordinated notes (see note 10). For 2000, diluted net income per share is adjusted to exclude interest expense and debt issuance cost amortization (net of tax) of approximately $8.3 million and $1.2 million, respectively. Diluted loss per common share for 2002 and 2001 is based only on the weighted-average number of common shares outstanding during these periods, as the inclusion of options, warrants and convertible subordinated notes would have been antidilutive. A reconciliation of the numerators and denominators of basic and diluted net income per share is presented below:

	YEAR ENDED DEC. 31, 2002	YEAR ENDED DEC. 31, 2001	YEAR ENDED DEC. 31, 2000
	(in thousands, except per share data)		
Basic and diluted net (loss) income	$(175,235)	$(109,519)	$167,887
Shares used in basic net (loss) income per share calculations	110,193	108,814	101,716
Dilutive effect of stock options, warrants and convertible subordinated notes	—	—	18,605
Shares used in diluted net income per share calculations	110,193	108,814	120,321
Basic net (loss) income per share	$ (1.59)	$ (1.01)	$ 1.65
Diluted net (loss) income per share	$ (1.59)	$ (1.01)	$ 1.47

On August 31, 2000 our Board of Directors approved a two-for-one stock split of our common stock to be effected in the form of a stock dividend of one share of common stock for each share of our outstanding common stock. This dividend was paid on October 11, 2000 to shareholders of record on September 20, 2000. All share and per share amounts presented in the accompanying consolidated financial statements and notes thereto have been adjusted retroactively to reflect this two-for-one split.

In July 2000, we completed a follow-on public stock offering, consisting of 8,000,000 shares of our common stock at a price of $27.44 per share. Our net proceeds were approximately $210 million after deducting underwriting discounts and offering expenses.

Comprehensive (Loss) Income

For 2000, comprehensive income consists primarily of net income of $167.9 million and an unrealized loss on depreciation of foundry investments (net of tax) of approximately $47.9 million. For 2001, comprehensive loss consists primarily of net loss of $109.5 million offset by unrealized gain recorded related to the market value of our foundry investments (net of tax) of approximately $72.0 million. For 2002, comprehensive loss consists primarily of net loss of $175.2 million, unrealized loss on depreciation of our foundry investments of approximately $24.9 million and recognized gain on sale of foundry investments previously unrealized of approximately $3.4 million (see note 7).

Statement of Cash Flows

During 2002, we received income tax refunds, net of payments, of approximately $37.2 million. Income taxes paid approximated $7.3 million and $55.9 million in 2001 and 2000, respectively. Interest paid aggregated approximately $12.0 million, $12.4 million and $12.3 million in 2002, 2001, and 2000, respectively.

Note 1. Nature of Operations and Significant Accounting Policies (continued):

Use of Estimates

The preparation of financial statements in conformity with generally accepted accounting principles requires management to make estimates and assumptions that affect the reported amounts of assets, such as accounts receivable, inventory and deferred income taxes and liabilities, such as accrued liabilities, income taxes and deferred income, disclosure of contingent assets and liabilities at the date of the financial statements and the reported amounts of revenues and expenses during the fiscal periods presented. Actual results could differ from those estimates.

New Accounting Pronouncements

In June 2001, the FASB issued SFAS 142, "Goodwill and Other Intangible Assets," which supersedes APB Opinion No. 17, "Intangible Assets." SFAS 142, among other things, establishes new standards for intangible assets acquired in a business combination, eliminates amortization of goodwill and sets forth requirements to periodically evaluate goodwill for impairment. We adopted this statement during the first quarter of 2002 and thus goodwill and certain intangibles with indefinite lives are no longer being amortized. Accordingly, approximately $8 million of previous quarterly amortization is no longer being recorded (see *Goodwill* in this note 1 above).

The following table presents the impact of SFAS 142 on our net income and our net income per share had the new standard been in effect for the years ended December 31, 2001 and 2000:

	YEAR ENDED DEC. 31, 2001	YEAR ENDED DEC. 31, 2000
	(In thousands, except per share amounts)	
Net (loss) income -as reported	$(109,519)	$167,887
Adjustments:		
Amortization of goodwill	32,949	30,997
Income tax effect	(12,206)	(11,140)
Net adjustments	20,743	19,857
Net (loss) income — as adjusted	$ (88,776)	$187,744
Basic net (loss) income per share — as reported	$ (1.01)	$ 1.65
Basic net (loss) income per share — adjusted	$ (.82)	$ 1.85
Diluted net (loss) income per share — as reported	$ (1.01)	$ 1.47
Diluted net (loss) income per share — adjusted	$ (.82)	$ 1.64

The following tables present details of the Company's total purchased intangible assets (in millions):

DECEMBER 31, 2002	GROSS	ACCUMULATED AMORTIZATION	NET
Current technology	$273.6	$(160.3)	$113.3
Core technology	7.3	(.5)	6.8
Licenses	10.2	(1.4)	8.8
Non-compete agreements	14.2	(4.4)	9.8
Workforce	4.7	(.3)	4.4
Backlog	1.4	(1.4)	—
Customer list	17.4	(12.3)	5.1
Patents and trademarks	26.8	(19.0)	7.8
Total	$355.6	$(199.6)	$156.0

DECEMBER 31, 2001	GROSS	ACCUMULATED AMORTIZATION	NET
Current technology	$210.2	$(106.8)	$103.4
Customer list	17.4	(8.9)	8.5
Patents and trademarks	26.8	(13.6)	13.2
Total	$254.4	$(129.3)	$125.1

Note 1. Nature of Operations and Significant Accounting Policies (continued):

The estimated future amortization expense of purchased intangible assets as of December 31, 2002 is as follows:

FISCAL YEAR:	AMOUNT (In millions)
2003	$ 71.4
2004	43.8
2005	14.4
2006	10.8
2007	9.8
Later years	5.8
	$156.0

The estimated future amortization expense of deferred stock compensation attributable to Research and Development activities as of December 31, 2002 is approximately $4.2 million annually for 2003 and 2004, and $3.1 million for 2005.

In October 2001, the FASB issued SFAS 144, "Accounting for the Disposal of Long-Lived Assets," which supersedes SFAS 121, "Accounting for the Impairment Of Long-Lived Assets and for Long-Lived Assets to be Disposed of." SFAS 144 retains the fundamental provisions of SFAS 121 regarding the recognition and measurement of the impairment of long-lived assets to be held and used and the measurement of long-lived assets to be disposed of by sale, but provides additional definition and measurement criteria for determining when an impairment has occurred. Goodwill and financial instruments are excluded from the scope of SFAS 144, however amortizable intangible assets fall within its scope. The adoption of this statement in the first quarter of 2002 did not have a material impact on our results of operations, financial position or cash flows.

In May 2002, the FASB issued SFAS 145, "Rescission of FAS Nos. 4, 44, and 64, Amendment of FAS 13, and Technical Corrections." Among other things, SFAS 145 rescinds various pronouncements regarding early extinguishment of debt and allows extraordinary accounting treatment for early extinguishment only when the provisions of Accounting Principles Board Opinion No. 30, "Reporting the Results of Operations — Reporting the Effects of Disposal of a Segment of a Business, and Extraordinary, Unusual and Infrequently Occurring Events and Transactions," are met. SFAS 145 provisions regarding early extinguishment of debt are generally effective for fiscal years beginning after May 15, 2002. Management adopted this pronouncement during the second quarter of 2002.

During 2002, we extinguished approximately $51.9 million face value of our 4¾% convertible notes for approximately $42.8 million in cash, including accrued interest. We recognized a gain of approximately $9.3 million in connection with these transactions (see note 10). As specified in SFAS 145, this gain was recorded in "Other income, net" in the accompanying Consolidated Statement of Operations.

In July 2002, the FASB issued SFAS 146, "Accounting for Costs Associated with Exit or Disposal Activities." SFAS 146 requires that a liability for a cost associated with an exit or disposal activity be recognized when the liability is incurred. SFAS 146 eliminates the definition and requirement for recognition of exit costs in Emerging Issues Task Force (EITF) Issue No. 94-3, "Liability Recognition for Certain Employee Termination Benefits and Other Costs to Exit an Activity (including Certain Costs Incurred in a Restructuring)," where a liability for an exit cost was recognized at the date of an entity's commitment to an exit plan. This statement is effective for exit or disposal activities initiated after December 31, 2002. We do not believe that the adoption of this statement will have a material impact on our results of operations, financial position or cash flows.

In December 2002, the FASB issued SFAS 148, "Accounting for Stock-Based Compensation — Transition and Disclosure." This statement provides alternative methods of transition for a voluntary change to the fair value method of accounting for stock-based employee compensation. In addition, it amends the disclosure requirements of SFAS 123 to require prominent disclosure in both annual and interim financial statements about the method of accounting for stock-based employee compensation and the effect of the method used on reporting results. This statement is generally effective for fiscal years ending after December 15, 2002 and for the interim periods beginning after December 15, 2002. As we continue to report stock-based employee compensation costs using the intrinsic value method as defined by APB 25, adoption of the provisions of the new statement affects only our disclosure of these costs, which is presented in note 1.

Financial presentation

Certain reclassifications of prior year balances included in our consolidated financial statements have been made to conform to the 2002 presentation.

Note 2. Inventories:

	DECEMBER 31, 2002	DECEMBER 31, 2001
	(In thousands)	
Work in progress	$ 40,515	$ 44,460
Finished goods	15,726	20,466
	$ 56,241	$ 64,926

Note 3. Property and Equipment:

	DECEMBER 31, 2002	DECEMBER 31, 2001
	(In thousands)	
Land	$ 2,099	$ 2,099
Construction in progress	3,024	—
Buildings	24,703	24,703
Computer and test equipment	123,115	109,606
Office furniture and equipment	10,379	9,452
Leasehold and building improvements	13,833	13,513
	177,153	159,373
Accumulated depreciation and amortization	(114,367)	(96,151)
	$ 62,786	$ 63,222

Depreciation expense was approximately $19.2 million, $19.1 million and $17.1 million for 2002, 2001 and 2000, respectively.

Note 4. Acquisition of Cerdelinx:

On August 26, 2002, we completed the stock for stock acquisition of Cerdelinx for 2.6 million shares valued at $8.30 per share. Cerdelinx was an early stage fabless semiconductor company focused on the design of application specific standard products targeted towards emerging high-speed communications and storage applications. Cerdelinx had a team of engineers who were developing a portfolio of low-power CMOS transceivers and backplane interfaces with embedded high-speed SERDES I/O to support 10 gigabit-per-second applications. The acquisition serves to enhance our silicon development efforts and our ability to deliver leading-edge programmable solutions within the communications and storage market segments. This acquisition principally comprises intellectual property and a work force. The core technology portion of the intellectual property is valued using a royalty savings methodology which discounts estimated royalties that would be paid on an after tax basis. The in-process technology portion of the intellectual property is valued using a discounted cash flow methodology described in detail below. Work force is valued using a replacement cost methodology which discounts costs to an after tax amount. The transaction was completed pursuant to an Agreement and Plan of Reorganization entered into on July 15, 2002, as amended on July 24, 2002, among Lattice, Cerdelinx and affiliated parties. The components of the purchase price were as follows (in millions):

Stock issued and liabilities assumed	$ 22.8
Estimated direct acquisition costs	1.1
Total	$ 23.9

Note 4. Acquisition of Cerdelinx (continued):

In conformity with Financial Accounting Standard SFAS 142, the total purchase price was allocated to the estimated fair value of assets acquired and liabilities assumed. As Cerdelinx was not considered a business under SFAS 141, "Business Combinations," no goodwill was recognized. In estimating the fair value of the assets acquired, management considered various factors, including an appraisal. The purchase price allocation is subject to further refinement and change over the four quarters subsequent to the acquisition. We are in the process of completing our integration of Cerdelinx and accordingly, the amounts recorded are based on our current estimates of these costs. The total purchase price was allocated as follows (in millions):

Core technology	$ 7.2
Deferred stock compensation	5.8
In process research and development costs	5.7
Work force	4.7
Liabilities assumed	(1.2)
Equipment	1.1
Non compete agreement	0.3
Cash	0.3
Total	$ 23.9

There were no significant exit costs incurred or accrued in connection with this transaction. Management does not expect intangible assets acquired to be deductible for income tax purposes.

Employees who joined Lattice as a result of this acquisition held Cerdelinx shares and options which were converted into 0.9 million Lattice shares and options which were either unvested or otherwise restricted from sale over terms up to four years at a grant price from $0.41 per share to $2.54 per share. The spread, which is the difference between grant price and market value of our common stock on the Closing Date, aggregating $5.8 million on these shares and options, was recorded as Paid-in capital and Deferred stock compensation and is being amortized to operations equally over the vesting (or restriction lapsing) period as part of Amortization of intangible assets.

In-Process Research and Development ("IPR&D")

IPR&D consists of those products obtained through acquisition that are not yet proven to be technologically feasible but have been developed to a point where there is value associated with them in relation to potential future revenue. Because technological feasibility was not yet proven and no alternative future uses are believed to exist for the in-process technologies, the assigned value was expensed immediately after the closing of the acquisition.

The fair value underlying the $5.7 million assigned to acquired IPR&D from the Cerdelinx acquisition was determined by identifying research projects in areas for which technological feasibility had not been established and there were no alternative future uses. The acquired IPR&D consists of low-power CMOS transceivers and backplane interfaces with embedded high-speed SERDES I/O. These products were approximately 60% complete and are estimated to be completed in 2003 at an estimated cost of approximately $2 million. There has been no material change in the schedule or estimated cost of this project.

The fair value was determined by an income approach where fair value is the present value of projected free cash flows that will be generated by the products incorporating the acquired technologies under development, assuming they are successfully completed. The estimated net free cash flows generated by the products over six year periods were discounted at rates ranging from 15 to 17 percent in relation to the stage of completion and the technical risks associated with achieving technological feasibility. The net cash flows for such projects were based on management's estimates of revenue, expenses and asset requirements.

All of these projects have completion risks related to silicon functionality, architecture performance, process technology availability, packaging technology, continued availability of key technical personnel and product reliability. To the extent that estimated completion dates are not met, the risk of competitive product introduction is greater and revenue opportunity may be permanently lost.

The core technology included in the acquisition of Cerdelinx has an estimated weighted average useful life of approximately six years, and the work force and non-compete agreements included in the Cerdelinx acquisition have estimated useful lives of approximately four years resulting in a weighted average useful life of approximately five years.

Note 5. Acquisition of Agere FPGA:

On January 18, 2002, we completed the acquisition of Agere FPGA for $250 million in cash. This acquisition increased our share of the PLD market, accelerated our entry into the FPGA portion of the market and provided us with additional technical employees and intellectual property. This acquisition principally comprises intellectual property, which was valued using a discounted cash flow methodology of which goodwill was a by-product. The transaction was completed pursuant to an Asset Purchase Agreement dated as of December 7, 2001 between Lattice and Agere. The components of the purchase price were as follows (in millions):

Cash	$ 250.0
Estimated direct acquisition costs	6.3
Total	$ 256.3

In accordance with SFAS 141, the total purchase price was allocated to the estimated fair value of assets acquired and liabilities assumed. In estimating the fair value of the assets acquired, management considered various factors, including an appraisal. We are in the process of completing our integration of Agere FPGA, and accordingly, the amounts recorded are based on our current estimates of these costs. The total purchase price was allocated as follows (in millions):

Excess of purchase price over net assets acquired	$ 142.4
Current technology	63.4
In-process research and development	24.2
Fair value of non-compete agreement	13.8
Licensed technology	10.2
Inventory	3.5
Backlog	1.4
Property, plant and equipment	0.2
Accrued liabilities	(2.8)
Total	$ 256.3

There were no significant exit costs incurred or accrued in connection with this transaction. Management expects the costs of this acquisition, including goodwill, to be deductible for income tax purposes.

Employees joining us from Agere during the first quarter of 2002 were awarded approximately 1.1 million stock options which vest equally over four years at a grant price of $14.76 per share. The difference between grant price and market value of our common stock on the grant date, aggregating approximately $7.0 million, was recorded as Paid-in capital and Deferred stock compensation and is being amortized to operations ratably over the vesting period as part of Amortization of intangible assets.

In-Process Research and Development ("IPR&D")

IPR&D consists of those products obtained through acquisition that are not yet proven to be technologically feasible but have been developed to a point where there is value associated with them in relation to potential future revenue. Because technological feasibility was not yet proven and no alternative future uses are believed to exist for the in-process technologies, the assigned value was expensed immediately upon the closing date of the acquisition.

The fair value underlying the $24.2 million assigned to acquired IPR&D in the Agere FPGA acquisition was determined by identifying research projects in areas for which technological feasibility had not been established and there was no alternative future use. Projects in the IPR&D category are the ORCA 4 FPGA family, the next generation FPGA family and the FPSC field-programmable system chips. The following is a brief description of these projects. The ORCA 4 FPGA family project, increasing speed and density and enhancing yields, was approximately 85% complete and estimated to be completed by 2003 at an estimated cost of $1.5 million. This project was completed during 2002 with no material change in cost. The next generation FPGA family project, increasing speed and density while reducing die size, was approximately 50% complete and estimated to be completed by 2004 at an estimated cost of $2 million. There has been no material change in the schedule or estimated cost of this project. The future development of FPSC field-programmable system chips (field-programmable system chips which combine embedded pre-defined logic circuits with an FPGA platform) was approximately 25% to 90% complete, and estimated to be completed by 2004 at an estimated cost

Note 5. Acquisition of Agere FPGA (continued):

of $2 million. There has been no material change in the schedule or estimated cost of this project. The IPR&D value of $24.2 million was determined by an income approach where fair value is the present value of projected free cash flows that will be generated by the products incorporating the acquired technologies under development, assuming they are successfully completed. The estimated net free cash flows generated by the products over 5-7 year periods were discounted at rates ranging from 23 to 25 percent in relation to the stage of completion and the technical risks associated with achieving technological feasibility. The net cash flows for such projects were based on management's estimates of revenue, expenses and asset requirements. Any delays or failures in the completion of these projects could impact our expected return on investment and future results. In addition, our financial condition would be adversely affected if the value of other intangible assets acquired became impaired.

All of these projects have completion risks related to silicon functionality, architecture performance, process technology availability, packaging technology, continued availability of key technical personnel, product reliability and availability of software support. To the extent that estimated completion dates are not met, the risk of competitors' product introductions is greater and revenue opportunity may be permanently lost.

The non-compete agreement from Agere and the current and licensed technology included in the acquisition of Agere FPGA have an estimated weighted average useful life of approximately 6.3 years. In accordance with SFAS 142, the excess of purchase price over net assets acquired, or Goodwill, is subject to an impairment test at least annually and is not amortized.

Pro forma results

The following pro forma results of operations information are provided for illustrative purposes only and do not purport to be indicative of the consolidated results of operations for future periods or that actually would have been realized had Lattice and Agere FPGA been a consolidated entity during the periods presented. The pro forma results combine the results of operations as if Agere FPGA had been acquired as of the beginning of the periods presented. The results include the impact of certain adjustments such as intangible asset amortization, estimated changes in interest income (expense) related to cash outlays associated with the transaction and income tax benefits related to the aforementioned adjustments. Additionally, the IPR&D charge of $24.2 million discussed above has been excluded from the periods presented due to its non-recurring nature.

	YEAR ENDED	
	DEC. 31, 2002	DEC. 31, 2001
	(in thousands, except per share amounts) (unaudited)	
Revenue	$ 234,518	$ 364,426
Net Loss	$(159,707)	$(122,419)
Basic net loss per share	$ (1.45)	$ (1.13)
Diluted net loss per share	$ (1.45)	$ (1.13)

Note 6. Acquisition of Vantis:

On June 15, 1999, we paid approximately $500.1 million in cash to AMD for all of the outstanding capital stock of Vantis Corporation. The total purchase price of Vantis was $583.1 million, including certain direct acquisition costs, the accrual of certain exit costs and the assumption of certain liabilities related to the Vantis business. Of this purchase price, approximately $422.6 million was allocated to goodwill and intangible assets.

The recorded balances of goodwill and intangible assets, net of accumulated amortization, related to the Vantis acquisition approximated $77.1 million and $ 74.2 million, respectively, at December 31, 2002 and $77.3 million and $125.1 million, respectively, at December 31, 2001. Amortization expense related to these assets approximated $50.9 million, $80.9 million and $81.9 million for 2002, 2001 and 2000, respectively. The decrease in amortization expense for 2002 was due to the elimination of goodwill amortization beginning in 2002 (see note 1).

Note 7. Foundry Investments, Advances and Other Assets:

	DECEMBER 31,	
	2002	2001
	(In thousands)	
Foundry investments and other assets	$ 68,990	$124,870
Wafer supply advances	35,517	37,548
	$104,507	$162,418

In 1995, we entered into a series of agreements with United Microelectronics Corporation ("UMC"), a public Taiwanese company, pursuant to which we agreed to join UMC and several other companies to form a separate Taiwanese corporation, ("UICC"), for the purpose of building and operating an advanced semiconductor manufacturing facility in Taiwan, Republic of China. Under the terms of the agreements, we invested approximately $49.7 million for an approximate 10% equity interest in the corporation and the right to receive a percentage of the facility's wafer production at market prices.

In 1996, we entered into an agreement with Utek Corporation ("Utek"), a public Taiwanese company in the wafer foundry business that became affiliated with the UMC group in 1998, pursuant to which we agreed to make a series of equity investments in Utek under specific terms. In exchange for these investments, we received the right to purchase a percentage of Utek's wafer production. Under this agreement, we invested approximately $17.5 million. On January 3, 2000, UICC and Utek merged into UMC.

We own approximately 88.2 million shares of UMC common stock at December 31, 2002 of which approximately 23.3 million are restricted from sale for more than one year by the terms of our agreement with UMC. Under the terms of the UMC agreement, if we sell any of these restricted shares, our rights to guaranteed wafer capacity at UMC may be reduced on a pro-rata basis based on the number of shares that we sell. If we sell over 10.1 million of these restricted shares, we may lose all of our rights to guaranteed wafer capacity at UMC.

For financial reporting purposes, all of our UMC shares are accounted for as available for sale and marked to market in our Consolidated Balance Sheet until they are sold, at which time a gain or loss is recognized in our Consolidated Statement of Operations. Unrealized gains and losses are included in Accumulated other comprehensive (loss) income within Stockholders' Equity. An other than temporary impairment of UMC share value could result in a reduction of the Consolidated Balance Sheet carrying value and would result in a charge to our Consolidated Statement of Operations.

As a result of the merger discussed above, during the first quarter of 2000, we recognized a $150.0 million gain ($92.1 million after-tax) in income representing the equity market appreciation of our foundry investment in UICC and Utek. During 2000, we subsequently recorded unrealized gains and losses related to this investment due to changes in the market value of our unrestricted UMC shares, to equity as Accumulated other comprehensive (loss) income. These unrealized losses in 2000 totaled $77.9 million ($47.9 million net of tax).

In the September 2001 quarter, the carrying value of the UMC shares was reduced as we recorded a $152.8 million loss representing a decline in the market value of our UMC shares. In each quarter that the market value of the UMC investment is below carrying value, we evaluate whether the investment is other than temporarily impaired. We recorded the unrealized loss on our UMC investment in the September 30, 2001 Statement of Operations. At that time, we believed the investment was other than temporarily impaired for the following reasons:

- it was becoming increasingly likely that the stock price would not recover based on the increasing size of the unrealized loss, the extended time period during which the stock price had continued to decline without a trend reversal, and the dampening volatility, which indicated to us that the stock price was becoming more stable;
- UMC's financial performance had weakened relative to earlier quarters;
- the opinion of many industry observers and analysts regarding the semiconductor downturn had become significantly more negative;
- the events of September 11, 2001 further exacerbated market conditions;

Note 7. Foundry Investments, Advances and Other Assets (continued):

- we had previously believed that UMC would initiate an ADR conversion program that would enable us to sell our shares at a premium on the New York Stock Exchange, but such a program was never initiated; and
- although we still had the intent and ability to hold the shares for an indefinite period, we concluded this fact did not overcome the negative factors associated with the shares.

The carrying value of our investment in UMC was approximately $103.1 million at December 31, 2001. During 2002, we recorded a $36.1 million unrealized loss ($24.9 million net of tax and reflected in Accumulated other comprehensive (loss) income) related to changes in the market value of our unrestricted UMC shares. In connection with the sale of certain UMC shares discussed below, approximately $3.4 million of previously unrealized gain (net of tax) on these shares was realized. During 2002, we sold approximately 7.6 million of our UMC shares for approximately $9.9 million cash. The resultant $4.0 million pre-tax gain associated with these sales was recorded in "Other income, net" in the accompanying Consolidated Statement of Operations and represents the difference between market value on the date of sale and the carrying value at September 30, 2001. The resultant carrying value of our UMC shares was approximately $56.3 million at December 31, 2002 and this balance is classified as part of Foundry investments, advances and other assets. If we liquidate our UMC shares, it is likely that the amount of any future realized gain or loss will be different from the accounting gain or loss reported in prior periods.

In March 1997 and as subsequently amended in January 2002, we entered into an advance payment production agreement with Seiko Epson and Epson Electronics America, Inc. ("EEA") under which we agreed to advance up to $69 million, payable upon completion of specific milestones, to Seiko Epson to finance construction of an eight-inch sub-micron semiconductor wafer manufacturing facility. Under the terms of the agreement, the advance is to be repaid with semiconductor wafers over a multi-year period. No interest income is recorded. The agreement calls for wafers to be supplied by Seiko Epson through EEA pursuant to purchase agreements with EEA. Payments of approximately $51.3 million have been made under this agreement. Cumulatively, approximately $13.3 million of these payments have been repaid to us in the form of semiconductor wafers. Approximately $2.4 million of the outstanding advances are expected to be repaid with semiconductor wafers during 2003 and are thus reflected as part of Prepaid expenses and other current assets in our accompanying Consolidated Balance Sheet. We do not anticipate making additional payments under this agreement.

Note 8. Lease Obligations:

Certain of our facilities and equipment are leased under operating leases, which expire at various times through 2009. Rental expense under the operating leases was approximately $5,972,000, $5,078,000 and $5,469,000 for 2002, 2001, and 2000, respectively. Future minimum lease commitments (before consideration of sublease receipts discussed below) at December 31, 2002 are as follows (in thousands):

YEAR	
2003	$ 8,897
2004	8,751
2005	7,925
2006	7,905
2007	5,444
Later years	6,087
	$ 45,009

Note 8. Lease Obligations (continued):

Included in these amounts are certain properties which are currently subleased. A portion of this sublease income is payable to the property owner. Future minimum sublease receipts, based on agreements in place at December 31, 2002, net of such payments are as follows (in thousands):

YEAR	
2003	$ 2,473
2004	2,555
2005	2,622
2006	886
	$ 8,536

Note 9. Income Taxes:

The components of the provision (benefit) for income taxes for 2002, 2001, and 2000 are presented in the following table

	DEC. 31, 2002	DEC. 31, 2001	DEC. 31, 2000
	(In thousands)		
Current:			
Federal	$ (27,082)	$ (7,018)	$68,791
State	—	(2,087)	8,414
	(27,082)	(9,105)	77,205
Deferred:			
Federal	99,334	(47,482)	14,925
State	9,614	(7,860)	2,054
	108,948	(55,342)	16,979
	$ 81,866	$(64,447)	$94,184

Foreign income taxes were not significant for the years presented.

The provision (benefit) for income taxes differs from the amount of income tax determined by applying the applicable U.S. statutory federal income tax rate to pretax income as a result of the following differences:

	YEAR ENDED DEC. 31, 2002	YEAR ENDED DEC. 31, 2001	YEAR ENDED DEC. 31, 2000
	(In thousands)		
Computed income tax (benefit) expense at the statutory rate	$ (32,679)	$(60,886)	$91,725
Adjustments for tax effects of:			
State taxes, net	(4,016)	(6,466)	6,805
Research and development credits	(800)	(1,175)	(808)
Nontaxable investment items	(1,388)	4,177	(3,976)
Valuation allowance	118,648	—	—
Other	2,101	(97)	438
	$ 81,866	$(64,447)	$94,184

In the fourth quarter of 2002, we recorded a $118.6 million charge to income tax expense, representing a valuation allowance on our recorded deferred tax assets, in accordance with SFAS 109, “Accounting for Income Taxes.” SFAS 109 provides for the recognition of deferred tax assets if realization of these assets is more likely than not. We have provided a valuation allowance equal to our net deferred tax assets due to uncertainties regarding their realization.

Note 9. Income Taxes (continued):

The components of our net deferred tax assets are as follows:

	DECEMBER 31, 2002	DECEMBER 31, 2001
	(In thousands)	
Current deferred tax assets:		
Deferred income	$ 4,434	$ 5,929
Expenses and allowances not currently deductible	15,931	25,662
	20,365	31,591
Less: valuation allowance	(20,365)	—
	$ —	$ 31,591
Non-current deferred tax assets:		
Intangible asset charges not currently deductible	$ 82,686	$ 70,011
Expenses and allowances not currently deductible	7,673	5,576
Net operating loss and credit carryforwards	11,658	—
Other	3,613	3,333
	105,630	78,920
Less: valuation allowance	(105,630)	—
Total deferred tax assets	—	78,920
Non-current deferred tax liabilities:		
Tax effect on net unrealized gain on market value of foundry investments	—	(13,330)
Net non-current deferred tax assets	$ —	$ 65,590

Valuation allowances approximating $7.3 million were provided earlier in 2002 for deferred tax assets acquired with Cerdelinx as discussed below and for certain net operating loss and state credit carryforwards.

In conjunction with the $150.0 million pre-tax gain on our foundry investments as discussed in note 7, we recorded a deferred tax liability of approximately $57.9 million. This deferred tax liability was adjusted for subsequent realized and unrealized gains and losses related to these investments during 2001 and 2002. The December 31, 2001 balance for the deferred tax liability related to our foundry investments, aggregating approximately $13.3 million, was netted against non-current deferred tax assets as summarized above. Deferred taxes related to our foundry investments at December 31, 2002 were not significant.

As of December 31, 2002 and 2001, respectively, we had approximately $26.0 million and $30.0 million in federal and other income taxes receivable relating primarily to federal net operating loss carrybacks. These amounts are reflected in Prepaid expenses and other current assets in the Consolidated Balance Sheet.

As of December 31, 2002, we have federal and state credit carryforwards of approximately $6.6 million, most of which have no expiration date and with the remainder expiring at various dates between 2006 and 2022. We also have federal net operating loss carryforwards of $5.5 million and state net operating loss carryforwards of $7.7 million that expire at various dates from 2006 through 2022.

We acquired Cerdelinx on August 26, 2002 (see note 4). Cerdelinx had federal and state net operating loss and tax credit carryforwards at the time of the acquisition for which we recorded deferred tax assets of $2.8 million with an off-setting valuation allowance. In conjunction with the change in ownership, applicable Internal Revenue code sections limit the use of these tax benefits to approximately $400,000 per year.

Note 10. Long-term debt:

On October 28, 1999, we issued $260 million in 4 3/4% convertible subordinated notes due on November 1, 2006. These notes pay interest semi-annually on May 1 and November 1. Holders of these notes may convert them into shares of our common stock at any time on or before November 1, 2006, at a conversion price of $20.72 per share, subject to adjustment in certain events. Beginning on November 6, 2002 and ending on October 31, 2003, we may redeem the notes in whole or in part at a redemption price of 102.71% of the principal amount. In the subsequent three twelve-month periods, the redemption price declines to 102.04%, 101.36% and 100.68% of principal, respectively. The notes are subordinated in right of payment to all of our senior indebtedness, and are subordinated by operation of law to all liabilities of our subsidiaries. At December 31, 2002, we had no senior indebtedness and our subsidiaries had $2.5 million of debt and other liabilities outstanding.

During 2002, we extinguished approximately $51.9 million face value of our 4 3/4% convertible notes for approximately $42.8 million in cash, including accrued interest. We recognized a gain of approximately $9.3 million in connection with these transactions.

Issuance costs relative to the convertible subordinated notes are included in Other assets and aggregated approximately $6.9 million and are being amortized to expense over the lives of the notes. Accumulated amortization of these issuance costs amounted to approximately $5.3 million at December 31, 2002. The estimated fair value of the convertible subordinated notes, based on quoted market prices, was approximately $184.7 million and $315.9 million at December 31, 2002 and December 31, 2001, respectively.

Note 11. Stockholders' Equity:

Common Stock

In December 2000, our Board of Directors authorized management to repurchase up to five million shares of our common stock. As of December 31, 2002, we had repurchased 1,136,000 shares (596,000 in 2001) at an aggregate cost of approximately $20.0 million ($10.6 million in 2001). There were no repurchases of common stock in 2002.

Stock Warrants

During 2000, we issued a warrant to a vendor to purchase 74,000 shares of common stock, earned ratably from March 2000 to February 2001. During 2001, a warrant was issued to purchase 95,563 shares of common stock, earned ratably from March 2001 to February 2002. During 2002, a warrant was issued to purchase 119,074 shares of common stock, earned ratably from March 2002 to February 2003. Additionally, during 2002 the vendor exercised warrants for 206,200 shares at $13.75 per share, leaving 709,229 shares unexercised as of December 31, 2002, including warrants issued prior to 2000. Expense recorded in conjunction with the vesting of warrants by this vendor was not significant.

Stock Option Plans

As of December 31, 2002, we had authorized 9,000,000 and 17,200,000 shares of common stock for issuance to officers and employees under our 2001 Stock Option Plan and 1996 Stock Option Plan, respectively. The 2001 Plan options are granted at fair value at the date of grant, generally vest over four years in increments as determined by the Board of Directors and have terms up to ten years. The 1996 Plan options are typically granted at fair value at the date of grant, generally vest over four years in increments as determined by the Board of Directors and have terms up to ten years.

In conjunction with the acquisition of Cerdelinx on August 26, 2002, we exchanged 246,540 Lattice stock options for all of the options outstanding under the former Cerdelinx stock option plans. These options generally vest over four years and have terms of ten years. In conjunction with the acquisition of I2P on March 16, 2001, we exchanged 223,276 Lattice stock options for all of the options outstanding under the for I2P stock option plans. These options generally vest over four years and have terms of ten years.

Note 11. Stockholders' Equity (continued):

The 2001 Directors' Stock Option Plan, which replaced the 1993 Director's Stock Option Plan, provides for the issuance of stock options to members of our Board of Directors who are not employees of Lattice; 1,000,000 shares of our Common Stock are authorized for issuance thereunder. These options are granted at fair value at the date of grant and become exercisable quarterly over a one year period beginning three years after the date of grant and expire ten years from the date of grant.

The following table summarizes our stock option activity and related information for the past three years:

	YEAR ENDED DECEMBER 31, 2002		YEAR ENDED DECEMBER 31, 2001		YEAR ENDED DECEMBER 31, 2000	
	NUMBER OF SHARES UNDER OPTION	WEIGHTED-AVERAGE EXERCISE PRICE	NUMBER OF SHARES UNDER OPTION	WEIGHTED-AVERAGE EXERCISE PRICE	NUMBER OF SHARES UNDER OPTION	WEIGHTED-AVERAGE EXERCISE PRICE
	(Number of shares in thousands)					
Options outstanding at beginning of year	20,075	$ 17.71	17,008	$ 14.95	16,444	$ 9.80
Options granted	4,877	8.08	5,713	22.16	5,170	27.31
Options canceled	(721)	17.73	(399)	17.81	(1,306)	13.22
Options exercised	(191)	7.81	(2,247)	8.15	(3,300)	9.32
Options outstanding at end of year	24,040	$ 15.83	20,075	$ 17.71	17,008	$ 14.95

The following table summarizes information about stock options outstanding at December 31, 2002:

(Number of shares in thousands)	OPTIONS OUTSTANDING			OPTIONS EXERCISABLE	
RANGE OF EXERCISE PRICES	NUMBER OF SHARES	WEIGHTED-AVERAGE REMAINING CONTRACT LIFE (IN YEARS)	WEIGHTED-AVERAGE EXERCISE PRICE	NUMBER OF SHARES	WEIGHTED-AVERAGE EXERCISE PRICE
$ 0.41 – $ 7.75	6,341	7.93	$ 6.57	3,084	$ 7.41
$ 7.88 – $11.16	4,355	6.13	9.35	3,960	9.19
$11.89 – $17.08	4,602	7.87	15.40	2,362	15.37
$17.44 – $24.91	4,118	8.46	24.43	1,344	24.39
$24.92 – $32.25	4,624	7.45	27.40	2,695	27.53
	24,040	7.59	$15.83	13,445	$15.06

Stock Purchase Plan

Our employee stock purchase plan, most recently approved by the stockholders in August 1997, permits eligible employees to purchase shares of common stock through payroll deductions, not to exceed 10% of the employee's compensation. The purchase price of the shares is the lower of 85% of the fair market value of the stock at the beginning of each six-month period or 85% of the fair market value at the end of such period, but in no event less than the book value per share at the mid-point of each offering period. Amounts accumulated through payroll deductions during the offering period are used to purchase shares on the last day of the offering period. Of the 3,700,000 shares authorized to be issued under the plan, 347,107, 203,049, and 200,072 shares were issued during 2002, 2001 and 2000, respectively, and 906,612 shares were available for issuance at December 31, 2002.

Note 11. Stockholders' Equity (continued):

Stock Based Compensation

We account for our stock options and employee stock purchase plan in conformity with APB 25 and have adopted the additional pro forma disclosure provisions of SFAS 123, as amended by SFAS 148. The fair value of our stock-based employee compensation cost (see note 1), as defined by SFAS 123, for stock options and employee stock plan purchase rights was estimated on the date of grant using the Black-Scholes option pricing model with the following assumptions:

	GRANTS FOR YEARS ENDED		
	DEC. 31, 2002	DEC. 31, 2001	DEC. 31, 2000
Stock options:			
Expected volatility	59.3%	56.1%	53.9%
Risk-free interest rate	2.8%	3.9%	6.3%
Expected life from vesting date	1.7 years	1.9 years	1.8 years
Dividend yield	0%	0%	0%
Stock purchase rights:			
Expected volatility	64.3%	53.3%	46.6%
Risk-free interest rate	3.52%	4.65%	6.3%
Expected life	6 months	6 months	6 months
Dividend yield	0%	0%	0%

The Black-Scholes option pricing model was developed for use in estimating the fair value of freely tradable, fully transferable options without vesting restrictions. Our stock options have characteristics which differ significantly from those of freely tradable, fully transferable options. The Black-Scholes option pricing model also requires highly subjective assumptions, including expected stock price volatility and expected stock option term which greatly affect the calculated fair value of an option. Our actual stock price volatility and option term may be materially different from the assumptions used herein.

The resultant grant date weighted-average fair values calculated using the Black-Scholes option pricing model and the noted assumptions for stock options granted was $3.70, $10.29 and $13.13, and for stock purchase rights $5.32, $5.92 and $7.79, for 2002, 2001, and 2000, respectively. For purposes of pro forma disclosures (see note 1), the estimated fair value of the options is amortized to expense over the options' vesting period.

Note 12. Employee Benefit Plans:

Profit Sharing Plan

We initiated a profit sharing plan effective April 1, 1990. Under the provisions of this plan, as approved by the Board of Directors, a percentage of our operating income, as defined and calculated at the end of March and September for the prior six-month period, is paid to qualified employees. In 2002, the provision charged to operations for this plan was not significant. In 2001 and 2000, approximately $2.1 million, and $6.7 million, respectively, was charged against operations in connection with the plan.

Qualified Investment Plan

In 1990, we adopted a 401(k) plan, which provides participants with an opportunity to accumulate funds for retirement. Under the terms of the plan, eligible participants may contribute up to 15% of their eligible earnings to the plan Trust. The plan does not allow investments in our securities. The plan allows for us to make discretionary matching contributions in cash. For the years presented, matching contributions of up to 5% of base pay, vesting over four years, were made through the second quarter of 2001. There was no expense recorded related to matching contributions in 2002. Expense related to our matching contributions was approximately $1.0 million and $1.8 million, respectively, for 2001 and 2000.

Executive Deferred Compensation Plan

Our Executive Deferred Compensation Plan enables certain senior managers to annually defer up to 75% of their salary and up to 100% of their incentive compensation. The return on deferred funds is based upon the performance of designated mutual funds or our publicly traded common stock. There is no guaranteed return or matching contribution.

Note 13. Commitments and Contingencies:

We are exposed to certain asserted and unasserted potential claims. There can be no assurance that, with respect to potential claims made against us, that we could resolve such claims under terms and conditions that would not have a material adverse effect on our financial position, cash flows or results of operations.

Note 14. Related Party:

Larry W. Sonsini is a member of our Board of Directors and is presently the Chairman and CEO of Wilson Sonsini Goodrich & Rosati, Professional Corporation, a law firm that provides us with corporate legal services. Legal services billed to Lattice aggregated approximately $885,000, $1,314,000, and $373,000, respectively, for 2002, 2001 and 2000. Amounts payable to the law firm were not significant at December 31, 2002 or 2001, respectively.

Note 15. Segment and Geographic Information:

We operate in one industry segment comprising the design, development, manufacture and marketing of high performance programmable logic devices. Our sales by major geographic area were as follows:

	YEARS ENDED DECEMBER 31,		
	2002	2001	2000
	(In thousands)		
United States	$ 92,086	$135,832	$245,882
Export sales:			
Europe	58,871	81,177	158,591
Asia	67,324	62,582	120,285
Other	10,845	15,735	43,001
	137,040	159,494	321,877
	$229,126	$295,326	$567,759

Resale of product through two distributors accounted for approximately 22% and 29%, 20% and 19%, and 18% and 20% of total worldwide revenue for 2002, 2001, and 2000, respectively. No individual customer accounted for more than 10% of revenue for any of the years presented. More than 90% of our property and equipment is located in the United States. Other long-lived assets located outside the United States consist primarily of foundry investments and advances (see note 7).

Note 16. Subsequent Events:

During the first quarter of 2003, we have extinguished an additional $32.8 million of our convertible subordinated notes (see note 10) for approximately $29.9 million in cash, resulting in a gain of approximately $2.9 million.

REPORT OF INDEPENDENT ACCOUNTANTS

To the Board of Directors and Stockholders of
Lattice Semiconductor Corporation

In our opinion, the accompanying consolidated balance sheet and the related consolidated statements of operations, of changes in stockholders' equity, and of cash flows present fairly, in all material respects, the financial position of Lattice Semiconductor Corporation and its subsidiaries (the Company) at December 31, 2002 and 2001, and the results of their operations and their cash flows for each of the three years in the period ended December 31, 2002 in conformity with accounting principles generally accepted in the United States of America. These financial statements are the responsibility of the Company's management; our responsibility is to express an opinion on these financial statements based on our audits. We conducted our audits of these statements in accordance with auditing standards generally accepted in the United States of America, which require that we plan and perform the audit to obtain reasonable assurance about whether the financial statements are free of material misstatement. An audit includes examining, on a test basis, evidence supporting the amounts and disclosures in the financial statements, assessing the accounting principles used and significant estimates made by management, and evaluating the overall financial statement presentation. We believe that our audits provide a reasonable basis for our opinion.

As discussed in Note 1 to the consolidated financial statements, on January 1, 2002 the Company changed its method of accounting for goodwill.

PricewaterhouseCoopers LLP

Portland, Oregon
February 14, 2003

Item 9. Changes in and Disagreements with Accountants On Accounting and Financial Disclosure.

None.

PART III

Certain information required by Part III is incorporated by reference from our definitive proxy statement for the Annual Meeting of Stockholders to be held on May 6, 2003, pursuant to Regulation 14A of the Securities Exchange Act of 1934, as amended (the "Proxy Statement"), which we will file not later than 120 days after the end of the fiscal year covered by this report. With the exception of the information expressly incorporated by reference from the Proxy Statement, the Proxy Statement is not to be deemed filed as a part of this report.

Item 10. Directors and Executive Officers of the Registrant.

Information regarding our directors that is required by this item is incorporated by reference from the information contained under the caption "Proposal 1: Election of Directors" in the Proxy Statement. Information regarding our officers that is required by this item is set forth in Part I of this report under the caption "Executive Officers and Directors of the Registrant." Information regarding Section 16 reporting compliance that is required by this item is incorporated by reference from the information contained under the caption "Beneficial Ownership Reporting Compliance" in the Proxy Statement.

Item 11. Executive Compensation.

The information contained under the captions entitled "Proposal 1: Election of Directors," "Executive Compensation," "Options Granted and Options Exercised in the Last Fiscal Year" and "Comparison of Total Cumulative Stockholder Return" in the Proxy Statement is incorporated herein by reference.

Item 12. Security Ownership of Certain Beneficial Owners and Management and Related Stockholder Matters.

The information contained under the caption entitled "Security Ownership of Certain Beneficial Owners and Management" in the Proxy Statement is incorporated herein by reference.

Equity Compensation Plan Information

The following table summarizes information, as of December 31, 2002, with respect to shares of our common stock that may be issued under our existing equity compensation plans. The table does not include information with respect to shares subject to outstanding options assumed by us in connection with mergers and acquisitions. Footnote (4) to the table sets forth the total number of shares of our common stock issuable upon the exercise of those assumed options as of December 31, 2002, and the weighted average exercise price of those options. No additional options may be granted under those assumed plans.

	(A) NUMBER OF SECURITIES TO BE ISSUED UPON EXERCISE OF OUTSTANDING OPTIONS, WARRANTS AND RIGHTS	(B) WEIGHTED-AVERAGE EXERCISE PRICE OF OUTSTANDING OPTIONS, WARRANTS AND RIGHTS	(C) NUMBER OF SECURITIES REMAINING AVAILABLE FOR FUTURE ISSUANCE UNDER EQUITY COMPENSATION PLANS (EXCLUDING SECURITIES REFLECTED IN COLUMN (A))
	(In thousands except per share amounts)		
Equity compensation plans approved by security holders[1]	21,395	$16.59	4,402[2]
Equity compensation plans not approved by security holders[3]	709	$15.13	0
Total	22,104[4]	$16.55	4,402

[1] Includes shares of our common stock issuable upon exercise of options from the 1996 Stock Incentive Plan, the 2001 Stock Plan, the 1993 Outside Directors Stock Option Plan and the 2001 Outside Directors' Stock Option Plan.

[2] Includes approximately 907 shares reserved for issuance under our Employee Stock Purchase Plan.

[3] Consists of shares of our common stock issuable upon exercise of warrants issued to a vendor as compensation for services. The warrants have an exercise price equal to the closing market price on the date of issue and are earned by the vendor ratably over the life of the service period, usually one year, and usually have a term of 5 years.

[4] The table does not include information for the stock options assumed by the us in connection with mergers and acquisitions. As of December 31, 2002, a total of approximately 2,645 shares of our common stock were issuable upon exercise of those assumed options. The weighted-average exercise price of those assumed options is $9.65 per share.

Item 13. Certain Relationships and Related Transactions.

The information contained under the caption entitled "Proposal 1: Election of Directors - Transactions with Management" in the Proxy Statement is incorporated herein by reference.

Item 14. Controls and Procedures

(a) *Evaluation of disclosure controls and procedures.* Within the 90-day period prior to the date of this report, we carried out an evaluation, under the supervision and with the participation of our management, including our Chief Executive Officer and Chief Financial Officer, of the effectiveness of the design and operation of our disclosure controls and procedures (as defined in Rules 13a-14(c) and 15d — 14(c) of the Securities Exchange Act of 1934 (the "Exchange Act")). Based upon that evaluation, the Chief Executive Officer and Chief Financial Officer concluded that our disclosure controls and procedures are effective in ensuring that information required to be disclosed by the Company in the reports that it files or submits under the Exchange Act is recorded, processed, summarized and reported within the time periods specified in the Securities and Exchange Commission's rules and forms.

(b) *Changes in internal controls.* There have been no significant changes in our internal controls or in other factors which could significantly affect our internal controls subsequent to the date we carried out our evaluation, including any corrective actions with regard to significant deficiencies and material weaknesses.

PART IV

Item 15. Exhibits, Financial Statement Schedules and Reports on Form 8-K.

(a)(1) and (2) Financial Statements and Financial Statement Schedules.

The information required by this Item is included under Item 8 of this Report.

(a)(3) EXHIBITS.

3.1 The Company's Certificate of Incorporation, as amended (Incorporated by reference to Exhibit 3.1 filed with the Company's Registration Statement on Form S-3 on July 11, 2000).

3.2 The Company's Bylaws, as amended and restated as of February 4, 2003.

4.2 Indenture between Lattice Semiconductor Corporation and State Street Bank and Trust Company of California, N.A., dated as of November 1, 1999 (Incorporated by reference to Exhibit 4.1 filed with the Company's Registration Statement on Form S-3 on December 21, 1999).

4.3 Form of Note for the Company's 4¾% Convertible Subordinated Notes (Incorporated by reference to Exhibit 4.3 filed with the Company's Registration Statement on Form S-3 on December 21, 1999).

10.10 * Form of Stock Option Agreement (Incorporated by reference to Exhibit 10.9, File No. 33-31231).

10.11 * Employment Letter dated September 2, 1988 from Lattice Semiconductor Corporation to Cyrus Y. Tsui (Incorporated by reference to Exhibit 10.10, File No. 33-31231).

10.15 * 1993 Outside Directors Stock Option Plan (Incorporated by reference to Exhibit 10.15 filed with the Company's Annual Report on Form 10-K for the fiscal year ended April 3, 1993).

10.16 * Employee Stock Purchase Plan, as amended and restated effective May 7, 2002 (Incorporated by reference to Exhibit 4.3 filed with the Company's Registration Statement on Form S-8 filed September 6, 2002).

10.20 Foundry Venture Side Letter dated September 13, 1995 among Lattice Semiconductor Corporation, United Microelectronics Corporation and FabVen (Incorporated by reference to Exhibit 10.2 filed with the Company's Current Report on Form 8-K dated September 28, 1995)[(1)].

10.21 FabVen Foundry Capacity Agreement dated as of August ___, 1995 among FabVen, United Microelectronics Corporation and Lattice Semiconductor Corporation (Incorporated by reference to Exhibit 10.3 filed with the Company's Current Report on Form 8-K dated September 28, 1995)[(1)].

10.22 Foundry Venture Agreement dated as of August ___, 1995, between Lattice Semiconductor Corporation and United Microelectronics Corporation (Incorporated by reference to Exhibit 10.4 filed with the Company's Current Report on Form 8-K dated September 28, 1995)[(1)].

10.23 Advance Production Payment Agreement dated March 17, 1997 among Lattice Semiconductor Corporation and Seiko Epson Corporation and S MOS Systems, Inc. (Incorporated by reference to Exhibit 10.23 filed with the Company's Annual Report on Form 10-K for the fiscal year ended March 29, 1997)[(1)].

10.24 * Lattice Semiconductor Corporation 1996 Stock Incentive Plan as amended and Related Form of Option Agreement (Incorporated by reference to Exhibits (d)(1) and (d)(2) on Schedule TO filed February 13, 2003).

10.30 Registration Rights Agreement by and among Lattice Semiconductor Corporation, Morgan Stanley & Co. Incorporated, Goldman Sachs & Co., BancBoston Robertson Stephens Inc. and ABN Amro Incorporated dated as of November 3, 1999 (Incorporated by reference to Exhibit 4.2 filed with the Company's Registration Statement on Form S-3 on December 21, 1999).

10.31 Asset Purchase Agreement by and between Agere Systems Inc. and Lattice Semiconductor Corporation, dated December 7, 2001 (Incorporated by reference to Exhibit 10.1 filed with the Company's Current Report on Form 8-K filed on December 18, 2001).

10.32 Amendment dated December 21, 2001 to Advance Production Payment Agreement dated March 17, 1997 among Lattice Semiconductor Corporation and Seiko Epson Corporation and S MOS Systems, Inc.[(1)] (Incorporated by reference to Exhibit 10.32 filed with the Company's Annual Report on Form 10-K for the year ended December 31, 2001).

10.33 * 2001 Outside Directors' Stock Option Plan (Incorporated by reference to Appendix B filed with the Company's Definitive Proxy Statement on Schedule 14A filed on March 23, 2001).

10.34 * 2001 Stock Plan as amended and Related Form of Option Agreement (Incorporated by reference to Exhibits (d)(3) and (d)(4) on Schedule TO filed February 13, 2003).

10.35 Intellectual Property Agreement by and between Agere Systems Inc. and Agere Systems Guardian Corporation and Lattice Semiconductor Corporation as Buyer, dated January 18, 2002 (Incorporated by reference to Exhibit 10.35 filed with the Company's Annual Report on Form 10-K for the year ended December 31, 2001).

10.36 * Octillion Communication, Inc. 2001 Stock Plan (Incorporated by reference to Exhibit 4.1 filed with the Company's Registration Statement on Form S-8 filed on September 6, 2002.)**

10.37 * Lattice Semiconductor Corporation Executive Deferred Compensation Plan, as Amended and Restated effective as of August 11, 1997 (Incorporated by reference to Exhibit 99.3 filed with the Company's Registration Statement on Form S-3, as amended, dated October 17, 2002).

10.38 * Amendment No. 1 to the Lattice Semiconductor Corporation Executive Deferred Compensation Plan, as Amended and Restated effective as of August 11, 1997, dated November 19, 1999 (Incorporated by reference to Exhibit 99.3 filed with the Company's Registration Statement on Form S-3, as amended, dated October 17, 2002).

21.1 Subsidiaries of the Registrant.

23.1 Consent of Independent Accountants.

24.1 Power of Attorney (see page 55).

[(1)] Pursuant to Rule 24b-2 under the Securities Exchange Act of 1934, confidential treatment has been granted to portions of this exhibit, which portions have been deleted and filed separately with the Securities and Exchange Commission.

* Management contract or compensatory plan or arrangement required to be filed as an Exhibit to this Annual Report on Form 10-K pursuant to Item 14(c) thereof.

** Cerdelinx Technologies, Inc. was initially incorporated as Octillian Communications, Inc.

On December 19, 2002, we filed a report on Form 8-K/A dated January 18, 2002 amending Item 7 of our Current report on Form 8-K, originally filed with the Securities and Exchange Commission on February 4, 2002 and amended on April 2, 2002, reporting our acquisition from Agere Systems Inc., a Delaware corporation, of the field programmable gate array business of Agere.

(c) See (a)(3) above.

(d) See (a)(1) and (2) above.

SIGNATURES

Pursuant to the requirements of Section 13 or 15(d) of the Securities Exchange Act of 1934, the Registrant has duly caused this Report to be signed on its behalf by the undersigned, thereunto duly authorized, in the City of Hillsboro, State of Oregon, on the 19th of March, 2003.

LATTICE SEMICONDUCTOR CORPORATION

/s/ Stephen A. Skaggs

Stephen A. Skaggs, Senior Vice President,
Chief Financial Officer and Secretary

POWER OF ATTORNEY

KNOW ALL PERSONS BY THESE PRESENTS, that each person whose signature appears below constitutes and appoints Cyrus Y. Tsui and Stephen A. Skaggs, jointly and severally, his attorneys-in-fact, each with the power of substitution, for him in any and all capacities, to sign any amendments to this Report on Form 10-K, and to file the same, with exhibits thereto and other documents in connection therewith, with the Securities and Exchange Commission, hereby ratifying and confirming all that each of said attorneys-in-fact, or his substitute or substitutes, may do or cause to be done by virtue hereof.

Pursuant to the requirements of the Securities Exchange Act of 1934, this Report has been signed below by the following persons on the 19th day of March, 2003 on behalf of the Registrant and in the capacities indicated:

SIGNATURE	TITLE
/s/ Cyrus Y. Tsui Cyrus Y. Tsui	Chief Executive Officer and Chairman of the Board (Principal Executive Officer)
/s/ Steven A. Laub Steven A. Laub	President and Director
/s/ Stephen A. Skaggs Stephen A. Skaggs	Senior Vice President, Chief Financial Officer and Secretary (Principal Financial Officer)
/s/ Mark O. Hatfield Mark O. Hatfield	Director
/s/ Daniel S. Hauer Daniel S. Hauer	Director
/s/ Harry A. Merlo Harry A. Merlo	Director
/s/ Larry W. Sonsini Larry W. Sonsini	Director
/s/ Soo Boon Koh Soo Boon Koh	Director

CERTIFICATIONS

I, Cyrus Y. Tsui, certify that:

1. I have reviewed this annual report on Form 10-K of Lattice Semiconductor Corporation;
2. Based on my knowledge, this annual report does not contain any untrue statement of a material fact or omit to state a material fact necessary to make the statements made, in light of the circumstances under which such statements were made, not misleading with respect to the period covered by this annual report;
3. Based on my knowledge, the financial statements, and other financial information included in this annual report, fairly present in all material respects the financial condition, results of operations and cash flows of the registrant as of, and for, the periods presented in this annual report;
4. The registrant's other certifying officer and I are responsible for establishing and maintaining disclosure controls and procedures (as defined in Exchange Act Rules 13a-14 and 15d-14) for the registrant and have:
   a) designed such disclosure controls and procedures to ensure that material information relating to the registrant, including its consolidated subsidiaries, is made known to us by others within those entities, particularly during the period in which this annual report is being prepared;
   b) evaluated the effectiveness of the registrant's disclosure controls and procedures as of a date within 90 days prior to the filing date of this annual report (the "Evaluation Date"); and
   c) presented in this annual report our conclusions about the effectiveness of the disclosure controls and procedures based on our evaluation as of the Evaluation Date;
5. The registrant's other certifying officer and I have disclosed, based on our most recent evaluation, to the registrant's auditors and the audit committee of registrant's board of directors (or persons performing the equivalent functions):
   a) all significant deficiencies in the design or operation of internal controls which could adversely affect the registrant's ability to record, process, summarize and report financial data and have identified for the registrant's auditors any material weaknesses in internal controls; and
   b) any fraud, whether or not material, that involves management or other employees who have a significant role in the registrant's internal controls; and
6. The registrant's other certifying officer and I have indicated in this annual report whether or not there were significant changes in internal controls or in other factors that could significantly affect internal controls subsequent to the date of our most recent evaluation, including any corrective actions with regard to significant deficiencies and material weaknesses.

Date: March 19, 2003

/s/ Cyrus Y. Tsui

Cyrus Y. Tsui
Chief Executive Officer

I, Stephen A. Skaggs, certify that:

1. I have reviewed this annual report on Form 10-K of Lattice Semiconductor Corporation;
2. Based on my knowledge, this annual report does not contain any untrue statement of a material fact or omit to state a material fact necessary to make the statements made, in light of the circumstances under which such statements were made, not misleading with respect to the period covered by this annual report;
3. Based on my knowledge, the financial statements, and other financial information included in this annual report, fairly present in all material respects the financial condition, results of operations and cash flows of the registrant as of, and for, the periods presented in this annual report;
4. The registrant's other certifying officer and I are responsible for establishing and maintaining disclosure controls and procedures (as defined in Exchange Act Rules 13a-14 and 15d-14) for the registrant and have:
   a) designed such disclosure controls and procedures to ensure that material information relating to the registrant, including its consolidated subsidiaries, is made known to us by others within those entities, particularly during the period in which this annual report is being prepared;
   b) evaluated the effectiveness of the registrant's disclosure controls and procedures as of a date within 90 days prior to the filing date of this annual report (the "Evaluation Date"); and
   c) presented in this annual report our conclusions about the effectiveness of the disclosure controls and procedures based on our evaluation as of the Evaluation Date;
5. The registrant's other certifying officer and I have disclosed, based on our most recent evaluation, to the registrant's auditors and the audit committee of registrant's board of directors (or persons performing the equivalent functions):
   a) all significant deficiencies in the design or operation of internal controls which could adversely affect the registrant's ability to record, process, summarize and report financial data and have identified for the registrant's auditors any material weaknesses in internal controls; and
   b) any fraud, whether or not material, that involves management or other employees who have a significant role in the registrant's internal controls; and
6. The registrant's other certifying officer and I have indicated in this annual report whether there were significant changes in internal controls or in other factors that could significantly affect internal controls subsequent to the date of our most recent evaluation, including any corrective actions with regard to significant deficiencies and material weaknesses.

Date: March 19, 2003

/s/ Stephen A. Skaggs

Stephen A. Skaggs
Chief Financial Officer

EXHIBIT 21.1

LATTICE SEMICONDUCTOR CORPORATION
SUBSIDIARIES OF THE REGISTRANT

NAME	JURISDICTION OF INCORPORATION
1. Lattice Semiconductor GmbH	Germany
2. Lattice Semiconducteurs SARL	France
3. Lattice Semiconductor AB	Sweden
4. Lattice Semiconductor Asia Limited	Hong Kong
5. Lattice Semiconductor KK	Japan
6. Lattice Semiconductor (Shanghai) Co. Ltd.	China
7. Lattice UK Limited	United Kingdom
8. Lattice Semiconductor SRL	Italy
9. Vantis International Limited	Delaware, USA
10. Lattice Semiconductor Canada Corporation	Canada
11. Lattice Semiconductor Corp. Worldwide	Cayman Islands

EXHIBIT 23.1

Consent of Independent Accountants

We hereby consent to the incorporation by reference in the Registration Statements on Form S-8 (No. 33-33933, No. 33-35259, No. 33-38521, No. 33-76358, No. 33-51232, No. 33-69496, No. 333-15737, No. 333-40031, No. 333-59990, No. 333-69467, No. 333-81035, No. 333-67274 and No. 333-99247) and the Registration Statements on Form S-3 (No. 333-15741, No. 333-40043, No. 333-69469, No. 333-93285, No. 333-93289, No. 333-50192, No. 333-59992, No. 333-88128 and No. 333-99249) of Lattice Semiconductor Corporation and subsidiaries of our report dated February 14, 2003 relating to the consolidated financial statements, which appears in this Form 10-K. We also consent to the incorporation by reference of our report dated February 14, 2003 relating to the financial statement schedule, which appears in this Form 10-K.

PricewaterhouseCoopers LLP

Portland, Oregon
March 19, 2003

EXHIBIT 99.1

CERTIFICATION OF CHIEF EXECUTIVE OFFICER AND CHIEF FINANCIAL OFFICER
PURSUANT TO
18 U.S.C. SECTION 1350,
AS ADOPTED PURSUANT TO
SECTION 906 OF THE SARBANES-OXLEY ACT OF 2002

I, Cyrus Y. Tsui, certify, pursuant to 18 U.S.C. Section 1350, as adopted pursuant to Section 906 of the Sarbanes-Oxley Act of 2002, that the Annual Report of Lattice Semiconductor Corporation on Form 10-K for the year ended December 31, 2002 fully complies with the requirements of Section 13(a) or 15(d) of the Securities Exchange Act of 1934 and that information contained in such Annual Report fairly presents, in all material respects, the financial condition and results of operations of Lattice Semiconductor Corporation.

By: /s/ Cyrus Y. Tsui
Name: Cyrus Y. Tsui
Title: Chief Executive Officer

I, Stephen A. Skaggs, certify, pursuant to 18 U.S.C. Section 1350, as adopted pursuant to Section 906 of the Sarbanes-Oxley Act of 2002, that the Annual Report of Lattice Semiconductor Corporation on Form 10-K for the year ended December 31, 2002 fully complies with the requirements of Section 13(a) or 15(d) of the Securities Exchange Act of 1934 and that information contained in such Annual Report fairly presents, in all material respects, the financial condition and results of operations of Lattice Semiconductor Corporation.

By: /s/ Stephen A. Skaggs
Name: Stephen A. Skaggs
Title: Chief Financial Officer

REPORT OF INDEPENDENT ACCOUNTANTS ON FINANCIAL STATEMENT SCHEDULE

To the Board of Directors of
Lattice Semiconductor Corporation

Our audits of the consolidated financial statements referred to in our report dated February 14, 2003 appearing in the 2002 Annual Report to Stockholders of Lattice Semiconductor Corporation and subsidiaries (which report and consolidated financial statements are also included in this Annual Report on Form 10-K) also included an audit of the financial statement schedule listed in Item 15(a)(2) of this Form 10-K. In our opinion, this financial statement schedule presents fairly, in all material respects, the information set forth therein when read in conjunction with the related consolidated financial statements.

PricewaterhouseCoopers LLP

Portland, Oregon
February 14, 2003

VALUATION AND QUALIFYING ACCOUNTS

(In thousands)

Schedule II

COLUMN A CLASSIFICATION	COLUMN B BALANCE AT BEGINNING OF PERIOD	COLUMN C CHARGED TO COSTS AND EXPENSES	COLUMN D CHARGED TO OTHER ACCOUNTS (DESCRIBE)	COLUMN E WRITE-OFFS NET OF RECOVERIES	COLUMN F BALANCE AT END OF PERIOD
Fiscal year ended December 31, 2000:					
Allowance for doubtful accounts.	$1,583	$ 150	$ —	$ (33)	$1,700
	$1,583	$ 150	$ —	$ (33)	$1,700
Fiscal year ended December 31, 2001:					
Allowance for doubtful accounts.	$1,700	$ (225)	$ —	$ —	$1,475
	$1,700	$(225)	$ —	$ —	$1,475
Fiscal year ended December 31, 2002:					
Allowance for doubtful accounts.	$1,475	$ (401)	$ —	$ —	$1,074
	$1,475	$ (401)	$ —	$ —	$1,074

CORPORATE DIRECTORY

BOARD OF DIRECTORS
Cyrus Y. Tsui
Chairman and
Chief Executive Officer

Steven A. Laub
President

Mark O. Hatfield[1,2]
Former U.S. Senator

Daniel S. Hauer[2]
Business Consultant

Soo Boon Koh[1]
Managing Partner,
iGlobe Partners, Inc.

Harry A. Merlo[1]
President,
Merlo Corporation

Larry W. Sonsini
Chairman and CEO,
Wilson, Sonsini, Goodrich & Rosati,
Professional Corporation

OFFICERS
Cyrus Y. Tsui
Chairman and
Chief Executive Officer

Steven A. Laub
President

Stephen A. Skaggs
Senior Vice President,
Chief Financial Officer and Secretary

Frank J. Barone
Corporate Vice President,
Product Operations

Stephen M. Donovan
Corporate Vice President,
Sales

Jonathan K. Yu
Corporate Vice President,
Business Development

Martin R. Baker
Vice President and
General Counsel

Jan Johannessen
Vice President,
Investments

Rodney F. Sloss
Vice President,
Finance

Kenneth K. Yu
Vice President and Managing
Director, Lattice Asia

[1] Member of the Audit Committee
[2] Member of the Compensation Committee

CORPORATE HEADQUARTERS
Lattice Semiconductor Corporation
5555 N.E. Moore Court
Hillsboro, Oregon 97124-6421
Telephone:(503) 268-8000
Facsimile: (503) 268-8347

LEGAL COUNSEL
Wilson, Sonsini, Goodrich & Rosati
Palo Alto, California

INDEPENDENT ACCOUNTANTS
PricewaterhouseCoopers LLP
Portland, Oregon

REGISTRAR AND TRANSFER AGENT
Mellon Investor Services LLC
Shareholder Relations
P.O. Box 3315
South Hackensack, NJ 07606
Telephone: (800) 522-6645
(201) 329-8660
Web: www.melloninvestor.com

ANNUAL MEETING
Our annual meeting of stockholders will be held at our corporate headquarters on Tuesday, May 6, 2003, at 1:00 PM.

FORM 10-K AND ADDITIONAL INFORMATION
Our website is www.latticesemi.com. We make available free of charge through our website, via a link to the SEC's website at http://www.sec.gov, our annual reports on Form 10-K, quarterly reports on Form 10-Q and current reports on Form 8-K and amendments to those reports as soon as reasonably practicable after such materials are electronically filed with, or furnished to, the SEC. You may also obtain free copies of these materials by contacting our Investor Relations Department at 5555 N.E. Moore Court, Hillsboro, Oregon 97124-6421, Telephone (503) 268-8000.

COMMON STOCK
Our common stock is traded on the NASDAQ National Market System under the symbol "LSCC."

STOCK PRICE HISTORY

	Low	High
2001:		
March	$ 16.75	$ 27.25
June	15.88	27.64
September	14.04	25.85
December	14.36	22.65
2002:		
March	$ 17.06	$ 24.14
June	6.94	18.49
September	5.35	9.36
December	4.08	10.79

Design: Lawrence Bender & Associates

Lattice Semiconductor Corporation

5555 N.E. Moore Court
Hillsboro, Oregon 97124-6421
U.S.A.