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UNITED STATES
SECURITIES AND EXCHANGE COMMISSION
WASHINGTON, D.C 20549

FORM 10-K

COMMISSION FILE NUMBER: 0-18032

/X/ TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934

FOR THE TRANSITION PERIOD FROM APRIL 4, 1999 TO JANUARY 1, 2000

LATTICE SEMICONDUCTOR CORPORATION
(Exact name of Registrant as specified in its Charter)

DELAWARE	93-0835214
(State of Incorporation)	(I.R.S Employer Identification No.)
5555 NE MOORE COURT, HILLSBORO, OREGON	97124-6421
(Address of principal executive offices)	(Zip Code)

Registrant's telephone number, including area code: (503) 268-8000

SECURITIES REGISTERED PURSUANT TO SECTION 12(b) OF THE ACT: NONE

SECURITIES REGISTERED PURSUANT TO SECTION 12(g) OF THE ACT:

TITLE OF CLASS	NAME OF EXCHANGE
Common Stock, $.01 par value	NASDAQ
Preferred Share Purchase Rights	None

Indicate by check mark whether the Registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the Registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days.

Yes /X/ No / /

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of the Registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K.

Yes / / No /X/

As of March 16, 2000, the aggregate market value of the shares of voting stock of the Registrant held by non-affiliates was approximately $2.33 billion. Shares of Common Stock held by each officer and director and by each person who owns 5% or more of the outstanding Common Stock have been excluded in that such persons may be deemed affiliates. This determination of affiliate status is not necessarily a conclusive determination for other purposes.

As of March 16, 2000, 49,163,765 shares of the Registrant's common stock were outstanding.

DOCUMENTS INCORPORATED BY REFERENCE

1. Portions of the Annual Report to Stockholders for the fiscal period ended January 1, 2000 are incorporated by reference in Part II hereof.

2. Portions of the definitive proxy statement of the Registrant to be filed pursuant to Regulation 14A for the Fiscal Period 1999 Annual Meeting of Stockholders to be held on May 2, 2000 are incorporated by reference in Part III hereof.

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LATTICE SEMICONDUCTOR CORPORATION

FORM 10-K

ANNUAL REPORT

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ITEM 1. BUSINESS

Lattice Semiconductor Corporation, ("Lattice"), founded in 1983 and based in Hillsboro, Oregon, designs, develops and markets the broadest range of high performance ISP-TM- programmable logic devices ("PLDs") and offers total solutions for today's advanced logic designs. We introduced in-system programmability to the logic industry in 1992. Our products are sold worldwide through an extensive network of independent sales representatives and distributors primarily to OEM customers in the communications, computing, industrial and military end markets. Approximately one-half of our revenue is derived from export sales, mainly to Europe and Asia.

In June 1999, we acquired Vantis Corporation, Advanced Micro Device, Inc.'s ("AMD's") PLD division, for approximately $500 million in cash. The transaction is being accounted for under the purchase method in our consolidated financial statements beginning with the period ended July 3, 1999. We have also agreed with AMD to sign a mutual election under the Internal Revenue Code that will allow us to deduct the purchase price for tax purposes over a 15-year period. We believe this acquisition will enable us to increase our share of the PLD market, accelerate development of new products and technologies and provide us with access to a complementary customer base. While Vantis remains a wholly-owned subsidiary, its business, which was substantially similar to our business, has been integrated into our operations. Prior to the acquisition, Vantis relied upon AMD for most manufacturing services. As a part of our acquisition agreement, AMD has agreed to continue to perform these services for a specific time period.

CHANGE IN FISCAL REPORTING PERIOD

In the fourth quarter of calendar 1999, we changed our reporting period to a 52 or 53 week year ending on the Saturday closest to December 31 from a 52 or 53 week fiscal year ending on the Saturday closest to March 31. This Form 10-K covers the nine-month transition period from April 4, 1999 to January 1, 2000. For purposes of this report and for ease of presentation, December 31 or March 31 has been utilized as the fiscal year end date for all financial statement captions contained herein. Additionally, for purposes of this report the nine month fiscal period ended January 1, 2000 is referred to as "the nine months ended December 31, 1999 or "fiscal period 1999". The fiscal periods ended April 3, 1999 and March 28, 1998, respectively, are referred to as "the fiscal year ended March 31, 1999" and "the fiscal year ended March 31, 1998", or "fiscal year 1999" and "fiscal year 1998", respectively.

PLD MARKET BACKGROUND

Three principal types of digital integrated circuits are used in most electronic systems: microprocessors, memory and logic. Microprocessors are used for control and computing tasks, memory is used to store programming instructions and data, and logic is employed to manage the interchange and manipulation of digital signals within a system. Logic contains interconnected groupings of simple logical "AND" and logical "OR" functions, commonly described as "gates." Typically, complex combinations of individual gates are required to implement the specialized logic functions required for systems applications. While system designers use a relatively small number of standard architectures to meet their microprocessor and memory needs, they require a wide variety of logic circuits in order to achieve end product differentiation.

Logic circuits are found in a wide range of today's digital electronic equipment including communication, computing, industrial and military systems. According to World Semiconductor Trade Statistics, a semiconductor industry association, logic accounted for approximately 27% of the estimated $130 billion worldwide digital integrated circuit market in 1999. The logic market encompasses, among other segments, standard logic, custom-designed ASICs, which include conventional gate-arrays, standard cells and full custom logic circuits, and PLDs.

Manufacturers of electronic equipment are increasingly challenged to bring differentiated products to market quickly. These competitive pressures often preclude the use of custom-designed ASICs, which generally entail significant design risks and time delay. Standard logic products, an alternative to custom-

designed ASICs, limit a manufacturer's flexibility to adequately customize an end system. PLDs address this inherent dilemma. PLDs are standard products, purchased by systems manufacturers in a "blank" state, that can be custom configured into a virtually unlimited number of specific logic functions by programming the device with electrical signals. PLDs give system designers the ability to quickly create their own custom logic functions to provide product differentiation without sacrificing rapid time to market. Certain PLD products, including our own, are reprogrammable, meaning that the logic configuration can be modified, if needed, after the initial programming. ISP PLDs, pioneered by us, extend the flexibility of standard reprogrammable PLDs by allowing the system designer to configure and reconfigure the logic functions of the PLD with standard 5-volt or 3.3-volt power supplies without removing the PLD from the system board.

The PLD market has two primary segments: low-density PLDs (less than 1,000 logic gates) and high-density PLDs (greater than 1,000 logic gates). High-density PLD devices include devices based on both the CPLD and field programmable gate array, or FPGA, architectures.

Products based on these alternative high-density PLD architectures are generally optimal for different types of logic functions, although many logic functions can be implemented using either architecture. CPLDs are characterized by a regular building block structure of wide-input logic cells, called macrocells, and use of a centralized logic interconnect scheme. CPLDs are optimal for control logic applications, such as state machines, bus arbitration, encoders, decoders and sequencers. FPGAs are characterized by a narrow-input logic cell and use a distributed interconnect scheme. FPGAs are optimal for register intensive and data path logic applications such as interface logic and arithmetic functions. We believe that a substantial portion of high-density PLD customers utilize both CPLD and FPGA architectures within a single system design, partitioning logic functions across multiple devices to optimize overall system performance and cost.

TECHNOLOGY

We believe that our proprietary E(2)CMOS-Registered Trademark- technology is the preferred process technology for PLD products due to its inherent performance, reprogrammability and testability benefits. E(2)CMOS technology, through its fundamental ability to be programmed and erased electronically, serves as the foundation for our ISP products.

We pioneered the development of ISP products which utilize 5-volt or 3.3-volt programming signals and, as a result, can be configured and reconfigured by a system designer without being removed from the printed circuit board. Standard E(2)CMOS PLDs require a 12-volt programming signal and therefore must be removed from the printed circuit board and programmed using specialized hardware. ISP devices offer enhanced flexibility versus standard PLDs and provide significant customer benefits. ISP devices can allow customers to reduce design cycle times, accelerate time to market, reduce prototyping costs, reduce manufacturing costs and lower inventory requirements. ISP devices can also provide customers the opportunity to perform simplified and cost-effective field reconfiguration through a data file transferred by computer disk or serial data signal.

PRODUCTS

ISP PRODUCTS

We first entered the ISP market in 1992 and currently offer eleven distinct families of proprietary ISP products, each consisting of multiple devices. We are currently shipping over 300 performance, package

and temperature range combinations of ISP products. The key features of our CPLD product families are described in the table below:

	SPEED (MHZ)	PROPAGATION DELAY (NANOSECONDS)	GATES	SURFACE MOUNT PINS
ispLSI-Registered Trademark- 1000/E/EA	200	4.0	2,000-8,000	44-128
ispLSI 2000E/VE	225	3.5	1,000-8,000	44-208
ispLSI 3000/E	125	7.5	7,000-20,000	160-432
ispLSI 5000V	125	7.5	12,000-24,000	208-388
ispLSI 8000/V	125	8.5	25,000-50,000	272-492
MACH-Registered Trademark- 1/2	180	5.0	1,000-5,000	44-100
MACH 4/LV/A	180	5.0	1,000-10,000	44-256
MACH 5/LV	180	5.5	5,000-20,000	100-352

Our newest product families, the MACH 4A, ispLSI 2000VE, ispLSI 5000V and ispLSI 8000V, use new innovative architectures and are targeted towards the emerging 3.3 volt CPLD market.

We offer three additional ISP product families:

ISPGAL-REGISTERED TRADEMARK-: This proprietary family combines in-system programmability with the industry standard 22V10 low-density PLD architecture. Offered with performance of up to 200 MHz (5.0 nanosecond propagation delay), the ispGAL family is available in both 5-volt and 3.3-volt operating supply versions.

ISPGDX-REGISTERED TRADEMARK-: This family extends in-system programmability to the circuit board level using an innovative digital cross-point switch architecture. Offered with propagation delays as low as 5.0 nanoseconds, up to 160 I/O and complete pin-to-pin signal routing, the ispGDX is targeted towards digital signal interconnect and interface applications.

ISPPAC-REGISTERED TRADEMARK-: First introduced in 1999, this three device family extends in-system programmability to the analog market. The innovative architecture of the ispPAC allows designers to quickly and easily program resistor and capacitor values, gain and signal polarity and circuit interconnect to implement a wide variety of analog circuits. The initial ispPAC products are targeted towards filtering and signal conditioning applications and can replace numerous discrete analog components. ispPAC designs are implemented and programmed via a PC using our intuitive software development tool, PAC-Designer.

We plan to continue to introduce new families of ISP products, as well as improve the performance and reduce the manufacturing cost of our existing product families based on market needs.

SOFTWARE DEVELOPMENT TOOLS

All Lattice ISP products are supported by ispDesignEXPERT-TM-, our fourth generation software development tool suite. Supporting both the PC and UNIX platforms, ispDesignEXPERT allows a customer to enter, verify and synthesize a design, perform logic simulation and timing analysis, assign I/O pins and critical speed paths, debug and floorplan a design, execute automatic place and route tasks and download a program to an ISP device. Seamlessly integrated with third-party electronic design automation, or EDA, environments, ispDesignEXPERT leverages customers' prior investments in products offered by Aldec, Cadence, Mentor Graphics, OrCAD, Synopsys, Synplicity, Viewlogic and Veribest. In the future, we plan to continue to enhance and expand the capability of our software development tool suite.

We also provide a variety of software algorithms that support in-system programming of our ISP devices via multiple formats and mechanisms. These software products include ispCODE-Registered Trademark-, Turbo ispDOWNLOAD-Registered Trademark-, ispREMOTE-TM-, ispATE-TM-, ispSVF-TM- and ispVM-TM-.

NON-ISP PRODUCTS

We offer the industry's broadest line of low-density CMOS PLDs based on our 20 families of GAL-Registered Trademark-and PALCE-Registered Trademark- products offered in over 200 speed, power, package and temperature range combinations. PALCE products were originally introduced by Vantis and are generally compatible with GAL products. GAL and PALCE devices range in complexity from approximately 200 to 1,000 logic gates and are typically assembled in 20-, 24- and 28-pin standard dual in-line packages and in 20- and 28-pin standard plastic leaded chip carrier packages. We offer standard 610, 16V8, 20V8 and 22V10 architectures in a variety of speed grades, with propagation delays as low as 3.5 nanoseconds, the highest performance in the industry. In addition, we offer several proprietary extension architectures, the 6001/2, 16VP8, 16V8Z, 18V10, 20VP8, 20V8Z, 22V10Z, 24V10, 29M16, 20RA10, 20XV10 and 26V12, each of which is optimized for specific applications. We also offer a full range of 3.3-volt standard architectures, the 16LV8, 20LV8, 22LV10 and 26CLV12, in a variety of speed grades, with propagation delays as low as 3.5 nanoseconds, the highest performance in the industry.

Our non-ISP products are supported by industry standard software and hardware development tools marketed by independent manufacturers specifically for PLD applications.

PRODUCT DEVELOPMENT

We place substantial emphasis on new product development and believe that continued investment in this area is required to maintain our competitive position. Our product development activities emphasize new proprietary ISP products, enhancement of existing products and process technologies and improvement of software development tools. Product development activities occur in Hillsboro, Oregon; Silicon Valley, California; Austin, Texas; Colorado Springs, Colorado; Corsham, England and Shanghai, China.

Research and development expenses were $32.0 million in fiscal year 1998, $33.2 million in fiscal year 1999 and $45.9 million for fiscal period 1999. We expect to continue to make significant future investments in research and development and expect our research and development expenses to approximately double with the acquisition of Vantis.

OPERATIONS

We do not manufacture our own silicon wafers and maintain strategic relationships with large semiconductor manufacturers to source our finished silicon wafers. This strategy allows us to focus our internal resources on product, process and market development, and eliminates the fixed cost of owning and operating manufacturing facilities. We are also able to take advantage of the ongoing advanced process technology dedicated development efforts of semiconductor manufacturers. In addition, all of our assembly operations are performed by outside suppliers. We perform certain test operations and reliability and quality assurance processes internally. We have achieved an ISO 9001 quality certification, an indication of our high internal operational standards.

WAFER FABRICATION

The majority of our silicon wafer requirements have historically been supplied by Seiko Epson in Japan pursuant to an agreement with EEA, an affiliated U.S. distributor of Seiko Epson. We negotiate wafer volumes, prices and terms with Seiko Epson and EEA on a periodic basis. We also receive silicon wafers from the UMC Group in Taiwan pursuant to a series of agreements entered into in 1995. Wafer prices and other purchase terms related to this commitment are subject to periodic adjustment. Currently, the substantial majority of the silicon wafers for Vantis products are manufactured by AMD pursuant to an agreement first entered into in 1996 and subsequently amended and restated at the time of our acquisition of Vantis. A significant interruption or shortage in our wafer supply or a significant or unexpected deterioration in wafer quality or yield levels achieved could have a material adverse effect on our business. See "--Licenses and Agreements."

ASSEMBLY

After wafer fabrication and initial testing, we ship wafers to independent subcontractors for assembly. During assembly, wafers are separated into individual die and encapsulated in plastic or ceramic packages. Presently, we have qualified long-term assembly partners in Hong Kong, Malaysia, the Philippines, Singapore, South Korea, Taiwan and Thailand.

TESTING

We electrically test the die on each wafer prior to shipment for assembly. Following assembly, prior to customer shipment, each product undergoes final testing and quality assurance procedures. Final testing on certain products is performed by independent contractors in Malaysia, the Philippines, South Korea, Taiwan, Thailand and the United States.

MARKETING, SALES AND CUSTOMERS

We sell our products directly to end customers through a network of independent manufacturers' representatives and indirectly through a network of independent distributors. We also employ a direct sales management and field applications engineering organization to support our end customers and indirect sales resources. Our end customers are primarily OEMs in the fields of communication, computing, industrial and military systems.

At January 1, 2000 we utilized 23 manufacturers' representatives and three distributors in North America. Arrow Electronics and Avnet provide full distribution coverage. We have also established export sales channels in over 30 foreign countries through a network of over 30 sales representatives and distributors. Approximately one-half of our North American sales and the majority of our export sales are made through distributors.

We protect each of our North American distributors and some of our foreign distributors against reductions in published prices, and expect to continue this policy in the foreseeable future. We also allow returns from these distributors of unsold products under certain conditions. For these reasons, we do not recognize revenue until products are resold by these distributors to an end customer.

We provide technical and marketing support to our end customers with engineering staff based at our headquarters, design centers and selected field sales offices. We maintain numerous domestic and international field sales offices in major metropolitan areas.

Export sales as a percentage of our total revenue were 51% in fiscal year 1998, 50% in fiscal year 1999 and 53% in fiscal period 1999. Both export and domestic sales are denominated in U.S. dollars, with the exception of sales to Japan, which are dominated in yen. If our export sales decline significantly there would be a material adverse impact on our business.

Our products are sold to a large and diverse group of customers. No individual end customer accounted for more than 10% of total revenue in fiscal year 1998 or 1999 or fiscal period 1999. No export sales to any individual country accounted for more than 10% of total revenue in fiscal years 1998 or 1999 or fiscal period 1999.

BACKLOG

Our backlog of scheduled and released orders as of January 1, 2000 was approximately $83.4 million as compared to approximately $63.5 million as of April 3, 1999. This backlog consists of direct OEM and distributor orders scheduled for delivery within the next 90 days. Distributor orders accounted for the majority of the backlog in both periods. Direct OEM customer orders may be changed, rescheduled or cancelled under certain circumstances without penalty prior to shipment. Additionally, distributor orders generally may be changed, rescheduled or cancelled without penalty prior to shipment. Furthermore,

distributor shipments are subject to rights of return and price adjustment. Revenue associated with distributor shipments is not recognized until the product is resold to an end customer. Typically, the majority of our revenue results from orders placed and filled within the same period. Such orders are referred to as "turns orders". By definition, turns orders are not captured in a backlog measurement made at the beginning of a period. We do not anticipate a significant change in this business pattern. For all these reasons, backlog as of any particular date should not be used as a predictor of revenue for any future period.

COMPETITION

The semiconductor industry is intensely competitive and characterized by rapid rates of technological change, product obsolescence and price erosion. Our current and potential competitors include a broad range of semiconductor companies from large, established companies to emerging companies, many of which have greater financial, technical, manufacturing, marketing and sales resources.

The principal competitive factors in the PLD market include product features, price, customer support, and sales, marketing and distribution strength. The availability of competitive software development tools is also critical. In addition to product features such as density, speed, power consumption, reprogrammability, design flexibility and reliability, competition in the PLD market occurs on the basis of price and market acceptance of specific products and technology. We believe that we compete favorably with respect to each of these factors. We intend to continue to address these competitive factors by working to continually introduce product enhancements and new products, by seeking to establish our products as industry standards in their respective markets, and by working to reduce the manufacturing cost of our products.

In the ISP PLD market, we primarily compete directly with Altera and Xilinx, both of whom offer competing products. We also compete indirectly with other PLD suppliers as well as other semiconductor companies who provide non-PLD based logic solutions. Although to date we have not experienced significant competition from companies located outside the United States, such companies may become a more significant competitive factor in the future. Competition may also increase as we and our current competitors seek to expand our markets. Any such increases in competition could have a material adverse effect on our operating results.

PATENTS

We seek to protect our products and wafer fabrication process technologies primarily through patents, trade secrecy measures, copyrights, mask work protection, trademark registrations, licensing restrictions, confidentiality agreements and other approaches designed to protect proprietary information. There can be no assurance that others may not independently develop competitive technology not covered by our intellectual property rights or that measures we take to protect our technology will be effective.

We hold numerous domestic, European and Japanese patents and have patent applications pending in the United States, Japan and Europe. There can be no assurance that pending patent applications or other applications that may be filed will result in issued patents, or that any issued patents will survive challenges to their validity. Although we believe that our patents have value, there can be no assurance that our patents, or any additional patents that may be issued in the future, will provide meaningful protection from competition. We believe that our success will depend primarily upon the technical expertise, experience, creativity and the sales and marketing abilities of our personnel.

Patent and other proprietary rights infringement claims are common in our industry. There can be no assurance that, with respect to any claim made against us, we could obtain a license on terms or under conditions that would not have a material adverse effect on our business.

LICENSES AND AGREEMENTS

SEIKO EPSON/EPSON ELECTRONICS AMERICA (EEA)

EEA, an affiliated U.S. distributor of Seiko Epson, has agreed to provide us with manufactured wafers in quantities based on six-month rolling forecasts. We have committed to buy certain minimum quantities of wafers per month. Wafers for our products are manufactured in Japan at Seiko Epson's wafer fabrication facilities and are delivered to us by EEA. Prices for the wafers obtained from EEA are reviewed and adjusted periodically.

In March 1997, we entered into an advance production payment agreement with Seiko Epson and EEA under which we agreed to advance approximately $85.0 million, payable upon completion of specific milestones, to Seiko Epson to finance construction of an eight-inch sub-micron semiconductor wafer manufacturing facility. The timing of the payments is related to certain milestones in the development of the facility. Under the terms of the agreement, the advance is to be repaid with semiconductor wafers over a multi-year period. The agreement calls for wafers to be supplied by Seiko Epson through EEA pursuant to purchase agreements concluded with EEA. We also have an option under the agreement to advance Seiko Epson an additional $60.0 million for additional wafer supply under similar terms. The first payment under this agreement, approximately $17.0 million, was made during fiscal 1997. During fiscal 1998, we made two additional payments aggregating approximately $34.2 million.

UMC GROUP

In September 1995, we entered into a series of agreements with UMC pursuant to which we agreed to join UMC and several other companies to form a separate Taiwanese company, UICC, for the purpose of building and operating an advanced semiconductor manufacturing facility in Taiwan. Under the terms of the agreement, we invested approximately $49.7 million between fiscal 1996 and fiscal 1998 for an approximate 10% equity interest in UICC and the right to purchase a percentage of the facility's wafer production at market prices.

In October 1996, we entered into an agreement with Utek Corporation, a public Taiwanese company in the wafer foundry business that became affiliated with the UMC Group in 1998, pursuant to which we agreed to make a series of equity investments in Utek under specific terms. In exchange for these investments we received the right to purchase a percentage of Utek's wafer production. Under this agreement we have invested approximately $17.5 million in three separate installments and currently own approximately 2.5 percent of the outstanding equity of Utek.

In June 1999, the board of directors of UICC and Utek and the board of directors of UMC voted in favor of merging UICC and Utek into UMC. These mergers became effective on January 3, 2000. After the mergers we own approximately 61 million shares of UMC common stock and have retained our capacity rights. Due to regulatory restrictions, the majority of our UMC shares may not be sold until July 2000. These regulatory restrictions will gradually expire between July 2000 and January 2004.

AMD

In June 1999, as part of our acquisition of Vantis, we entered into a series of agreements with AMD to support the continuing operations of Vantis.

AMD has agreed to provide us with finished silicon wafers through September 2003 in quantities based either on a rolling six-month or an annual forecast. We have committed to buy certain minimum quantities of wafers and AMD has committed to supply certain quantities of wafers during this period. Wafers for our products are manufactured in the United States at multiple AMD wafer fabrication facilities. Prices for these wafers will be reviewed and adjusted periodically.

We have also entered into an agreement with AMD pursuant to which we have cross-licensed Vantis patents with AMD patents, having an effective filing date on or before June 15, 1999, related to PLD products. This cross-license was made on a worldwide, non-exclusive and royalty-free basis.

As part of our acquisition of Vantis Corporation, we have acquired certain third-party license rights held by Vantis prior to the acquisition. Included are rights to use certain Xilinx patents to manufacture, market and sell products.

EMPLOYEES

As of January 1, 2000 we had 916 full-time employees. We believe that our future success will depend, in part, on our ability to continue to attract and retain highly skilled technical and management personnel. None of our employees is subject to a collective bargaining agreement. We have never experienced a work stoppage and consider our employee relations good.

ITEM 2. PROPERTIES

Our corporate headquarters are located in three connected buildings we own in Hillsboro, Oregon, comprising a total of approximately 200,000 square feet. We also own a 13,000 square foot research and development facility and approximately 6,000 square feet of dormitory facilities in Shanghai, China. We lease a 133,000 square foot facility in San Jose, California (through 2008); we expect to occupy this facility in 2000 in order to consolidate our existing Silicon Valley product development centers as described following. We currently lease a 80,000 square foot product development facility in Sunnyvale, California (through 2006), a 41,000 square foot product development facility in Milpitas, California (through February 14, 2001), a 40,000 square foot product development facility in Austin, Texas (through 2004) and a 7,000 square foot product development facility in Colorado Springs, Colorado (through 2004). We also lease, on a short-term basis, office facilities for our product development facility in the United Kingdom and for our domestic and international sales offices.

ITEM 3. LEGAL PROCEEDINGS

In connection with our acquisition of Vantis, we have agreed to assume both the claims against Altera and the claims by Altera against AMD in the case captioned ADVANCED MICRO DEVICES, INC. V. ALTERA CORPORATION (CASE NO. C-94-20567-RMW) proceeding in the United States District Court for the Northern District of California. This litigation, which began in 1994, involves multiple claims and counterclaims for patent infringement relating to Vantis and Altera programmable logic devices and both parties are seeking damages and injunctive relief.

In April 1999, the United States Court of Appeals for the Federal Circuit reversed earlier jury and District Court decisions and held that Altera is not licensed to the eight AMD patents-in-suit. These eight AMD patents were subsequently assigned to Vantis. Also in April 1999, following the decision of the Court of Appeals, Altera filed a petition for rehearing. In June 1999, the Court of Appeals denied Altera's petition for rehearing.

Although there can be no assurance as to the results of such litigation, based upon information presently known to management, we do not believe that the ultimate resolution of this lawsuit will have a material adverse effect on our business. The foregoing statement constitutes a forward-looking statement and the actual results may differ materially depending on a number of factors, including new court decisions and additional counterclaims made by other parties to such litigation.

Except as described above, we are not currently a party to any material legal proceedings.

ITEM 4. SUBMISSION OF MATTERS TO A VOTE OF SECURITY HOLDERS

Not applicable

ITEM 4(a). EXECUTIVE OFFICERS OF THE REGISTRANT

The following table sets forth certain information regarding our executive officers and directors:

NAME	AGE	POSITION
Cyrus Y. Tsui.....	54	President, Chief Executive Officer and Chairman of the Board
Steven A. Laub.....	41	Senior Vice President and Chief Operating Officer
Stephen A. Skaggs.....	37	Senior Vice President, Chief Financial Officer and Secretary
Frank J. Barone.....	60	Corporate Vice President, Product Operations
Stephen M. Donovan.....	49	Corporate Vice President, Sales
Jonathan K. Yu.....	59	Corporate Vice President, Business Development
Martin R. Baker.....	44	Vice President and General Counsel
Randy D. Baker.....	41	Vice President, Manufacturing
Albert L. Chan.....	50	Vice President and General Manager, Lattice Silicon Valley
Thomas J. Kingzett.....	53	Vice President, Reliability and Quality Assurance
Stanley J. Kopec.....	49	Vice President, Corporate Marketing
Andrew D. Robin.....	47	Vice President, New Venture Business
Rodney F. Sloss.....	56	Vice President, Finance
James V. Tortolano.....	50	Vice President and Co-General Counsel
Kenneth K. Yu.....	52	Vice President and Managing Director, Lattice Asia
Mark O. Hatfield.....	77	Director
Daniel S. Hauer.....	63	Director
Harry A. Merlo.....	75	Director
Larry W. Sonsini.....	59	Director
Douglas C. Strain.....	80	Director

CYRUS Y. TSUI joined Lattice in September 1988 as President, Chief Executive Officer and Director, and in March 1991 was named Chairman of the Board. From 1987 until he joined, Mr. Tsui was Corporate Vice President and General Manager of the Programmable Logic Division of AMD. He was Vice President and General Manager of the Commercial Products Divisions of Monolithic Memories Incorporated (MMI) from 1983 until its merger with AMD in 1987. Mr. Tsui has held technical and managerial positions in the semiconductor industry for over 30 years. He has worked in the programmable logic industry since its inception.

STEVEN A. LAUB joined Lattice in June 1990 as Vice President and General Manager. He was elected Senior Vice President and Chief Operating Officer in August 1996.

STEPHEN A. SKAGGS joined Lattice in December 1992 as Director, Corporate Development. He was elected Senior Vice President, Chief Financial Officer and Secretary in August 1996.

FRANK J. BARONE joined Lattice in June 1999 as a Corporate Vice President as a result of the Vantis acquisition. From September 1997 until he joined, Mr. Barone was Chief Operating Officer of Vantis. Prior thereto, Mr. Barone held various technical and managerial positions at AMD. He has worked in the programmable logic industry since 1978.

STEPHEN M. DONOVAN joined Lattice in October 1989 and has served as Director of Marketing and Director of International Sales. He was elected Vice President, International Sales in August 1993. He was

elected Corporate Vice President, Sales, in May 1998. Mr. Donovan has worked in the programmable logic industry since 1982.

JONATHAN K. YU joined Lattice in February 1992 as Vice President, Operations. He was elected Corporate Vice President, Business Development in August 1996. Mr. Yu has held technical and managerial positions in the semiconductor industry for over 30 years.

MARTIN R. BAKER joined Lattice in January 1997 as Vice President and General Counsel. From 1991 until he joined, Mr. Baker held legal positions with Altera Corporation.

RANDY D. BAKER joined Lattice in April 1985 as Manager, Manufacturing and was promoted in 1988 to Director, Manufacturing. He was elected Vice President, Manufacturing in August 1996.

ALBERT L. CHAN joined Lattice in May 1989 as California Design Center Manager and was promoted in 1991 to Director, California Product Development Center. He was elected Vice President, California Product Development in August 1993. He was elected Vice President and General Manager, Lattice Silicon Valley, in August 1997. Mr. Chan has worked in the programmable logic industry since 1983.

THOMAS J. KINGZETT joined Lattice in July 1992 as Director, Reliability and Quality Assurance. He was elected Vice President, Reliability and Quality Assurance in May 1998. Mr. Kingzett has worked in the semiconductor industry for over 25 years.

STANLEY J. KOPEC joined Lattice in August 1992 as Director, Marketing. He was elected Vice President, Corporate Marketing in May 1998. Mr. Kopec has worked in the programmable logic industry since 1985.

ANDREW D. ROBIN joined Lattice in June 1999 as Vice President, New Venture Business as a result of the Vantis acquisition. From March 1998 until he joined, Mr. Robin was Vice President, Marketing at Vantis. Prior thereto, Mr. Robin held various marketing and managerial positions at AMD and MMI. Mr. Robin has worked in the programmable logic industry since 1984.

RODNEY F. SLOSS joined Lattice in May 1994 as Vice President, Finance.

JAMES V. TORTOLANO joined Lattice in June 1999 as a Vice President as a result of the Vantis acquisition. From November 1998 until he joined, Mr. Tortolano was Vice President, General Counsel of Vantis. Prior thereto, Mr. Tortolano held various legal positions at AMD. He has worked in the semiconductor industry since 1983.

KENNETH K. YU joined Lattice in January 1991 as Director of Process Technology. He has served as Managing Director, Lattice Asia since November 1992 and was elected Vice President, Lattice Asia in August 1993. Mr. Yu has held technical and managerial positions in the semiconductor industry for over 25 years.

MARK O. HATFIELD has been a member of our board of directors since 1997. Mr. Hatfield is a former U.S. Senator from Oregon.

DANIEL S. HAUER has been a member of our board of directors since 1987. Mr. Hauer is the former Chairman and Chief Executive Officer of Epson Electronics America.

HARRY A. MERLO has been a member of our board of directors since 1983. Mr. Merlo is the President of Merlo Corporation and is the former President and Chairman of Louisiana-Pacific Corporation.

LARRY W. SONSINI has been a member of our board of directors since 1991. Mr. Sonsini is Chairman of the Executive Committee of Wilson Sonsini Goodrich & Rosati, Professional Corporation, a law firm based in Palo Alto, California.

DOUGLAS C. STRAIN has been a member of our board of directors since 1986. Mr. Strain is the founder and former Vice Chairman of Electro Scientific Industries, Inc.

PART II

ITEM 5. MARKET FOR THE REGISTRANT'S COMMON STOCK AND RELATED STOCKHOLDER MATTERS.

Our common stock is traded on the over-the-counter market and prices are quoted on the Nasdaq National Market under the symbol "LSCC". The following table sets forth the low and high sale prices for our common stock for the last two fiscal years and for the period since January 1, 2000. On March 16, 2000, the last reported sale price of our common stock was $68.063. As of March 16, 2000, we had approximately 370 stockholders of record.

	LOW	HIGH
Fiscal Year 1999:		
First Quarter	$12.813	$27.313
Second Quarter	11.625	18.313
Third Quarter	9.438	23.250
Fourth Quarter	18.875	28.156
Fiscal Period 1999:		
First Quarter	$19.031	$31.156
Second Quarter	26.938	34.625
Third Quarter	27.250	54.375
Fiscal 2000:		
First Quarter (through March 16, 2000)	$40.875	$79.063

All share amounts have been adjusted retroactively to reflect the two-for-one stock split effected in the form of a stock dividend of one share of common stock for each share of our outstanding common stock which was paid on September 16, 1999.

The payment of dividends on our common stock is within the discretion of the our Board of Directors. We intend to retain earnings to finance the growth of our business. We have not paid cash dividends and our Board of Directors does not expect to declare a cash dividend in the near future.

ITEM 6. SELECTED FINANCIAL DATA.

SELECTED FINANCIAL DATA

(IN THOUSANDS, EXCEPT PER SHARE DATA)

	NINE MONTHS ENDED DEC. 31, 1999	YEAR ENDED MAR. 31, 1999	MAR. 31, 1998	MAR. 31, 1997	MAR. 31, 1996
STATEMENT OF OPERATIONS DATA:					
Revenue	$269,699	$200,072	$245,894	$204,089	$198,167
Costs and expenses:					
Cost of products sold	108,687	78,440	98,883	83,736	82,216
Research and development	45,903	33,190	32,012	27,829	26,825
Selling, general and administrative	50,676	36,818	39,934	33,558	31,323
In-process research and development	89,003	--	--	--	--
Amortization of intangible assets	45,780	--	--	--	--
	340,049	148,448	170,829	145,123	140,364
(Loss) income from operations	(70,350)	51,624	75,065	58,966	57,803
Interest and other (expense) income, net	(4,120)	10,668	10,643	8,712	5,442
(Loss) income before (benefit) provision for income taxes	(74,470)	62,292	85,708	67,678	63,245
(Benefit) provision for income taxes	(27,989)	20,246	29,141	22,673	21,461
(Loss) income before extraordinary item	(46,481)	42,046	56,567	45,005	41,784
Extraordinary item, net of income taxes	(1,665)	--	--	--	--
Net (loss) income	$(48,146)	$ 42,046	$ 56,567	$ 45,005	$ 41,784
Basic (loss) income per share, before extraordinary item	$ (0.97)	$ 0.90	$ 1.22	$ 1.00	$ 1.03
Diluted (loss) income per share, before extraordinary item	$ (0.97)	$ 0.88	$ 1.18	$ 0.98	$ 1.00
Basic net (loss) income per share	$ (1.01)	$ 0.90	$ 1.22	$ 1.00	$ 1.03
Diluted net (loss) income per share	$ (1.01)	$ 0.88	$ 1.18	$ 0.98	$ 1.00
Shares used in per share calculations:					
Basic	47,714	46,974	46,478	44,920	40,654
Diluted	47,714	47,638	47,788	45,946	41,958
BALANCE SHEET DATA:					
Working capital	$152,758	$324,204	$283,678	$267,669	$244,649
Total assets	916,155	540,896	489,066	403,462	342,935
Stockholders' equity	482,773	483,734	434,686	360,491	298,768

	NINE MONTHS ENDED DEC. 31, 1999			YEAR ENDED MARCH 31, 1999			
	THIRD QUARTER	SECOND QUARTER	FIRST QUARTER	FOURTH QUARTER	THIRD QUARTER	SECOND QUARTER	FIRST QUARTER
UNAUDITED QUARTERLY DATA:							
Revenue	$114,988	$94,973	$ 59,738	$53,788	$50,168	$48,088	$48,028
Gross profit	$ 68,953	$55,202	$ 36,857	$33,045	$30,623	$29,045	$28,919
Income (loss) before extraordinary item	$ 9,652	$(4,970)	$(51,163)	$11,848	$10,513	$ 9,870	$ 9,816
Extraordinary item	$ (1,665)	--	--	--	--	--	--
Net income (loss)	$ 7,987	$(4,970)	$(51,163)	$11,848	$10,513	$ 9,870	$ 9,816
Net income per share:							
Basic income (loss) per share, before extraordinary item	$ 0.20	$ (0.10)	$ (1.08)	$ 0.25	$ 0.22	$ 0.21	$ 0.21
Diluted net income (loss) per share before extraordinary item	$ 0.19	$ (0.10)	$ (1.08)	$ 0.24	$ 0.22	$ 0.21	$ 0.20
Basic net income (loss) per share	$ 0.17	$ (0.10)	$ (1.08)	$ 0.25	$ 0.22	$ 0.21	$ 0.21
Diluted net income (loss) per share	$ 0.16	$ (0.10)	$ (1.08)	$ 0.24	$ 0.22	$ 0.21	$ 0.20

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All share and per share amounts have been adjusted retroactively to reflect the two-for-one stock split effected in the form of a stock dividend and paid on September 16, 1999.

ITEM 7. MANAGEMENT'S DISCUSSION AND ANALYSIS OF FINANCIAL CONDITION AND RESULTS OF OPERATIONS.

OVERVIEW

RESULTS OF OPERATIONS

The following table sets forth, for the periods indicated, the percentage of revenue represented by selected items reflected in our consolidated statement of operations:

	NINE MONTHS ENDED	YEAR ENDED	
	DEC. 31, 1999	MAR. 31, 1999	MAR. 31, 1998
Revenue	100%	100%	100%
Costs and expenses:			
Cost of products sold	40	39	40
Research and development	17	17	13
Selling, general and administrative	19	18	16
In-process research and development	33	--	--
Amortization of intangible assets	17	--	--
Total costs and expenses	126	74	69
(Loss) income from operations	(26)	26	31
Other (expense) income, net	(2)	5	4
(Loss) income before (benefit) provision for income taxes	(28)	31	35
(Benefit) provision for income taxes	(11)	10	12
(Loss) income before extraordinary item	(17)	21	23
Extraordinary item, net of income taxes	(1)	--	--
Net (loss) income	(18)	21	23

ACQUISITION OF VANTIS As discussed in Note 4 to the Consolidated Financial Statements, we completed the acquisition of Vantis Corporation ("Vantis") from AMD on June 15, 1999. We paid approximately $500.1 million in cash for all of the outstanding capital stock of Vantis, plus $10.8 million in indirect acquisition costs, we accrued $5.4 million for preacquistion contingencies, $8.3 million for exit costs, and recorded normal accruals of $34.5 million for the Vantis business. In addition, we exchanged Company stock options for all of the outstanding stock options under the former Vantis employee stock plans with a calculated Black-Scholes value of $24.0 million. Our aggregate purchase price for Vantis was $583.1 million. The purchase was financed using a combination of cash reserves and a new credit facility that was replaced with Convertible Notes in November 1999 (see Note 8 to the Consolidated Financial Statements.) The purchase price was allocated to the estimated fair value of assets acquired and liabilities assumed based on an independent appraisal and management estimates. In process research & development (IPR&D) costs were appraised at $89 million at the acquisition date using a methodology consistent with current views of the staff of the SEC. These IPR&D costs were charged to operations on the acquisition date. Remaining intangible asset costs of $422.6 million at the acquisition date are being amortized to operations over five years using the straight-line method. The purchase price and related allocation are subject to further refinement and change over the period covering one year from the acquisition date.

We have taken certain actions to integrate the Vantis operations and, in certain instances, to consolidate duplicative operations. Accrued exit costs related to Vantis were recorded as an adjustment to the fair value of net assets in the purchase price allocation. Accrued exit costs include $4.2 million related to Vantis office closures, $2.5 million related to separation benefits for Vantis employees and $1.1 million in other exit costs primarily relating to the termination of Vantis foreign distributors. Separation benefits relate primarily to twenty Vantis senior managers. At December 31, 1999, five employees from this group had terminated. As of December 31, 1999, an additional 55 Vantis employees had terminated for other merger-related reasons. Payments of approximately $747,000 have been charged to this accrued liability. If these employees had not terminated, substantially all of the related costs would have been charged to selling, general and administrative expenses. Charges to other exit cost accrued liabilities were not significant for the period from June 15, 1999 through December 31, 1999. There have been no non-cash charges or credits to accrued exit costs. These accruals are based upon our current estimates and are in accordance with Emerging Issues Task Force ("EITF") No. 95-3, "Recognition of Liabilities in Connection with a Purchase Business Combination."

REVENUE. Revenue was $269.7 million in fiscal period 1999, an increase of 35% from fiscal year 1999. Fiscal year 1999 revenue of $200.1 million represented a decrease of 19% from the $245.9 million recorded in fiscal year 1998.

In addition to our acquisition of Vantis, the revenue increase in fiscal period 1999 as compared to fiscal year 1999 was attributable to increased sales of ISP products and recovering demand from Asia. Fiscal year 1999 revenue as compared to fiscal 1998 was negatively impacted by a decline in demand from Asia due to the economic crisis in that region. Furthermore, revenue in all geographies was negatively impacted by a decline in demand for our non-ISP product families.

Our sales by geographic area were as follows:

	NINE MONTHS ENDED DEC. 31, 1999	YEAR ENDED MAR. 31, 1999	YEAR ENDED MAR. 31, 1998
		(IN THOUSANDS)	
United States	$126,333	$100,778	$120,278
Export sales:			
Europe	70,641	53,649	61,243
Asia	55,003	34,680	55,853
Other	17,722	10,965	8,520
	$269,699	$200,072	$245,894

Revenue from export sales as a percentage of total revenue was approximately 53% for fiscal period 1999, 50% for fiscal year 1999 and 51% for fiscal year 1998. We expect export sales to continue to represent a significant portion of revenue.

The average selling price of our products decreased slightly in fiscal period 1999 as compared to fiscal year 1999. The average selling price of our products was flat in fiscal year 1999 as compared to fiscal year 1998. The decrease in fiscal period 1999 was due primarily to changes in product mix. Although selling prices of mature products generally decline over time, this decline is at times offset by higher selling prices of new products. Our ability to maintain or increase the level of our average selling price is dependent on the continued development, introduction and market acceptance of new products.

GROSS MARGIN. Our gross margin was 60% for fiscal period 1999, 61% for fiscal year 1999 and 60% for fiscal year 1998. The gross margin decline in fiscal period 1999 as compared to fiscal year 1999 is attributable to our acquisition of Vantis on June 15, 1999. The decline was partially offset by an improvement in product mix and reductions in our manufacturing costs. The improvement in fiscal year 1999 as compared to fiscal year 1998 was primarily due to an improvement in product mix and reductions in our manufacturing costs. Reductions in manufacturing costs resulted primarily from yield improvements, migration of products to more advanced technologies and smaller die sizes, and wafer price reductions.

RESEARCH AND DEVELOPMENT. Research and development expense was $45.9 million in fiscal period 1999, $33.2 million in fiscal year 1999 and $32.0 million in fiscal year 1998. For fiscal period 1999, in addition to our acquisition of Vantis, spending increases resulted primarily from the increased development of new products. Spending increases in fiscal year 1999 as compared to fiscal year 1998 resulted primarily from the increased development of new products. We believe that a continued commitment to research and development is essential in order to maintain product leadership in our existing product families and provide innovative new product offerings, and therefore we expect to continue to make significant future investments in research and development.

SELLING, GENERAL AND ADMINISTRATIVE. Selling, general and administrative expense was $50.7 million in fiscal period 1999, $36.8 million in fiscal year 1999 and $39.9 million in fiscal year 1998. The increase in the 1999 fiscal period as opposed to fiscal year 1999 was primarily due to our Vantis acquisition and to a lesser extent attributable to increased variable costs associated with higher revenue levels. The decrease in fiscal year 1999 expense as compared to fiscal year 1998 was primarily due to decreased variable costs associated with lower revenue levels.

IN-PROCESS RESEARCH AND DEVELOPMENT. On June 15, 1999, we bought from AMD all of the outstanding capital stock of Vantis Corporation for approximately $500 million in cash in a transaction accounted for under the purchase method of accounting. Including liabilities assumed and purchase accounting reserves established, the total purchase cost was $583.1 million, of which $511.6 million was allocated to

intangible assets. A portion of the intangible asset value was in-process research and development, or IPR&D, with a value of approximately $89 million which was charged to expense on the acquisition date as required by generally accepted accounting principles. The remaining $422.6 million of intangible asset value consisting of existing technology, assembled workforce, customer lists, patents, trademarks and goodwill, is being amortized to operations over 5 years using the straight-line method.

AMORTIZATION OF INTANGIBLE ASSETS. Amortization of intangible assets acquired in the Vantis acquisition was $45.8 million for fiscal period 1999. The estimated weighted average useful life of the intangible assets for current technology, assembled workforce, customer lists, trademarks, patents and residual goodwill, created as a result of the acquisition, is approximately five years.

OTHER INCOME (EXPENSE), NET. Other income (expense), net, was ($4.1) million for fiscal period 1999, a $14.8 million decrease as compared to fiscal year 1999. This was primarily due to interest expense of approximately $9.7 million from acquisition related debt and reduced interest income resulting from lower cash and investment balances in conjunction with the acquisition. Other income (expense), net, was approximately flat for fiscal year 1999 as compared to fiscal year 1998, as higher cash and investment balances were offset by lower interest rates for invested balances, particularly in the second half of the fiscal year.

PROVISION FOR INCOME TAXES. The benefit for income taxes for fiscal period 1999 was 37.6% of the loss before benefit for income taxes. This reflects the estimated rate at which income taxes would be recoverable if a loss tax return were filed. The loss before benefit for income taxes is attributable to the IPR&D charge during the period of approximately $89.0 million and intangible asset amortization of $45.8 million. If these charges were not present, we would have had taxable income and an income tax rate of approximately 36.5%. Our effective tax rate was 32.5% for fiscal year 1999 and 34.0% for fiscal year 1998. The rate change in fiscal year 1999 as compared to fiscal year 1998 was due primarily to changes in the proportion of tax-exempt interest income included in our overall net income. The fiscal 1999 rate was also favorably impacted by reduced state taxes resulting from the increased realization of tax credits.

EXTRAORDINARY ITEM, NET OF INCOME TAXES. The extraordinary item, net of income taxes, represents the writeoff of unamortized loan fees related to the $220 million Term Loan repaid in conjunction with the financing of our acquisition of Vantis.

FACTORS AFFECTING FUTURE RESULTS

OUR WAFER SUPPLY COULD BE INTERRUPTED OR REDUCED AND RESULT IN A SHORTAGE OF FINISHED PRODUCTS AVAILABLE FOR SALE

We do not manufacture finished silicon wafers. Currently all of our silicon wafers are manufactured by Seiko Epson in Japan, AMD in the United States and the UMC Group, a group of affiliated companies, in Taiwan. If Seiko Epson, through its U.S. affiliate Epson Electronics America, AMD or the UMC Group significantly interrupts or reduces our wafer supply, our operating results would be adversely affected.

In the past, we have experienced delays in obtaining wafers and in securing supply commitments from our foundries. At present, we anticipate that our supply commitments are adequate. However, these existing supply commitments may not be sufficient for us to satisfy customer demand in future periods. Additionally, notwithstanding our supply commitments we may still have difficulty in obtaining wafer deliveries consistent with the supply commitments. We negotiate wafer prices and supply commitments from our suppliers on at least an annual basis. If Seiko Epson, Epson Electronics America, AMD or the UMC Group reduces our supply commitment or increases our wafer prices, and we cannot find alternative sources of wafer supply, our operating results could be adversely affected.

Many other factors that could disrupt our wafer supply are beyond our control. Since worldwide manufacturing capacity for silicon wafers is limited and inelastic, we could be adversely affected by

significant industry-wide increases in overall wafer demand or interruptions in wafer supply. Additionally, a future disruption of Seiko Epson's, AMD's or the UMC Group's foundry operations as a result of a fire, earthquake or other natural disaster could disrupt our wafer supply and could have an adverse effect on our operating results.

IF OUR FOUNDRY PARTNERS EXPERIENCE QUALITY OR YIELD PROBLEMS, WE MAY FACE A SHORTAGE OF FINISHED PRODUCTS AVAILABLE FOR SALE

We depend on our foundries to deliver reliable silicon wafers with acceptable yields in a timely manner. As is common in our industry, we have experienced wafer yield problems and delivery delays in the past. If our foundries are unable to produce silicon wafers that meet our specifications, with acceptable yields, for a prolonged period, our operating results could be adversely affected.

Substantially all of our revenue is derived from products based on a specialized silicon wafer manufacturing process technology called E(2)CMOS. The reliable manufacture of high performance E(2)CMOS semiconductor wafers is a complicated and technically demanding process requiring:

- a high degree of technical skill;
- state-of-the-art equipment;
- the absence of defects in the masks used to print circuits on a wafer;
- the elimination of minute impurities and errors in each step of the fabrication process; and
- effective cooperation between the wafer supplier and the circuit designer.

As a result, our foundries may experience difficulties in achieving acceptable quality and yield levels when manufacturing our silicon wafers.

WE MAY BE UNSUCCESSFUL IN DEFINING, DEVELOPING OR SELLING NEW PRODUCTS REQUIRED TO MAINTAIN OR EXPAND OUR BUSINESS

As a semiconductor company, we operate in a dynamic environment marked by rapid product obsolescence. Our future success depends on our ability to introduce new or improved products that meet customer needs while achieving acceptable margins. If we fail to introduce these new products in a timely manner or these products fail to achieve market acceptance, our business and financial condition will be adversely affected.

The introduction of new products in a dynamic market environment presents significant business challenges. Product development commitments and expenditures must be made well in advance of product sales. The success of a new product depends on accurate forecasts of long-term market demand and future technology developments.

Our future revenue growth is dependent on market acceptance of our new proprietary ISP product families and the continued market acceptance of our proprietary software development tools. The success of these products is dependent on a variety of specific technical factors including:

- successful product definition;
- timely and efficient completion of product design;
- timely and efficient implementation of wafer manufacturing and assembly processes;
- product performance; and
- the quality and reliability of the product.

If, due to these or other factors, our new products do not achieve market acceptance, our business and financial condition will be adversely affected.

OUR PRODUCTS MAY NOT BE COMPETITIVE IF WE ARE UNSUCCESSFUL IN MIGRATING OUR MANUFACTURING PROCESSES TO MORE ADVANCED TECHNOLOGIES

In order to develop new products and maintain the competitiveness of existing products, we need to migrate to more advanced wafer manufacturing processes that utilize larger wafer sizes and smaller device geometries. We may also utilize additional foundries. Since we depend upon foundries to provide their facilities and support for our process technology development, we may experience delays in the availability of advanced wafer manufacturing process technologies at existing or new wafer fabrication facilities. As a result, volume production of our advanced E(2)CMOS process technologies at the new fabs of Seiko Epson, the UMC Group or future foundries may not be achieved. This could have an adverse effect on our operating results.

IF OUR ASSEMBLY AND TEST SUBCONTRACTORS EXPERIENCE QUALITY OR YIELD PROBLEMS, WE MAY FACE A SHORTAGE OF FINISHED PRODUCTS AVAILABLE FOR SALE

We rely on subcontractors to assemble and test our devices with acceptable quality and yield levels. As is common in our industry, we have experienced quality and yield problems in the past. If we experience prolonged quality or yield problems in the future, there could be an adverse effect on our operating results.

The majority of our revenue is derived from semiconductor devices assembled in advanced packages. The assembly of advanced packages is a complex process requiring:

- a high degree of technical skill;

- state-of-the-art equipment;

- the absence of defects in lead frames used to attach semiconductor devices to the package;

- the elimination of raw material impurities and errors in each step of the process; and

- effective cooperation between the assembly subcontractor and the device manufacturer.

As a result, our subcontractors may experience difficulties in achieving acceptable quality and yield levels when assembling and testing our semiconductor devices.

WE MAY EXPERIENCE UNEXPECTED DIFFICULTIES DUE TO THE INTEGRATION OF VANTIS

We acquired Vantis on June 15, 1999, and at present have completed the integration of this business with our other operations. As a result of this acquisition and subsequent integration, we may incur unexpected disruptions to our ongoing business. These disruptions may have an adverse effect on our operations and financial results. Further, the following specific factors may adversely affect our ability to successfully operate the business of Vantis:

- we may experience unexpected losses of key employees or customers;

- we may experience unexpected costs and discover unexpected liabilities;

- we may not achieve historical levels of revenue growth, cost reduction and profitability improvement; and

- we may not be able to coordinate our new product and process development in a way which enables us to bring new technologies to the market in a timely manner.

In addition, as part of our acquisition of Vantis, we entered into arrangements with Vantis' former parent, AMD, for AMD to provide certain manufacturing support and services. In the event AMD fails to

provide these services, or provides such services at a level of quality and timeliness inconsistent with the historical delivery of such services, our ability to successfully operate Vantis will be severely hampered and our business may suffer.

DETERIORATION OF CONDITIONS IN ASIA MAY DISRUPT OUR EXISTING SUPPLY ARRANGEMENTS AND RESULT IN A SHORTAGE OF FINISHED PRODUCTS AVAILABLE FOR SALE

Two of our three silicon wafer suppliers operate fabs located in Asia. Our finished silicon wafers are assembled and tested by independent subcontractors located in Hong Kong, Malaysia, the Philippines, South Korea, Taiwan and Thailand. A prolonged interruption in our supply from any of these subcontractors could have an adverse effect on our operating results.

Although we have not experienced significant supply interruptions, the economic, financial, social and political situation in Asia has in the past been volatile. Financial difficulties, governmental actions or restrictions, prolonged work stoppages or any other difficulties experienced by our suppliers may disrupt our supply and could have an adverse effect on our operating results.

Our wafer purchases from Seiko Epson are denominated in Japanese yen. The value of the dollar with respect to the yen has fluctuated in the past and may not remain stable in the future. Future substantial deterioration of dollar-yen exchange rates could have an adverse effect on our operating results.

EXPORT SALES ACCOUNT FOR A SUBSTANTIAL PORTION OF OUR REVENUES AND MAY DECLINE IN THE FUTURE DUE TO ECONOMIC AND GOVERNMENTAL UNCERTAINTIES

Our export sales are affected by unique risks frequently associated with foreign economies including:

- changes in local economic conditions;

- exchange rate volatility;

- governmental controls and trade restrictions;

- export license requirements and restrictions on the export of technology;

- political instability;

- changes in tax rates, tariffs or freight rates;

- interruptions in air transportation; and

- difficulties in staffing and managing foreign sales offices.

For example, our export sales have in the past been affected by regional economic crises. Significant changes in the economic climate in the foreign countries where we derive our export sales could have an adverse effect on our operating results.

THE CYCLICAL NATURE OF THE SEMICONDUCTOR INDUSTRY MAY LIMIT OUR ABILITY TO MAINTAIN OR INCREASE REVENUE AND PROFIT LEVELS DURING FUTURE INDUSTRY DOWNTURNS

The semiconductor industry is highly cyclical, to a greater extent than other less dynamic or less technology-driven industries. In the past, our financial performance has been negatively affected by significant downturns in the semiconductor industry as a result of:

- the cyclical nature of the demand for the products of semiconductor customers;

- general reductions in inventory levels by customers;

- excess production capacity; and

- accelerated declines in average selling prices.

If these or other conditions in the semiconductor industry occur in the future, there could be an adverse effect on our operating results.

OUR FUTURE QUARTERLY OPERATING RESULTS MAY FLUCTUATE AND THEREFORE MAY FAIL TO MEET EXPECTATIONS

Our quarterly operating results have fluctuated in the past and may continue to fluctuate in the future. Consequently, our operating results may fail to meet the expectations of analysts and investors. As a result of industry conditions and the following specific factors, our quarterly operating results are more likely to fluctuate and are more difficult to predict than a typical non-technology company of our size and maturity:

- general economic conditions in the countries where we sell our products;

- the timing of our and our competitors' new product introductions;

- product obsolescence;

- the scheduling, rescheduling and cancellation of large orders by our customers;

- the cyclical nature of demand for our customers' products;

- our ability to develop new process technologies and achieve volume production at the new fabs of Seiko Epson and the UMC Group or at another foundry;

- changes in manufacturing yields;

- adverse movements in exchange rates, interest rates or tax rates; and

- the availability of adequate supply commitments from our wafer foundries and assembly and test subcontractors.

As a result of these factors, our past financial results are not necessarily a good predictor of our future results.

WE MAY NOT BE ABLE TO SUCCESSFULLY COMPETE IN THE HIGHLY COMPETITIVE SEMICONDUCTOR INDUSTRY

The semiconductor industry is intensely competitive and many of our direct and indirect competitors have substantially greater financial, technological, manufacturing, marketing and sales resources. If we are unable to compete successfully in this environment, our future results will be adversely affected.

The current level of competition in the programmable logic market is high and may increase as our market expands. We currently compete directly with companies that have licensed our products and technology or have developed similar products. We also compete indirectly with numerous semiconductor companies that offer products and solutions based on alternative technologies. These direct and indirect competitors are established multinational semiconductor companies as well as emerging companies. We also may experience significant competition from foreign companies in the future.

WE MAY FAIL TO RETAIN OR ATTRACT THE SPECIALIZED TECHNICAL AND MANAGEMENT PERSONNEL REQUIRED TO SUCCESSFULLY OPERATE OUR BUSINESS

To a greater degree than most non-technology companies or larger technology companies, our future success depends on our ability to attract and retain highly qualified technical and management personnel. As a mid-sized company, we are particularly dependent on a relatively small group of key employees. Competition for skilled technical and management employees is intense within our industry. As a result,

we may not be able to retain our existing key technical and management personnel. In addition, we may not be able to attract additional qualified employees in the future. If we are unable to retain existing key employees or are unable to hire new qualified employees, our operating results could be adversely affected.

IF WE ARE UNABLE TO ADEQUATELY PROTECT OUR INTELLECTUAL PROPERTY RIGHTS, OUR FINANCIAL RESULTS AND COMPETITIVE POSITION MAY SUFFER

Our success depends in part on our proprietary technology. However, we may fail to adequately protect this technology. As a result, we may lose our competitive position or face significant expense to protect or enforce our intellectual property rights.

We intend to continue to protect our proprietary technology through patents, copyrights and trade secrets. Despite this intention, we may not be successful in achieving adequate protection. Claims allowed on any of our patents may not be sufficiently broad to protect our technology. Patents issued to us also may be challenged, invalidated or circumvented. Finally, our competitors may develop similar technology independently.

Companies in the semiconductor industry vigorously pursue their intellectual property rights. If we become involved in protracted intellectual property disputes or litigation we may utilize substantial financial and management resources, which could have an adverse effect on our operating results. We may also be subject to future intellectual property claims or judgements. If these were to occur, we may not be able to obtain a license on favorable terms or without our operating results being adversely affected.

YEAR 2000 COMPLIANCE

During 1999 we completed our planned Year 2000 compliance activities with respect to our products, internal systems, software, equipment and facilities. In aggregate we spent approximately $2.0 million to fund Year 2000 compliance activities and related system and software upgrades. To date, we have not encountered any material Year 2000 problems with respect to our products, internal systems, software, equipment and facilities nor have we encountered any vendor supply disruptions related to Year 2000 problems.

OUR STOCK PRICE MAY CONTINUE TO EXPERIENCE LARGE SHORT-TERM FLUCTUATIONS

In recent years, the price of our common stock has fluctuated greatly. These price fluctuations have been rapid and severe and have left investors little time to react. The price of our common stock may continue to fluctuate greatly in the future due to a variety of company specific factors, including:

- quarter to quarter variations in our operating results;

- shortfalls in revenue or earnings from levels expected by securities analysts; and

- announcements of technological innovations or new products by other companies.

ITEM 7(a) QUANTITATIVE AND QUALITATIVE DISCLOSURES ABOUT MARKET RISK

As of December 31, 1999 and March 31, 1999 the Company's investment portfolio consisted of fixed income securities of $182.1 million and $293.4 million respectively. As with all fixed income instruments, these securities are subject to interest rate risk and will decline in value if market interest rates increase. If market rates were to increase immediately and uniformly by 10% from levels as of January 1, 2000 and April 3, 1999, the decline in the fair value of the portfolio would not be material. Further, the Company has the ability to hold its fixed income investments until maturity and, therefore, the Company would not expect to recognize such an adverse impact in income or cash flows.

The Company has international subsidiary and branch operations. Additionally, the majority of the Company's silicon wafer purchases are denominated in Japanese yen. The Company is therefore subject to foreign currency rate exposure. To mitigate rate exposure with respect to yen-denominated wafer purchases, the Company maintains yen-denominated bank accounts and bills its Japanese customers in yen. The yen bank deposits are utilized to hedge yen-denominated wafer purchases against specific and firm wafer purchases. If the foreign currency rates fluctuate by 10% from rates at January 1, 2000 and April 3, 1999, the effect on the company's consolidated financial statements would not be material. However, there can be no assurance that there will not be a material impact in the future.

LIQUIDITY AND CAPITAL RESOURCES

As of December 31, 1999, our principal source of liquidity was $214.1 million of cash and short-term investments, a decrease of $105.3 million from the balance of $319.4 million at March 31, 1999. The decrease was due to use of cash for our acquisition of Vantis partially offset by cash generated from operations and exercises of stock options. Working capital decreased $171.4 million to $152.8 million at December 31, 1999 from $324.2 million at March 31, 1999. This decrease in working capital was primarily a result of use of cash for our acquisition. During the nine months of fiscal period 1999, we generated approximately $80.9 million of cash and cash equivalents from our operating activities compared with $63.7 million during the twelve months of fiscal year 1999. In addition to the cash and cash equivalents generated, other changes in assets and liabilities are described below.

Accounts receivable at December 31, 1999 increased by $9.9 million, or 42%, as compared to the balance at March 31, 1999. This increase was primarily due to increased product shipments and revenue levels related to our acquisition. Inventories increased by $8.4 million, or 47%, as compared to the balance at March 31, 1999 primarily due to increased production in response to higher revenue levels and the inclusion of inventories related to our acquisition. Current deferred income taxes increased $15.3 million, or 106%, as compared to the balance at March 31, 1999 primarily due to the increase in deferred income for sales to distributors which is recognized currently for income tax purposes, and to a lesser extent the timing of deductions for certain expenses and allowances. Net property and equipment increased by $14.7 million, or 33%, as compared to the balance at March 31, 1999 primarily due to acquired assets. Long-term deferred income taxes increased $39.1 million versus the balance at March 31, 1999 and primarily represent future income tax benefits to be derived from the amortization for income tax purposes of the IPR&D charges which were written off in the first quarter of fiscal period 1999 for financial reporting purposes and the amortization of other intangible assets for tax purposes.

Accounts payable and accrued expenses increased by $66.1 million, or 355%, as compared to the balance at March 31, 1999 due primarily to the inclusion of liabilities related to our acquisition. Accrued payroll obligations increased by $5.3 million, or 39% as compared to the balance at March 31, 1999, due primarily to the inclusion of liabilities related to our acquisition. The $7.5 million, or 150% increase in income taxes payable as compared to the balance at March 31, 1999 is primarily attributable to the timing of tax deductions and payments. Deferred income increased by $25.2 million, or 126%, as compared to the balance at March 31, 1999, due primarily to increased billings to distributors associated with our acquisition.

On October 28, 1999, we issued $260 million in 4 3/4% convertible subordinated notes due on November 1, 2006. These notes require that we pay interest semi-annually on May 1 and November 1. Holders of these notes may convert them into shares of our common stock at any time on or before November 1, 2006, at a conversion price of $41.44 per share, subject to adjustment in certain events. Beginning on November 6, 2002 and ending on October 31, 2003, we may redeem the notes in whole or in part at a redemption price of 102.71% of the principal amount. In the subsequent three twelve-month periods, the redemption price declines to 102.04%, 101.36% and 100.68% of principal, respectively. The notes are subordinated in right of payment to all of our senior indebtedness, and are subordinated to all liabilities of our subsidiaries. At December 31, 1999, we had no senior indebtedness and our subsidiaries

had $26.5 million of other liabilities. Issuance costs relative to the convertible subordinated notes are included in other assets and aggregated approximately $6.9 million and are being amortized to expense over the lives of the notes. Accumulated amortization amounted to approximately $333,000 at December 31, 1999.

On June 15, 1999, we entered into a credit agreement with a group of lenders and ABN AMRO Bank N.V. ("ABN AMRO") as administrative agent for the lender group. The credit agreement consisted of two credit facilities: a $60 million unsecured revolving credit facility ("Revolver"), and a $220 million unsecured reducing term loan ("Term Loan"), both expiring and due on June 30, 2002. On June 15, 1999, we borrowed $220 million under the Term Loan and approximately $33 million under the Revolver. The credit facilities allowed for borrowings at adjustable rates with interest payments due quarterly. The $33 million Revolver was repaid in full during the third calendar quarter of 1999. In conjunction with the issuance of the convertible subordinated notes, we repaid the $220 million Term Loan in full during the fourth calendar quarter of fiscal 1999. Remaining unamortized loan fees at the time of repayment, aggregating approximately $2.6 million ($1.665 million net of income taxes or a charge of $0.04 for basic and diluted earnings per share), were written off and are reflected in our Consolidated Statement of Operations as an Extraordinary Item, Net of Income Taxes.

Capital expenditures were approximately $15.7 million, $18.4 million and $18.8 million for fiscal period 1999, and fiscal years 1999 and 1998, respectively. We expect to spend approximately $25 million to $30 million for the fiscal year ending December 31, 2000.

In March 1997, we entered into an advance payment production agreement with Seiko Epson and its affiliated U.S. distributor, Epson Electronics America, under which we agreed to advance approximately $85 million, payable upon completion of specific milestones, to Seiko Epson to finance construction of an eight-inch sub-micron wafer manufacturing facility. Under the terms of the agreement, the advance is to be repaid with semiconductor wafers over a multi-year period. The agreement calls for wafers to be supplied by Seiko Epson through Epson Electronics America, pursuant to purchase agreements with Epson Electronics America. We also have an option under this agreement to advance Seiko Epson an additional $60 million for additional wafer supply under similar terms. The first payment pursuant to this agreement, approximately $17.0 million, was made during fiscal 1997. During fiscal 1998, we made two additional payments aggregating approximately $34.2 million. The balance of the advance payment is currently anticipated to be made in two future installments.

We entered into a series of agreements with UMC, in September 1995 pursuant to which we agreed to join UMC and several other companies to form a separate Taiwanese company, UICC, for the purpose of building and operating an advanced semiconductor manufacturing facility in Taiwan. Under the terms of the agreements, we invested approximately $49.7 million for an approximate 10% equity interest in UICC and the right to receive a percentage of the facility's wafer production at market prices.

In October 1996, we entered into an agreement with Utek, a public Taiwanese company in the wafer foundry business that became affiliated with the UMC Group in 1998, pursuant to which we agreed to make a series of equity investments in Utek under specific terms. In exchange for these investments we received the right to purchase a percentage of Utek's wafer production. Under this agreement, we invested approximately $17.5 million in three separate installments.

In June 1999, the board of directors of UICC and board of directors of UMC voted in favor of merging UICC into UMC. These mergers became effective on January 3, 2000. After the mergers we own approximately 61 million shares of UMC common stock and have retained our capacity rights. Due to regulatory restrictions, the majority of our UMC shares may not be sold until July 2000. These regulatory restrictions will gradually expire between July 2000 and January 2004.

In June 1999, as part of our acquisition of Vantis, we entered into a series of agreements with AMD to support the continuing operations of Vantis. AMD has agreed to provide us with finished silicon wafers

through September 2003 in quantities based either on a rolling six-month or an annual forecast. We have committed to buy certain minimum quantities of wafers and AMD has committed to supply certain quantities of wafers during this period. Wafers for our products are manufactured in the United States at multiple AMD wafer fabrication facilities. Prices for these wafers will be reviewed and adjusted periodically.

We believe that our existing liquid resources, expected cash generated from operations and existing credit facilities combined with our ability to borrow additional funds will be adequate to meet our operating and capital requirements and obligations for the next 12 months.

In an effort to secure additional wafer supply, we may from time to time consider various financial arrangements including joint ventures, equity investments, advance purchase payments, loans, or similar arrangements with independent wafer manufacturers in exchange for committed wafer capacity. To the extent that we pursue any such additional financing arrangements, additional debt or equity financing may be required. We may in the future seek new or additional sources of funding. There can be no assurance that such additional financing will be available when needed or, if available, will be on favorable terms. Any future equity financing will decrease existing stockholders' equity percentage ownership and may, depending on the price at which the equity is sold, result in dilution.

ITEM 8. FINANCIAL STATEMENTS AND SUPPLEMENTARY DATA

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LATTICE SEMICONDUCTOR CORPORATION

CONSOLIDATED BALANCE SHEET

(IN THOUSANDS, EXCEPT SHARE AND PAR VALUE AMOUNTS)

	DEC. 31, 1999 (Note 1)	MARCH 31, 1999
ASSETS		
Current assets:		
Cash and cash equivalents	$113,824	$ 79,301
Short-term investments	100,316	240,133
Accounts receivable, net	33,676	23,788
Inventories (note 2)	26,036	17,683
Prepaid expenses and other current assets	10,407	6,061
Deferred income taxes (note 7)	29,727	14,400
Total current assets	313,986	381,366
Foundry investments, advances and other assets (notes 5 and 15)	130,274	114,537
Property and equipment, less accumulated depreciation (note 3)	59,689	44,993
Intangible assets, less accumulated amortization of $45,780 (note 4)	373,117	--
Deferred income taxes (note 7)	39,089	--
	$916,155	$540,896
LIABILITIES AND STOCKHOLDERS' EQUITY		
Current liabilities:		
Accounts payable and accrued expenses	$ 84,675	$ 18,611
Accrued payroll obligations	18,906	13,573
Income taxes payable (note 7)	12,459	4,985
Deferred income	45,188	19,993
Total current liabilities	161,228	57,162
4 3/4% Convertible notes due in 2006 (note 8)	260,000	--
Other long-term liabilities	12,154	--
Commitments and contingencies (notes 4,5,6,10,11 and 15)	--	--
Stockholders' equity (note 9):		
Preferred stock, $.01 par value, 10,000,000 shares authorized; none issued and outstanding	--	--
Common stock, $.01 par value, 100,000,000 shares authorized; 48,285,719 and 47,194,472 shares issued and outstanding	483	472
Paid-in capital	270,228	223,054
Retained earnings	212,062	260,208
	482,773	483,734
	$916,155	$540,896

The accompanying notes are an integral part of this statement.

LATTICE SEMICONDUCTOR CORPORATION

CONSOLIDATED STATEMENT OF OPERATIONS

(IN THOUSANDS, EXCEPT PER SHARE DATA)

	NINE MONTHS ENDED DEC. 31, 1999 (Notes 1 and 14)	YEAR ENDED MARCH 31, 1999	YEAR ENDED MARCH 31, 1998
Revenue	$269,699	$200,072	$245,894
Costs and expenses:			
Cost of products sold	108,687	78,440	98,883
Research and development	45,903	33,190	32,012
Selling, general and administrative (note 12)	50,676	36,818	39,934
In-process research and development (note 4)	89,003	--	--
Amortization of intangible assets (note 4)	45,780	--	--
	340,049	148,448	170,829
(Loss) income from operations	(70,350)	51,624	75,065
Other income (expense), net:			
Interest income	6,057	11,279	10,277
Interest expense (note 8)	(9,732)	(274)	--
Other (expense) income, net	(445)	(337)	366
(Loss) income before (benefit) provision for income taxes	(74,470)	62,292	85,708
(Benefit) provision for income taxes (note 7)	(27,989)	20,246	29,141
(Loss) income before extraordinary item	(46,481)	42,046	56,567
Extraordinary item, net of income taxes (note 8)	(1,665)	--	--
Net (loss) income	$(48,146)	$ 42,046	$ 56,567
Basic (loss) income per share, before extraordinary item	$ (0.97)	$ 0.90	$ 1.22
Diluted (loss) income per share, before extraordinary item	$ (0.97)	$ 0.88	$ 1.18
Basic net (loss) income per share	$ (1.01)	$ 0.90	$ 1.22
Diluted net (loss) income per share	$ (1.01)	$ 0.88	$ 1.18
Shares used in per share calculations:			
Basic	47,714	46,974	46,478
Diluted	47,714	47,638	47,788

The accompanying notes are an integral part of this statement.

LATTICE SEMICONDUCTOR CORPORATION

CONSOLIDATED STATEMENT OF CHANGES IN STOCKHOLDERS' EQUITY

(IN THOUSANDS, EXCEPT PAR VALUE)

	COMMON STOCK ($.01 PAR VALUE) SHARES	AMOUNT	PAID-IN CAPITAL	RETAINED EARNINGS	TOTAL
Balances, March 31, 1997	45,756	$458	$198,438	$161,595	$360,491
Common stock issued	1,100	11	12,540	--	12,551
Tax benefit of option exercises	--	--	5,225	--	5,225
Other comprehensive loss	--	--	(148)	--	(148)
Net income for fiscal year 1998	--	--	--	56,567	56,567
Balances, March 31, 1998	46,856	469	216,055	218,162	434,686
Common stock issued	1,014	10	11,202	--	11,212
Repurchase of common stock	(676)	(7)	(9,151)	--	(9,158)
Tax benefit of option exercises	--	--	4,888	--	4,888
Other comprehensive income	--	--	60	--	60
Net income for fiscal year 1999	--	--	--	42,046	42,046
Balances, March 31, 1999	47,194	472	223,054	260,208	483,734
Common stock issued	1,092	11	14,198	--	14,209
Fair value of options issued to Vantis employees	--	--	23,982	--	23,982
Tax benefit of option exercises	--	--	8,937	--	8,937
Other comprehensive income	--	--	57	--	57
Net loss for fiscal period 1999	--	--	--	(48,146)	(48,146)
Balances, December 31, 1999	48,286	$483	$270,228	$212,062	$482,773

The accompanying notes are an integral part of this statement.

LATTICE SEMICONDUCTOR CORPORATION

CONSOLIDATED STATEMENT OF CASH FLOWS

(IN THOUSANDS)

	NINE MONTHS ENDED DEC. 31, 1999	YEAR ENDED MAR. 31, 1999	YEAR ENDED MAR. 31, 1998
Cash flow from operating activities:			
Net (loss) income	$(48,146)	$42,046	$56,567
Adjustments to reconcile net (loss) income to net cash provided (used) by operating activities:			
Depreciation and amortization	57,842	10,064	9,558
In-process research and development costs	89,003	--	--
Deferred income taxes pertaining to intangible assets	(37,684)	--	--
Extraordinary item, net of income taxes	(1,665)	--	--
Changes in assets and liabilities (net of purchase accounting adjustments)			
Accounts receivable	(5,206)	4,441	(2,289)
Inventories	(884)	4,964	5,162
Prepaid expenses and other current assets	(387)	(489)	(2,654)
Deferred income taxes	(15,327)	100	(2,775)
Foundry investments, advances and other assets	769	(199)	(25,154)
Accounts payable and accrued expenses	2,054	415	3,920
Accrued payroll obligations	443	2,342	1,583
Income taxes payable	7,474	775	3,428
Deferred income	25,195	(750)	2,478
Other liabilities	7,443	--	--
Net cash provided by operating activities	80,924	63,709	49,824
Cash flow from investing activities:			
Proceeds from (purchase of) short-term investments, net	139,817	(33,367)	(32,068)
Acquisition of Vantis Corporation, net of cash acquired	(439,258)	--	--
Foundry investments	(4,593)	--	(10,164)
Capital expenditures	(15,675)	(18,387)	(18,825)
Net cash used by investing activities	(319,709)	(51,754)	(61,057)
Cash flow from financing activities:			
Proceeds from bank borrowings and convertible notes	513,000	--	--
Payments on bank borrowings	(253,000)	--	--
Debt issuance costs	(9,895)	--	--
Repurchase of common stock, net	--	(9,158)	--
Net proceeds from issuance of common stock	23,203	16,160	17,628
Net cash provided by financing activities	273,308	7,002	17,628
Net increase in cash and cash equivalents	34,523	18,957	6,395
Beginning cash and cash equivalents	79,301	60,344	53,949
Ending cash and cash equivalents	$113,824	$79,301	$60,344
Supplemental disclosure of non-cash investing and financing activities:			
Fair value of options issued to Vantis employees (note 4)	$ 23,982	--	--

The accompanying notes are an integral part of this statement.

(1)--NATURE OF OPERATIONS AND SIGNIFICANT ACCOUNTING POLICIES:

NATURE OF OPERATIONS

Lattice Semiconductor Corporation, ("Lattice"), founded in 1983 and based in Hillsboro, Oregon, designs, develops and markets the broadest range of high performance ISP-TM- programmable logic devices ("PLDs") and offers total solutions for today's advanced logic designs. We introduced in-system programmability to the logic industry in 1992. Our products are sold worldwide through an extensive network of independent sales representatives and distributors, primarily to OEM customers in the communications, computing, industrial and military end markets. Approximately one-half of our revenue is derived from export sales, mainly to Europe and Asia.

FISCAL REPORTING PERIOD

In the fourth quarter of calendar 1999, we changed our reporting period to a 52 or 53 week year ending on the Saturday closest to December 31 from a 52 or 53 week fiscal year ending on the Saturday closest to March 31. For ease of presentation, December 31 or March 31 has been utilized as the fiscal year end date for all financial statement captions. Additionally, for purposes of these consolidated financial statements, the nine-month fiscal period ended January 1, 2000 is referred to as "the nine months ended December 31, 1999" or "fiscal period 1999". The fiscal periods ended on April 3, 1999 and March 28, 1998, respectively, are referred to as "the fiscal year ended March 31, 1999" and "the fiscal year ended March 31, 1998", or "fiscal year 1999" and "fiscal year 1998", respectively. The fiscal year ended April 3, 1999 was a 53-week fiscal year. The nine-month period ended December 31, 1999 is not indicative of a full year (see note 14).

PRINCIPLES OF CONSOLIDATION

On June 15, 1999, we completed the acquisition of all of the outstanding capital stock of Vantis Corporation ("Vantis") from Advanced Micro Devices, Inc. ("AMD"). The transaction was accounted for as a purchase, and accordingly, the results of operations of Vantis and estimated fair value of assets acquired and liabilities assumed were included in our consolidated financial statements beginning June 16, 1999. The acquisition of Vantis is discussed further in note 4. There are no significant differences between our accounting policies and those of Vantis. The accompanying consolidated financial statements include the accounts of Lattice Semiconductor Corporation and its wholly owned subsidiaries after the elimination of all significant intercompany balances and transactions.

CASH EQUIVALENTS AND SHORT-TERM INVESTMENTS

We consider all highly liquid investments, which are readily convertible into cash and have original maturities of three months or less, to be cash equivalents. Short-term investments, which are relatively less liquid and have maturities of less than one year, are composed of corporate auction preferred stocks ($38.6 million), municipal and local government obligations ($17.8 million), Federal agency obligations ($8.1 million), time deposits ($16.8 million) and commercial paper ($19.0 million) at December 31, 1999.

We account for our short-term investments as held-to-maturity, which are stated at amortized cost with corresponding premiums or discounts amortized over the life of the investment to interest income. Amortized cost approximates market value at December 31, 1999.

(1)--NATURE OF OPERATIONS AND SIGNIFICANT ACCOUNTING POLICIES: (CONTINUED)

FINANCIAL INSTRUMENTS

All of our significant financial assets and liabilities are recognized in the Consolidated Balance Sheet as of December 31, 1999 and March 31, 1999. The carrying value of our financial instruments approximate current market value except foundry equity investments in Taiwan which were either not readily marketable or where market prices were not necessarily indicative of realizable value (see notes 5 and 15). We estimate the fair value of cash and cash equivalents, short-term investments, accounts receivable, other current assets and current liabilities based upon existing interest rates related to such assets and liabilities compared to the current market rates of interest for instruments of similar nature and degree of risk.

DERIVATIVE FINANCIAL INSTRUMENTS

In order to minimize exposure to foreign exchange risk with respect to long-term investments made with foreign currencies as further described in note 5 of notes to consolidated financial statements, we have at times entered into foreign forward exchange contracts in order to hedge these transactions. These contracts are accounted for as identifiable hedges against firm Lattice commitments. Realized gain or loss with respect to these contracts for the fiscal periods presented was not material. As of December 31, 1999, we had no open foreign exchange contracts for the purchase or sale of foreign currencies. We do not enter into derivative financial instruments for trading purposes.

FOREIGN EXCHANGE

The majority of our silicon wafer purchases are denominated in Japanese yen. We maintain yen-denominated bank accounts and bill our Japanese customers in yen. The yen bank deposits utilized to hedge yen-denominated wafer purchases are accounted for as identifiable hedges against specific and firm wafer purchases. Gains or losses from foreign exchange rate fluctuations on unhedged balances denominated in foreign currencies are reflected in other income. Realized and unrealized gains or losses were not significant for the fiscal periods presented.

CONCENTRATIONS OF CREDIT RISK

Financial instruments which potentially expose us to concentrations of credit risk consist primarily of short-term investments and trade receivables. We place our investments through several financial institutions and mitigate the concentration of credit risk by placing percentage limits on the maximum portion of the investment portfolio which may be invested in any one investment instrument. Investments consist primarily of A1 and P1 or better rated U.S. commercial paper, U.S. government agency obligations and other money market instruments, "AA" or better rated municipal obligations, money market preferred stocks and other time deposits. Concentrations of credit risk with respect to trade receivables are mitigated by a geographically diverse customer base and our credit and collection process. We perform credit evaluations for all customers and secure transactions with letters of credit or advance payments where necessary. Writeoffs for uncollected trade receivables have not been significant to date.

REVENUE RECOGNITION AND ACCOUNTS RECEIVABLE

Revenue from sales to OEM customers is recognized upon shipment. Certain of our sales are made to distributors under agreements providing price protection and right of return on unsold merchandise. Revenue and cost relating to such distributor sales are deferred until the product is sold by the distributor

(1)--NATURE OF OPERATIONS AND SIGNIFICANT ACCOUNTING POLICIES: (CONTINUED)
and related revenue and costs are then reflected in income. Accounts receivable are shown net of allowances for doubtful accounts of $1,583,000 and $881,000 at December 31, 1999 and March 31, 1999, respectively.

INVENTORIES

Inventories are stated at the lower of first-in, first-out cost or market.

LONG-LIVED ASSETS

We account for our long-lived assets in accordance with Statement of Financial Accounting Standards No. 121 (SFAS 121), "Accounting for the Impairment of Long-Lived Assets and for Long-Lived Assets to be Disposed of," which requires us to review the impairment of long-lived assets whenever events or changes in circumstances indicate that the carrying amount of an asset may not be recoverable. Impairment is measured by comparing the estimated undiscounted cash flows to the carrying amount.

PROPERTY AND EQUIPMENT

Property and equipment are stated at cost. Depreciation is computed using the straight-line method for financial reporting purposes over the estimated useful lives of the related assets, generally three to five years for equipment and software and thirty years for buildings. Accelerated methods of computing depreciation are generally used for income tax purposes.

INTANGIBLE ASSETS

Intangible assets consist of goodwill and other intangibles related to our acquisition of Vantis Corporation (see note 4) which are being amortized over five years on a straight-line basis, and fifteen years for income tax purposes. The undiscounted cash flows method is used to assess the carrying value of goodwill.

TRANSLATION OF FOREIGN CURRENCIES

We translate accounts denominated in foreign currencies in accordance with SFAS 52, "Foreign Currency Translation." Translation adjustments related to the consolidation of foreign subsidiary financial statements have not been significant to date.

RESEARCH AND DEVELOPMENT

Research and development costs are expensed as incurred.

STOCK-BASED COMPENSATION

We account for our employee and director stock options and employee stock purchase plan in accordance with provisions of Accounting Principles Board Opinion No. 25 ("APB 25"), "Accounting for Stock Issued to Employees." Additional pro forma disclosures as required under SFAS 123, "Accounting for Stock-Based Compensation," are presented in note 9.

(1)--NATURE OF OPERATIONS AND SIGNIFICANT ACCOUNTING POLICIES: (CONTINUED)
NET INCOME PER SHARE

Net income per share is computed based on the weighted average number of shares of common stock and common stock equivalents assumed to be outstanding during the period using the treasury stock method. Common stock equivalents consist of stock options and warrants to purchase common stock. The convertible notes issued in October 1999 (see note 8) are potentially dilutive securities. The incremental shares from assumed convertible note conversions are not included in computing the diluted per share amounts for fiscal period 1999 because there was a loss in this period. Thus, the inclusion of these shares would be antidilutive.

On August 11, 1999 our Board of Directors approved a two-for-one stock split of our common stock to be effected in the form of a stock dividend of one share of common stock for each share of our outstanding common stock. All share and per share amounts presented in the accompanying audited consolidated financial statements and notes thereto have been adjusted retroactively to reflect the two-for-one split.

The most significant difference between basic and diluted net income per share is that basic net income per share does not treat potentially dilutive securities such as convertible notes, options and warrants as outstanding. Diluted loss per common share for fiscal period 1999 is based only on the weighted average number of common shares outstanding during the period, as the inclusion of convertible notes, options and warrants would have been antidilutive. A reconciliation of the numerators and denominators of basic and diluted net income per share is presented below (in thousands, except for per share data):

	NINE MONTHS ENDED DEC. 31, 1999	YEAR ENDED MARCH 31, 1999	YEAR ENDED MARCH 31, 1998
Basic and diluted net (loss) income.....	$(48,146)	$42,046	$56,567
Shares used in basic net income per share calculations.....	47,714	46,974	46,478
Dilutive effect of stock options and warrants.....	--	664	1,310
Shares used in diluted net income per share calculations.....	47,714	47,638	47,788
Basic net (loss) income per share.....	$ (1.01)	$ .90	$ 1.22
Diluted net (loss) income per share.....	$ (1.01)	$ .88	$ 1.18

STATEMENT OF CASH FLOWS

Income taxes paid approximated $10.1 million, $16.4 million and $23.1 million in fiscal period 1999 and fiscal years 1999 and 1998, respectively. Interest paid aggregated approximately $6,871,000, $273,000 and $83,000 in fiscal period 1999 and fiscal years 1999 and 1998, respectively.

(1)--NATURE OF OPERATIONS AND SIGNIFICANT ACCOUNTING POLICIES: (CONTINUED)
USE OF ESTIMATES

The preparation of financial statements in conformity with generally accepted accounting principles requires management to make estimates and assumptions that affect the reported amounts of assets and liabilities and disclosure of contingent assets and liabilities at the date of the financial statements and the reported amounts of revenues and expenses during the fiscal periods presented. Actual results could differ from those estimates.

NEW ACCOUNTING PRONOUNCEMENTS

In June 1998, the FASB issued SFAS 133, "Accounting for Derivatives Instruments and Hedging Activities." SFAS 133 establishes new accounting treatment for derivatives and hedging activities and supersedes and amends a number of existing accounting standards. For Lattice, this pronouncement will be effective in 2001, and is not anticipated to have a material effect on the consolidated financial statements.

(2)--INVENTORIES (IN THOUSANDS):

	DEC. 31, 1999	MARCH 31, 1999
Work in progress	$14,009	$10,956
Finished goods	12,027	6,727
	$26,036	$17,683

(3)--PROPERTY AND EQUIPMENT (IN THOUSANDS):

	DEC. 31, 1999	MARCH 31, 1999
Land	$ 2,099	$ 2,099
Buildings	28,902	7,135
Construction in progress	--	18,768
Computer and test equipment	85,056	68,017
Office furniture and equipment	3,612	3,116
Leasehold and building improvements	6,625	2,643
	126,294	101,778
Accumulated depreciation and amortization	(66,605)	(56,785)
	$ 59,689	$ 44,993

(4)--ACQUISITION OF VANTIS:

On June 15, 1999, we paid approximately $500.1 million in cash to AMD for all of the outstanding capital stock of Vantis Corporation. Additionally, we paid approximately $10.8 million in direct acquisition costs, accrued an additional $5.4 million of pre-acquisition contingencies, accrued $8.3 million in exit costs and assumed certain liabilities of $34.5 million related to the Vantis business. This purchase was financed using a combination of cash reserves and a new credit facility bearing interest at adjustable rates (see note 8). In addition, we exchanged Lattice stock options for all of the options outstanding under the

(4)--ACQUISITION OF VANTIS: (CONTINUED)
former Vantis employee stock plans with a calculated Black-Scholes value of approximately $24.0 million. The total purchase price of Vantis was $583.1 million. The purchase price was allocated to the estimated fair value of assets acquired and liabilities assumed based on an independent appraisal and management estimates. The purchase price and the related allocation are subject to further refinement and change during the first half of 2000. The total purchase price was allocated as follows (in millions):

Current technology	$210.3
Excess of purchase price over net assets assumed	158.8
In-process research and development	89.0
Fair value of other tangible net assets	61.3
Assembled workforce, customer list, patents and trademarks	53.5
Fair value of property, plant and equipment	10.2
Total	$583.1

VANTIS INTEGRATION

We have taken certain actions to integrate the Vantis operations and, in certain instances, to consolidate duplicative operations. Accrued exit costs related to Vantis were recorded as an adjustment to the fair value of net assets in the purchase price allocation. Accrued exit costs include $4.2 million related to Vantis office closures, $2.5 million related to separation benefits for Vantis employees and $1.1 million in other exit costs primarily relating to the termination of Vantis foreign distributors. Separation benefits relate primarily to twenty Vantis senior managers. At December 31, 1999, five employees from this group had terminated. As of December 31, 1999, an additional 55 Vantis employees had terminated for other merger-related reasons. Payments of approximately $747,000 have been charged to this accrued liability. If these employees had not terminated, substantially all of the related costs would have been charged to selling, general and administrative expenses. Charges to other exit cost accrued liabilities were not significant for the period from June 15, 1999 through December 31, 1999. These accruals are based upon our current estimates and are in accordance with Emerging Issues Task Force ("EITF") No. 95-3, "Recognition of Liabilities in Connection with a Purchase Business Combination."

IN-PROCESS RESEARCH AND DEVELOPMENT ("IPR&D")

The value assigned to IPR&D was determined by identifying individual research projects for which technological feasibility had not been established. These include semiconductor projects with a value after application of the SEC's IPR&D valuation methodology of $77.2 million and a process technology project with a value of $11.8 million. The value of each project was determined by estimating the expected cash flows from the projects once commercially viable, applying a factor based on the stage of completion of each project so as to include only those cash flows that relate to development efforts prior to the acquisition date, and discounting the resulting net cash flows back to their present value. The percentage of completion for each project was determined using proportionate cost incurred and technical milestones achieved to date. The percentage of completion varied by individual project ranging from 50% to 69% for semiconductors on June 15, 1999. The process technology project was estimated to be 90% complete on June 15, 1999. Since June 15, 1999, there have been no significant changes in the assumptions underlying these valuations.

(4)--ACQUISITION OF VANTIS: (CONTINUED)

The nature of the efforts to develop the in-process research and development into commercially viable products for semiconductors principally relate to the completion of design, simulation, verification, documentation, test program development, prototyping, reliability testing and qualification, hardware and software integration as well as customer system-level testing and acceptance. For the process technology, the nature of the efforts required to establish the commercial viability of the in-process research and development project principally relate to transistor design, lithography and metalization process development, process integration, transistor size reduction plans, development of packaging integration technology, achievement of manufacturability goals, satisfaction of reliability standards and completion of qualification testing.

The semiconductor projects are related to new PLD products (requiring new architectures and process technologies) and have the attendant risks associated with development of advanced semiconductor circuit designs such as achievement of speed, power, density, reliability and cost goals. All of the semiconductor projects have remaining risks related to achievement of these design goals and effective software integration. In addition, certain projects have basic circuit design and layout activities which had not been completed as of June 15, 1999. These semiconductor projects are scheduled for market release during 2000 and continuing through 2001. Estimated costs to complete all in-process semiconductor projects total $19.0 million and range from $0.2 million to $16.5 million.

The process technology project is related to the development of a new advanced manufacturing process to reduce transistor size, improve speed and lower power consumption. Through June 15, 1999, transistor design, lithography and metalization process development, process integration and certain transistor size reduction plans had been achieved. Development of packaging integration technology, achievement of manufacturability yield objectives, satisfaction of reliability standards and qualification testing had not been accomplished at June 15, 1999. The process was qualified for initial production in the first quarter of 2000 with approximately $450,000 of costs incurred after June 15, 1999 out of a total of $4 million of estimated costs. This process technology, is expected to remain in production through 2004.

If the projects discussed above are not successfully developed, the future sales and profitability of the combined company may be adversely affected. Additionally, the value of other intangible assets acquired may become impaired. Management believes that the IPR&D charge of $89 million is valued consistently with the SEC staff's current views regarding valuation methodologies. There can be no assurances, however, that the SEC staff will not take issue with any assumptions used in our valuation model and require a revision in the amount allocated to IPR&D.

The estimated costs to develop the in-process research and development into commercially viable products at June 15, 1999 are approximately $19.4 million in aggregate--$4.7 million in 1999 subsequent to the transaction date, $10.0 million in 2000, and $4.7 million in 2001.

The net cash flows from each project are based on management's estimates of revenues, cost of sales, research and development costs, selling, general and administrative costs, and income taxes from such projects. These estimates are based on the below mentioned assumptions.

The estimated revenues are based on projected average compounded annual revenue growth rates for semiconductor products that are in line with industry analysts' forecasts of growth in the markets in which Vantis competes. Estimated total revenues from the in-process research and development product areas are expected to peak in the year 2005 and decline rapidly thereafter as replacement products are expected to enter the market. These projections are based on management estimates of market size and growth,

(4)--ACQUISITION OF VANTIS: (CONTINUED)
expected trends in technology, and the nature and expected timing of new product introductions by Vantis and its competitors.

In developing cash flow estimates, gross margins, research and development costs and selling general and administrative expenses were consistent with Vantis historical experience adjusted for expected changes in its stand-alone performance.

Vantis' management estimated a profit split from the in-process projects to the current products to account for the fact that Vantis' in-process projects are partially dependent on technology that has already established its feasibility. The profit split from each in-process product was estimated as a percentage of the total value of the in-process product which was attributable to existing Vantis core technology.

The net cash flows were discounted back to their present value based on the weighted average cost of capital (WACC). The WACC calculation estimates the rate of return required on an investment in an operating enterprise and considers the rates of return required from investments in various areas of that enterprise. The WACC assumed for Vantis, as a corporate business enterprise, is approximately 16%. The discount rate used in discounting the net cash flows from in-process research and development is 20% to 22%, which is 4% to 6% higher than the discount rate used in discounting the net cash flows from current technology. This discount rate is higher than the WACC due to the inherent uncertainties in the estimates described above including uncertainty surrounding the successful development of the in-process research and development projects, the useful life of such technology, the profitability levels of such technology and the uncertainty of technological advances that are unknown at this time.

USEFUL LIVES OF INTANGIBLE ASSETS

The estimated weighted average useful life of the intangible assets for current technology, assembled workforce, customer lists, trademarks, patents and residual goodwill, created as a result of the acquisition, is approximately five years.

PRO FORMA RESULTS

The following pro forma results of operations information is provided for illustrative purposes only and do not purport to be indicative of the consolidated results of operations for future periods or that actually would have been realized had Lattice and Vantis been a consolidated entity during the periods presented. These pro forma results do not include the effect of non-recurring purchase accounting adjustments. The pro forma results combine the results of operations as if Vantis had been acquired as of the beginning of the periods presented. The results include the impact of certain adjustments such as goodwill amortization, estimated changes in interest income (expense) related to cash outlays and

(4)--ACQUISITION OF VANTIS: (CONTINUED)
borrowings associated with the transaction (see note 8) and income tax benefits related to the aforementioned adjustments. Additionally, an in-process research and development charge of $89.0 million discussed above has been excluded from the periods presented due to its non-recurring nature:

	PRO FORMA RESULTS (UNAUDITED)	
	NINE MONTHS ENDED	
	DEC. 31, 1999	DEC. 31, 1998
	(IN THOUSANDS, EXCEPT PER-SHARE AMOUNTS)	
Revenue	$314,394	$295,057
Income (loss) before extraordinary item	$ 2,017	$(15,545)
Net income (loss)	$ 352	$(15,545)
Basic net income (loss) per share	$ 0.01	$ (0.33)
Diluted net income (loss) per share	$ 0.01	$ (0.33)

(5)--FOUNDRY INVESTMENTS, ADVANCES AND OTHER ASSETS (IN THOUSANDS):

	DECEMBER 31, 1999	MARCH 31, 1999
Foundry investments and other assets	$ 83,512	$ 63,275
Wafer supply advances	46,762	51,262
	$130,274	$114,537

We entered into a series of agreements with United Microelectronics Corporation ("UMC") in September 1995 pursuant to which we agreed to join UMC and several other companies to form a separate Taiwanese corporation, ("UICC"), for the purpose of building and operating an advanced semiconductor manufacturing facility in Taiwan, Republic of China. Under the terms of the agreements, we invested approximately $49.7 million between fiscal year 1996 and fiscal year 1998 for an approximate 10% equity interest in the corporation and the right to receive a percentage of the facility's wafer production at market prices. This investment is accounted for at cost.

In October 1996, we entered into an agreement with Utek Corporation, a public Taiwanese company in the wafer foundry business that became affiliated with the UMC group in 1998, pursuant to which we agreed to make a series of equity investments in Utek under specific terms. In exchange for these investments, we received the right to purchase a percentage of Utek's wafer production. Under this agreement, we have invested approximately $17.5 million in three separate installments and owned approximately 2.5% of the outstanding equity of Utek at December 31, 1999.

In June 1999, the Board of Directors of UICC and Utek and the Board of Directors of UMC voted in favor of merging UICC and Utek into UMC. These mergers became effective on January 3, 2000 (see note 15).

(5)--FOUNDRY INVESTMENTS, ADVANCES AND OTHER ASSETS (IN THOUSANDS): (CONTINUED)

In July 1994, we signed an agreement with Seiko Epson Corporation ("Seiko Epson") and its affiliated U.S. distributor, Epson Electronics America, Inc. ("EEA"), under which we advanced $44 million to be used to finance additional sub-micron wafer manufacturing capacity and technological development. The advance was completely repaid in the form of semiconductor wafers over a multi-year period ended in fiscal 1998.

In March 1997, we entered into a second advance payment production agreement with Seiko Epson and EEA under which we agreed to advance approximately $86 million, payable upon completion of specific milestones, to Seiko Epson to finance construction of an eight-inch sub-micron semiconductor wafer manufacturing facility. Under the terms of the agreement, the advance is to be repaid with semiconductor wafers over a multi-year period. No interest income is recorded. The agreement calls for wafers to be supplied by Seiko Epson through EEA pursuant to purchase agreements with EEA. We also have an option under the agreement to advance Seiko Epson an additional $60 million for additional wafer supply under similar terms. The first payment under this agreement, approximately $17.0 million, was made during fiscal 1997. During fiscal 1998, we made two additional payments aggregating approximately $34.2 million. Approximately $4.5 million of these advances are expected to be repaid with semiconductor wafers during fiscal year 2000 and are thus reflected as part of "Prepaid expenses and other current assets" in the accompanying Consolidated Balance Sheet.

(6)--LEASE OBLIGATIONS:

Certain of our facilities and equipment are leased under operating leases, which expire at various times through 2006. Rental expense under the operating leases was approximately $2,822,000, $1,200,000 and $1,026,000 for fiscal period 1999, and fiscal years 1999 and 1998, respectively. Future minimum lease commitments at December 31, 1999 are as follows (in thousands):

YEAR	
2000	$ 4,110
2001	2,921
2002	2,570
2003	2,434
2004	2,332
Later years	2,269
	$16,636

See note 15 describing a new operating lease commitment entered into in January 2000.

(7)--INCOME TAXES:

The components of the (benefit) provision for income taxes for fiscal period 1999, and fiscal years 1999 and 1998 are presented in the following table:

	NINE MONTHS ENDED DEC. 31, 1999	YEAR ENDED MARCH 31, 1999	YEAR ENDED MARCH 31, 1998
	(IN THOUSANDS)		
Current:			
Federal	$ 25,321	$18,678	$29,204
State	1,106	1,468	2,712
	26,427	20,146	31,916
Deferred:			
Federal	(52,180)	93	(2,539)
State	(2,236)	7	(236)
	(54,416)	100	(2,775)
	$(27,989)	$20,246	$29,141

Foreign income taxes were not significant for the fiscal periods presented.

The (benefit) provision for income taxes differs from the amount of income tax determined by applying the applicable U.S. statutory federal income tax rate to pretax income as a result of the following differences:

	NINE MONTHS ENDED DEC. 31, 1999	YEAR ENDED MARCH 31, 1999	YEAR ENDED MARCH 31, 1998
	(IN THOUSANDS)		
Computed income tax (benefit) expense at the statutory rate	$(26,064)	$21,802	$29,998
Adjustments for tax effects of:			
State taxes, net	(1,133)	1,478	2,402
Research and development credits	(400)	(270)	(154)
Nontaxable investment income	(1,113)	(3,037)	(3,009)
Other	721	273	(96)
	$(27,989)	$20,246	$29,141

(7)--INCOME TAXES: (CONTINUED)

The components of our net deferred tax assets are as follows (in thousands):

	DEC. 31, 1999	MARCH 31, 1999
Current deferred tax asset:		
Deferred income	$16,946	$ 7,547
Expenses and allowances not currently deductible	12,781	8,508
Total deferred tax assets	29,727	16,055
Valuation allowance	--	(1,655)
	$29,727	$14,400

	DEC. 31, 1999	MARCH 31, 1999
Non-current deferred tax asset:		
Intangible asset charges not currently deductible	$37,684	$ --
Expenses and allowances not currently deductible	1,405	--
Total deferred tax assets	$39,089	$ --

Prior to fiscal period 1999, we recorded valuation allowances to reduce deferred tax assets which could only be realized by earning taxable income in distant future years. We established the valuation allowances because we could not determine if it was more likely than not that such income would be earned. Management now believes that it is more likely than not that such taxable income will be earned, and therefore, no valuation allowance has been provided. The effect of this change in estimate was recorded in the first quarter of fiscal period 1999, and is included in the deferred tax benefit of $54.4 million for fiscal period 1999.

(8)--LONG-TERM DEBT:

On October 28, 1999, we issued $260 million in 4 3/4% convertible subordinated notes due on November 1, 2006. These notes pay interest semi-annually on May 1 and November 1. Holders of these notes may convert them into shares of our common stock at any time on or before November 1, 2006, at a conversion price of $41.44 per share, subject to adjustment in certain events. Beginning on November 6, 2002 and ending on October 31, 2003, we may redeem the notes in whole or in part at a redemption price of 102.71% of the principal amount. In the subsequent three twelve-month periods, the redemption price declines to 102.04%, 101.36% and 100.68% of principal, respectively. The notes are subordinated in right of payment to all of our senior indebtedness, and are subordinated by operation of law to all liabilities of our subsidiaries. At December 31, 1999, we had no senior indebtedness and our subsidiaries had $26.5 million of debt and other liabilities outstanding. Issuance costs relative to the convertible subordinated notes are included in other assets and aggregated approximately $6.9 million and are being amortized to expense over the lives of the notes. Accumulated amortization amounted to approximately $333,000 at December 31, 1999.

On June 15, 1999, we entered into a credit agreement with a group of lenders and ABN AMRO Bank N.V. ("ABN AMRO") as administrative agent for the lender group. The credit agreement consisted of two credit facilities: a $60 million unsecured revolving credit facility ("Revolver"), and a $220 million

(8)--LONG-TERM DEBT: (CONTINUED)
unsecured reducing term loan ("Term Loan"), both expiring and due on June 30, 2002. On June 15, 1999, we borrowed $220 million under the Term Loan and approximately $33 million under the Revolver. The credit facilities allowed for borrowings at adjustable rates with interest payments due quarterly. The $33 million Revolver was repaid in full during the third calendar quarter of 1999.

In conjunction with the issuance of the convertible subordinated notes, we repaid the $220 million Term Loan in full during the fourth calendar quarter of fiscal 1999. Remaining unamortized loan fees at the time of repayment, aggregating approximately $2.6 million ($1.665 million net of income taxes or a charge of $0.04 for basic and diluted earnings per share), were written off and are reflected in the accompanying Consolidated Statement of Operations as an Extraordinary Item, Net of Income Taxes.

9)--STOCKHOLDERS' EQUITY:

COMMON STOCK

On June 12, 1998, our Board of Directors authorized management to repurchase up to 2.4 million shares of our common stock. As of December 31, 1999, we had repurchased 675,000 shares at an aggregate cost of approximately $9.2 million.

STOCK WARRANTS

As of December 31, 1999, we issued warrants to purchase 1,376,484 shares of common stock to a vendor. Of this amount, 1,063,088 warrants were issued and 681,000 exercised prior to fiscal year 1998. During fiscal 1998, a warrant was issued to purchase 103,100 shares of common stock, earned ratably from March 1997 through February 1998. Additionally, the vendor exercised warrants for 247,250 shares at an average exercise price of $9.39 per share. During fiscal year 1999, a warrant was issued to purchase 100,196 shares of common stock, earned ratably from March 1998 to February 1999. During fiscal period 1999, a warrant was issued to purchase 110,100 shares of common stock, earned ratably from March 1999 to February 2000. Additionally, the vendor exercised warrants for 134,838 shares at $17.00 per share. Expense recorded in conjunction with the exercise of these warrants was not material.

STOCK OPTION PLANS

As of December 31, 1999, we had reserved 8,600,000 and 11,550,000 shares of common stock for issuance to officers and key employees under the 1996 Stock Option Plan and 1988 Stock Option Plan, respectively. The 1996 Plan options are granted at fair market value at the date of grant, generally vest over four years in increments as determined by the Board of Directors and have terms up to ten years. The 1988 Plan options are exercisable immediately and have terms up to ten years. The transfer of certain shares of common stock acquired through the exercise of 1988 Plan stock options is restricted under stock vesting agreements that grant us the right to repurchase unvested shares at the exercise price if employment is terminated. Generally, our repurchase rights lapse quarterly over four years. Additionally, on June 16, 1999, we exchanged 2,360,272 Lattice stock options for all of the options outstanding under the former Vantis stock option plans. These options generally vest over four years and have terms of ten years.

The 1993 Directors' Stock Option Plan provides for the issuance of stock options to members of our Board of Directors who are not employees of Lattice; 450,000 shares of our Common Stock are reserved for issuance thereunder. These options are granted at fair market value at the date of grant and generally

9)--STOCKHOLDERS' EQUITY: (CONTINUED)
become exercisable quarterly over a four year period beginning on the date of grant and expire five years from the date of grant.

The following table summarizes our stock option activity and related information for the past three fiscal periods (number of shares in thousands):

	NINE MONTHS ENDED DECEMBER 31, 1999		YEAR ENDED MARCH 31, 1999		YEAR ENDED MARCH 31, 1998	
	NUMBER OF SHARES UNDER OPTION	WEIGHTED-AVERAGE EXERCISE PRICE	NUMBER OF SHARES UNDER OPTION	WEIGHTED-AVERAGE EXERCISE PRICE	NUMBER OF SHARES UNDER OPTION	WEIGHTED-AVERAGE EXERCISE PRICE
Options outstanding at beginning of fiscal year.....	5,874	$15.71	5,512	$20.19	4,580	$13.75
Options granted.....	3,852	24.08	3,376	15.98	1,966	31.57
Options canceled.....	(536)	19.88	(2,136)	29.41	(268)	19.89
Options exercised.....	(968)	13.74	(878)	11.54	(766)	10.88
Options outstanding at end of fiscal year.....	8,222	$19.59	5,874	$15.71	5,512	$20.19

The following table summarizes information about stock options outstanding at December 31, 1999 (number of shares in thousands):

	OPTIONS OUTSTANDING			OPTIONS EXERCISABLE	
RANGE OF EXERCISE PRICES	NUMBER OF SHARES	WEIGHTED-AVERAGE REMAINING CONTRACT LIFE (IN YEARS)	WEIGHTED-AVERAGE EXERCISE PRICE	NUMBER OF SHARES	WEIGHTED-AVERAGE EXERCISE PRICE
$14.06-$15.49.....	973	0.61	$14.06	767	$14.06
$15.50-$15.74.....	1,737	2.86	15.50	419	15.50
$15.75-$18.49.....	1,916	1.65	16.23	1,048	16.55
$18.50-$29.74.....	2,131	3.30	20.92	511	20.08
$29.75-$42.75.....	1,465	3.42	30.57	157	31.49
	8,222	2.53	$19.59	2,902	$17.17

On November 10, 1998, we offered employees the choice of exchanging certain previously granted stock options for new stock options. The new stock options had an exercise price of $15.50, the fair value of our common stock on the date of exchange, and vest over four years. As a result, approximately 1,883,940 options were exchanged. The exchanged stock options had a weighted average exercise price of $30.73.

STOCK PURCHASE PLAN

Our employee stock purchase plan, most recently approved by the stockholders in August 1997, permits eligible employees to purchase shares of common stock through payroll deductions, not to exceed 10% of the employee's compensation. The purchase price of the shares is the lower of 85% of the fair

9)--STOCKHOLDERS' EQUITY: (CONTINUED)
market value of the stock at the beginning of each six-month period or 85% of the fair market value at the end of such period, but in no event less than the book value per share at the mid-point of each offering period. Amounts accumulated through payroll deductions during the offering period are used to purchase shares on the last day of the offering period. Of the 1,400,000 shares authorized to be issued under the plan, 98,614, 128,018 and 69,890 shares were issued during fiscal period 1999, fiscal years 1999 and 1998, respectively, and 319,096 shares were available for issuance at December 31, 1999.

PRO FORMA DISCLOSURES

We account for our stock options and employee stock purchase plan in conformity with APB 25 and have adopted the additional proforma disclosure provisions of SFAS 123. The fair value, as defined by SFAS 123, for stock options and employee stock plan purchase rights was estimated on the date of grant using the Black-Scholes option pricing model with the following assumptions:

	GRANTS FOR PERIODS ENDED		
	DEC. 31, 1999	MARCH 31, 1999	MARCH 31, 1998
Stock options:			
Expected volatility	41.4%	43.9%	48.6%
Risk-free interest rate	5.9%	4.7%	5.6%
Expected life from vesting date	1.6 years	1.3 years	1.2 years
Dividend yield	0%	0%	0%
Stock purchase rights:			
Expected volatility	52.8%	43.6%	36.0%
Risk-free interest rate	5.3%	4.8%	5.9%
Expected life	6 months	6 months	6 months
Dividend yield	0%	0%	0%

The Black-Scholes option pricing model was developed for use in estimating the fair value of freely tradable, fully transferable options without vesting restrictions. Our stock options have characteristics which differ significantly from those of freely tradable, fully transferable options. The Black-Scholes option pricing model also requires highly subjective assumptions, including expected stock price volatility and expected stock option term which greatly affect the calculated fair value of an option. Our actual stock price volatility and option term may be materially different from the assumptions used herein.

The resultant grant date weighted-average fair values calculated using the Black-Scholes option pricing model and the noted assumptions for stock options granted was $11.41, $5.19 and $12.60, and for stock purchase rights $7.74, $4.77 and $6.15, for fiscal period 1999, and fiscal years 1999 and 1998, respectively. For purposes of pro forma disclosures, the estimated fair value of the options is amortized to

9)--STOCKHOLDERS' EQUITY: (CONTINUED)
expense over the options' vesting period. Our pro forma information is as follows (in thousands, except per share data):

	NINE MONTHS ENDED DEC. 31, 1999	YEAR ENDED MARCH 31, 1999	YEAR ENDED MARCH 31, 1998
Pro forma net (loss) income	$(56,337)	$32,425	$48,777
Pro forma basic (loss) earnings per share	$ (1.18)	$ .69	$ 1.05
Pro forma diluted (loss) earnings per share	$ (1.18)	$ .68	$ 1.02

Because the SFAS 123 pro forma disclosure applies only to options granted subsequent to April 1, 1995, its pro forma effect will not be fully reflected until 2000.

SHAREHOLDER RIGHTS PLAN

A shareholder rights plan approved on September 11, 1991 provides for the issuance of one right for each share of outstanding common stock. With certain exceptions, the rights will become exercisable only in the event that an acquiring party accumulates beneficial ownership of 20% or more of the Company's outstanding common stock or announces a tender or exchange offer, the consummation of which would result in ownership by that party of 20% or more of the Company's outstanding common stock. The rights expire on September 11, 2001 if not previously redeemed or exercised. Each right entitles the holder to purchase, for $60.00, a fraction of a share of our Series A Participating Preferred Stock with economic terms similar to that of one share of our common stock. We will generally be entitled to redeem the rights at $0.01 per right at any time on or prior to the tenth day after an acquiring person has acquired beneficial ownership of 20% or more of our common stock. If, prior to the redemption or expiration of the rights, an acquiring person or group acquires beneficial ownership of 20% or more of the Company's our common stock, each right not beneficially owned by the acquiring person or group will entitle its holder to purchase, at the rights' then current exercise price, that number of shares of common stock having a value equal to two times the exercise price.

(10)--EMPLOYEE BENEFIT PLANS:

PROFIT SHARING PLAN

We initiated a profit sharing plan effective April 1, 1990. Under the provisions of this plan, as approved by the Board of Directors, a percentage of our operating income, as defined and calculated at the end of March and September for the prior six-month period, is paid to qualified employees. In fiscal period 1999, and fiscal years 1999 and 1998, approximately $2.6 million, $2.1 million and $3.0 million, respectively, was charged against operations in connection with the plan.

QUALIFIED INVESTMENT PLAN

In 1990, we adopted a 401(k) plan, which provides participants with an opportunity to accumulate funds for retirement. Under the terms of the plan, eligible participants may contribute up to 15% of their eligible earnings to the plan Trust. The plan allows for us to make discretionary matching contributions; no such contributions occurred through fiscal 1996. Beginning in fiscal 1997, we matched eligible employee

(10)--EMPLOYEE BENEFIT PLANS: (CONTINUED)
contributions of up to 5% of base pay. These matching contributions are discretionary and fully vest four years from the participants' hire date.

(11)--COMMITMENTS AND CONTINGENCIES:

We are exposed to certain asserted and unasserted potential claims. Patent and other proprietary rights infringement claims are common in the semiconductor industry. There can be no assurance that, with respect to potential claims made against us, that we could obtain a license on terms or under conditions that would not have a material adverse effect.

ADVANCED MICRO DEVICES, INC. V. ALTERA CORPORATION (CASE NO. C-94-20567-RMW, N.D. CAL.).

This litigation, which began in 1994, involves multiple claims and counterclaims for patent infringement relating to Vantis and Altera programmable logic devices. We assumed this litigation as part of our acquisition of Vantis. In April 1999, the Federal Court of Appeal reversed earlier jury and Court decisions and held that Altera is not licensed to the eight AMD patents-in-suit. These eight AMD patents were subsequently assigned to Vantis. Also in April 1999, following the decision of the Federal Court of Appeal, Altera filed a petition for rehearing. In June 1999, the Federal Court of Appeal denied Altera's petition for rehearing.

In connection with our acquisition of Vantis, we have agreed to assume both the claims against Altera and the claims by Altera against AMD. Although there can be no assurance as to the results of such litigation, based upon information presently known to management, we do not believe that the ultimate resolution of this lawsuit will have a material adverse effect on our consolidated results of operations, financial position, or cash flows.

(12)--RELATED PARTY:

Larry W. Sonsini is a member of our Board of Directors and is presently the Chairman of the Executive Committee of Wilson Sonsini Goodrich & Rosati, a law firm that provides us with corporate legal services. Legal services billed to Lattice aggregated approximately $1,086,000, $61,000 and $51,000, respectively, for fiscal period 1999, and fiscal years 1999 and 1998. Amounts payable to the law firm were not significant at December 31, 1999 or March 31, 1999.

(13)--SEGMENT AND GEOGRAPHIC INFORMATION:

We operate in one industry segment, programmable logic. Our sales by major geographic area were as follows:

	NINE MONTHS ENDED DEC. 31, 1999	YEAR ENDED MARCH 31, 1999	YEAR ENDED MARCH 31, 1998
	(IN THOUSANDS)		
United States	$126,333	$100,778	$120,278
Export sales:			
Europe	70,641	53,649	61,243
Asia	55,003	34,680	55,853
Other	17,722	10,965	8,520
	143,366	99,294	125,616
	$269,699	$200,072	$245,894

No individual customer accounted for more than 10% of revenue in fiscal period 1999, or fiscal years 1999 or 1998. Export sales to any individual country did not account for more than 10% of revenue in any of the fiscal periods presented. More than 90% of our property and equipment is located in the United States. Other long-lived assets located outside the United States consist primarily of foundry investments and advances (see note 5).

(14)--TRANSITION REPORTING:

The following table of selected consolidated financial data below provides a nine-month comparison of the results of operations through December 31, 1999 and 1998 (the transition period). The 1998 transition period figures are unaudited, however, we believe that all necessary adjustments have been made to make the periods comparable. Condensed consolidated results of operations for the comparable 1999 and 1998 nine-month periods are as follows:

	NINE MONTHS ENDED DEC. 31, 1999	NINE MONTHS ENDED DEC. 31, 1998
	(IN THOUSANDS, EXCEPT PER-SHARE AMOUNTS)	(UNAUDITED)
Revenue	$269,699	$146,284
Gross margin	$161,012	$ 88,587
(Benefit) provision for income taxes	$(27,989)	$ 14,541
Extraordinary item, net of income taxes	$ (1,665)	$ --
Net (loss) income	$(48,146)	$ 30,199
Basic net (loss) income per share	$ (1.01)	$ 0.65
Diluted net (loss) income per share	$ (1.01)	$ 0.64

(15)--SUBSEQUENT EVENTS:

On January 4, 2000, we announced that we will recognize a $150 million pre-tax ($92 million after-tax) gain in our Consolidated Statement of Operations for the first calendar quarter of 2000. The gain

(15)--SUBSEQUENT EVENTS: (CONTINUED)
represents appreciation of foundry investments made in two Taiwanese companies, UICC and Utek (see note 5). Effective January 3, 2000, UICC and Utek merged with UMC, a publicly traded Taiwanese company. As a result of this merger, Lattice now owns approximately 61 million shares of UMC common stock. Due to regulatory restrictions, the majority of our UMC shares may not be sold until July 2000. These regulatory restrictions will gradually expire between July 2000 and January 2004. As the regulatory restrictions expire and if we liquidate our UMC shares, it is likely that the amount of any future realized gain will be different from the accounting gain to be reported in the first calendar quarter of 2000.

In January 2000, we signed an agreement to lease and occupy two buildings, comprising approximately 133,000 square feet, in San Jose, California. This space will house our Silicon Valley product and software development groups as well as certain administrative services. The lease term commences in May 2000 and ends in December 2008. The lease agreement provides specified allowances for tenant improvements. Future minimum lease commitments related to this agreement aggregate approximately $25.6 million, payable in monthly installments.

REPORT OF INDEPENDENT ACCOUNTANTS

To the Board of Directors and Stockholders of
Lattice Semiconductor Corporation

In our opinion, the accompanying consolidated balance sheet and the related consolidated statements of operations, of changes in stockholders' equity and of cash flows present fairly, in all material respects, the financial position of Lattice Semiconductor Corporation and its subsidiaries at December 31, 1999 and March 31, 1999, and the results of their operations and their cash flows for the nine months ended December 31, 1999 and for each of the two years in the period ended March 31, 1999 in conformity with accounting principles generally accepted in the United States. These financial statements are the responsibility of the Company's management; our responsibility is to express an opinion on these financial statements based on our audits. We conducted our audits of these statements in accordance with auditing standards generally accepted in the United States, which require that we plan and perform the audit to obtain reasonable assurance about whether the financial statements are free of material misstatement. An audit includes examining, on a test basis, evidence supporting the amounts and disclosures in the financial statements, assessing the accounting principles used and significant estimates made by management, and evaluating the overall financial statement presentation. We believe that our audits provide a reasonable basis for the opinion expressed above.

/s/ PRICEWATERHOUSECOOPERS LLP

Portland, Oregon
January 19, 2000

ITEM 9.CHANGES IN AND DISAGREEMENTS WITH ACCOUNTANTS ON ACCOUNTING AND FINANCIAL DISCLOSURE.

Not applicable.

With the exception of the information expressly incorporated by reference from the Annual Report to Stockholders into Parts II and IV of this Form 10-K, the Company's Annual Report to Stockholders is not to be deemed filed as part of this Report.

PART III

Certain information required by Part III is omitted from this Report in that the Company will file its definitive proxy statement for the Annual Meeting of Stockholders to be held on May 2, 2000, pursuant to Regulation 14A of the Securities Exchange Act of 1934 (the "Proxy Statement"), not later than 120 days after the end of the fiscal year covered by this Report, and certain information included in the Proxy Statement is incorporated herein by reference. With the exception of the information expressly incorporated by reference from the Proxy Statement, the Company's Proxy Statement is not to be deemed filed as a part of this report.

ITEM 10. DIRECTORS AND EXECUTIVE OFFICERS OF THE REGISTRANT.

The information required by this Item with respect to directors of the Company is included under "Proposal 1: Election of Directors" in the Company's Proxy Statement, which information is incorporated herein by reference. Information with respect to executive officers of the Company is included under Item 4(a) of Part I of this Report and is incorporated herein by reference.

ITEM 11. EXECUTIVE COMPENSATION.

The information required by this Item with respect to executive compensation is included under "Proposal 1: Election of Directors--Directors," "Executive Compensation" and "Comparison of Total Cumulative Stockholder Return" in the Company's Proxy Statement, which information is incorporated herein by reference.

ITEM 12. SECURITY OWNERSHIP OF CERTAIN BENEFICIAL OWNERS AND MANAGEMENT.

The information required by this Item is included in the Company's Proxy Statement under the caption "Security Ownership of Certain Beneficial Owners and Management", which information is incorporated herein by reference.

ITEM 13. CERTAIN RELATIONSHIPS AND RELATED TRANSACTIONS.

The information required by this Item is included under "Proposal 1: Election of Directors--Transactions with Management" in the Company's Proxy Statement, which information is incorporated herein by reference.

PART IV

ITEM 14. EXHIBITS, FINANCIAL STATEMENT SCHEDULES AND REPORTS ON FORM 8-K.

(a)(1) AND (2) FINANCIAL STATEMENTS AND FINANCIAL STATEMENT SCHEDULES.

The information required by this Item is included under Item 8 of this Report.

(a)(3) EXHIBITS.

3.1	The Company's Certificate of Incorporation, as amended (including (i) the Company's Certificate Eliminating Matters set forth in Certificates of Designation with respect to Series A, Series B, Series D and Series E dated February 15, 1990; (ii) the Company's Restated Certificate of Incorporation, as amended, incorporated by reference to Exhibit 3.1 filed with the Company's Annual Report on Form 10-K for the fiscal year ended March 31,1990; (iii) the Company's Certificate of Designation of Rights, Preferences and Privileges of Series A participating Preferred Stock incorporated by reference to Exhibit 1 filed with the Company's Registration Statement on Form 8-A on September 13, 1991; and (iv) the Certificate of Amendment, dated September 8, 1993, of the Company's Certificate of Incorporation (Incorporated by reference to Exhibit 3.1 filed with the Company's Annual Report on Form 10-K for the fiscal year ended April 3, 1999).
3.2	The Company's Bylaws, as amended (including (i) the Company's Amended Bylaws, incorporated by reference to Exhibit 3.2 filed with the Company's Annual Report on Form 10-K for the fiscal year ended March 30, 1991; (ii) Amendment to the Company's Bylaws authorized by the Board of Directors on May 24, 1991 (Incorporated by reference to Exhibit 3.1 filed with the Company's Annual Report on Form 10-K for the fiscal year ended April 3, 1999); (iii) Amendment to the Company's Bylaws authorized by the Board of Directors on May 16, 1995 (Incorporated by reference to Exhibit 3.1 filed with the Company's Annual Report on Form 10-K for the fiscal year ended April 3, 1999); and (iv) Amendment to the Company's Bylaws authorized by the Board of Directors on February 4, 1997 (Incorporated by reference to Exhibit 3.1 filed with the Company's Annual Report on Form 10-K for the fiscal year ended April 3, 1999).
4.1	Preferred Shares Rights Agreement dated as of September 11, 1991 between Lattice Semiconductor Corporation and First Interstate Bank of Oregon, N.A., as Rights Agent (Incorporated by reference to Exhibit 1 filed with the Company's Registration Statement on Form 8-A on September 13, 1991).
10.9*	Lattice Semiconductor Corporation 1988 Stock Incentive Plan, as amended (Incorporated by reference to Exhibit 10.9 filed with the Company's Annual Report on Form 10-K for the fiscal year ended March 28, 1992).
10.10*	Form of Stock Option Agreement (Incorporated by reference to Exhibit 10.9, File No. 33-31231).
10.11*	Employment Letter dated September 2, 1988 from Lattice Semiconductor Corporation to Cyrus Y. Tsui (Incorporated by reference to Exhibit 10.10, File No. 33-31231).
10.12	Form of Proprietary Rights Agreement (Incorporated by reference Exhibit 10.11, File No. 33-31231).
10.13*	Outside Directors Compensation Plan (Incorporated by reference to Exhibit 10.12, File No. 33-31231).
10.15*	1993 Outside Directors Stock Option Plan (Incorporated by reference to Exhibit 10.15 filed with the Company's Annual Report on Form 10-K for the fiscal year ended April 3, 1993).
10.16*	Employee Stock Purchase Plan, as amended (Incorporated by reference to Exhibit 10.16 filed with the Company's Annual Report on Form 10-K for the fiscal year ended April 3, 1993).
10.19	Bridge Capacity Letter dated September 12, 1995 between Lattice Semiconductor Corporation and United Microelectronics Corporation. (Incorporated by reference to Exhibit 10.1 filed with the Company's Current Report on Form 8-K dated September 28, 1995)(1).

10.20	Foundry Venture Side Letter dated September 13, 1995 among Lattice Semiconductor Corporation, United Microelectronics Corporation and FabVen (Incorporated by reference to Exhibit 10.2 filed with the Company's Current Report on Form 8-K dated September 28, 1995)(1).
10.21	FabVen Foundry Capacity Agreement dated as of August , 1995 among FabVen, United Microelectronics Corporation and Lattice Semiconductor Corporation (Incorporated by reference to Exhibit 10.3 filed with the Company's Current Report on Form 8-K dated September 28, 1995)(1).
10.22	Foundry Venture Agreement dated as of August , 1995, between Lattice Semiconductor Corporation and United Microelectronics Corporation (Incorporated by reference to Exhibit 10.4 filed with the Company's Current Report on Form 8-K dated September 28, 1995)(1).
10.23	Advance Production Payment Agreement dated March 17, 1997 among Lattice Semiconductor Corporation and Seiko Epson Corporation and S MOS Systems, Inc. (Incorporated by reference to Exhibit 10.23 filed with the Company's Annual Report on Form 10-K for the fiscal year ended March 29, 1997)(1).
10.24*	Lattice Semiconductor Corporation 1996 Stock Incentive Plan (Incorporated by reference to Exhibit 4.1 filed on Form S-8 dated November 7, 1996).
10.26	Stock Purchase Agreement dated as of April 21, 1999 by and between Lattice Semiconductor Corporation and Advanced Micro Devices, Inc. (Incorporated by reference to Exhibit 2.1 filed with the Company's Current Report on Form 8-K dated April 21, 1999).
10.27	First Amendment to Stock Purchase Agreement dated as of June 7, 1999 entered into by and between Lattice Semiconductor Corporation and Advanced Micro Devices, Inc. (Incorporated by reference to Exhibit 10.27 filed with the Company's Annual Report on Form 10-K for the fiscal year ended April 3, 1999).
10.28	Second Amendment to Stock Purchase Agreement dated as of June 15, 1999 entered into by and between Lattice Semiconductor Corporation and Advanced Micro Devices, Inc. (Incorporated by reference to Exhibit 10.28 filed with the Company's Annual Report on Form 10-K for the fiscal year ended April 3, 1999).
10.29	Amended and Restated Wafer Fabrication Agreement dated April 21, 1999 (and subsequently amended on September 24, 1999 and February 18, 2000) by and between Advanced Micro Devices, Inc. and Vantis Corporation(1).
11.1	Computation of Net Income Per Share(2).
21.1	Subsidiaries of the Registrant.
23.1	Consent of Independent Accountants.
24.1	Power of Attorney (see page 54).
27.1	Financial Data Schedule for Fiscal Period Ended January 1, 2000.

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(1) Pursuant to Rule 24b-2 under the Securities Exchange Act of 1934, confidential treatment has been granted to portions of this exhibit, which portions have been deleted and filed separately with the Securities and Exchange Commission.

(2) Incorporated by reference to Note 1 to the Consolidated Financial Statements in the Company's Annual Report to Stockholders for the fiscal period ended January 1, 2000.

* Management contract or compensatory plan or arrangement required to be filed as an Exhibit to this Annual Report on Form 10-K pursuant to Item 14(c) thereof.

SIGNATURES

Pursuant to the requirements of Section 13 or 15(d) of the Securities Exchange Act of 1934, the Registrant has duly caused this Report to be signed on its behalf by the undersigned, thereunto duly authorized, in the City of Hillsboro, State of Oregon, on the 27th of March, 2000.

LATTICE SEMICONDUCTOR CORPORATION

By: /s/ STEPHEN A. SKAGGS
Stephen A. Skaggs,
SENIOR VICE PRESIDENT, CHIEF FINANCIAL OFFICER AND SECRETARY

POWER OF ATTORNEY

KNOW ALL PERSONS BY THESE PRESENTS, that each person whose signature appears below constitutes and appoints Cyrus Y. Tsui and Stephen A. Skaggs, jointly and severally, his attorneys-in-fact, each with the power of substitution, for him in any and all capacities, to sign any amendments to this Report on Form 10-K, and to file the same, with exhibits thereto and other documents in connection therewith, with the Securities and Exchange Commission, hereby ratifying and confirming all that each of said attorneys-in-fact, or his substitute or substitutes, may do or cause to be done by virtue hereof.

Pursuant to the requirements of the Securities Exchange Act of 1934, this Report has been signed below by the following persons on the 27th day of March, 2000 on behalf of the Registrant and in the capacities indicated:

SIGNATURE	TITLE
/s/ CYRUS Y.TSUI Cyrus Y. Tsui	President, Chief Executive Officer and Chairman of the Board (Principal Executive Officer)
/s/ STEPHEN A. SKAGGS Stephen A. Skaggs	Senior Vice President, Chief Financial Officer and Secretary (Principal Financial Officer)
/s/ MARK O. HATFIELD Mark O. Hatfield	Director
/s/ DANIEL. S HAUER Daniel S. Hauer	Director
/s/ HARRY A. MERLO Harry A. Merlo	Director
/s/ LARRY W. SONSINI Larry W. Sonsini	Director
/s/ DOUGLAS C. STRAIN Douglas C. Strain	Director

REPORT OF INDEPENDENT ACCOUNTANTS ON FINANCIAL STATEMENT SCHEDULE

To the Board of Directors of
Lattice Semiconductor Corporation

Our audits of the consolidated financial statements referred to in our report dated January 19, 2000 appearing in the 1999 Transition Report to Stockholders of Lattice Semiconductor Corporation and subsidiaries (which report and consolidated financial statements are incorporated in this Transition Report on Form 10-K) also included an audit of the financial statement schedule listed in Item 14(a)(2) of this Form 10-K. In our opinion, the financial statement schedule presents fairly, in all material respects, the information set forth therein when read in conjunction with the related consolidated financial statements.

/s/ PRICEWATERHOUSECOOPERS LLP

Portland, Oregon
January 19, 2000

SCHEDULE VIII

LATTICE SEMICONDUCTOR CORPORATION

VALUATION AND QUALIFYING ACCOUNTS

(IN THOUSANDS)

COLUMN A CLASSIFICATION	COLUMN B BALANCE AT BEGINNING OF PERIOD	COLUMN C CHARGED TO COSTS AND EXPENSES	COLUMN D CHARGED TO OTHER ACCOUNTS (DESCRIBE)	COLUMN E WRITE-OFFS NET OF RECOVERIES	COLUMN F BALANCE AT END OF PERIOD
Fiscal year ended March 31, 1998:					
Allowance for deferred tax asset.....	$1,996	$(205)	--	--	$1,791
Allowance for doubtful accounts.....	874	3	--	(80)	797
	$2,870	$(202)	$ --	$ (80)	$2,588
Fiscal year ended March 31, 1999:					
Allowance for deferred tax asset.....	$1,791	$(136)	--	--	$1,655
Allowance for doubtful accounts.....	797	70	--	14	881
	$2,588	$ (66)	$ --	$ 14	$2,536
Fiscal period ended December 31, 1999:					
Allowance for deferred tax asset.....	$1,655	$ --	--	$(1,655)	$ --
Allowance for doubtful accounts.....	881	75	650	--	1,606
	$2,536	$ 75	$650(1)	$(1,655)	$1,606

(1) Balance acquired in conjunction with our acquisition of Vantis Corporation on June 15, 1999.

AMENDED AND RESTATED
WAFER FABRICATION AGREEMENT

by and between

ADVANCED MICRO DEVICES, INC.,
a Delaware corporation

and

VANTIS CORPORATION,
a Delaware corporation

dated as of

APRIL 21, 1999

AMENDED AND RESTATED
WAFER FABRICATION AGREEMENT

THIS AMENDED AND RESTATED WAFER FABRICATION AGREEMENT (the "AGREEMENT"), is entered into as of this 21st day of April, 1999 (to be effective as of the Closing Date, as defined below), by and between ADVANCED MICRO DEVICES, INC., a Delaware corporation having its principal place of business at One AMD Place, Sunnyvale, California 94086 ("AMD"), and Vantis Corporation, a Delaware corporation having its principal place of business at 995 Stewart Drive, Sunnyvale, California 94088 ("VANTIS").

1. BACKGROUND

1.1. AMD. AMD is in the business of designing, manufacturing, testing and selling semiconductor devices, among other products. AMD manufactures certain semiconductor devices along submicron process lines within AMD's plant located at 5204 East Ben White Boulevard, Austin, Texas 78741 ("[*]" and "[*]") and within AMD's Submicron Development Center located at 915 DeGuigne Drive, Sunnyvale, CA 94088 (the "[*]") [*] are collectively referred to herein as the "FACILITIES").

1.2. VANTIS. Vantis is in the business of designing, developing and marketing CMOS programmable logic devices, field programmable gate arrays and related software.

1.3. SCOPE OF AGREEMENT. AMD has historically fabricated semiconductor devices for AMD's programmable logic business (the "BUSINESS") at the Facilities. AMD has transferred the Business to Vantis. AMD has entered into an agreement with Lattice Semiconductor Corporation ("LATTICE") pursuant to which Lattice has agreed to purchase, and AMD has agreed to sell, the stock of Vantis to Lattice (the "PURCHASE AGREEMENT," such transaction the "PURCHASE"). After the Purchase, the parties desire to continue a fabrication relationship between the Business and AMD. Specifically, Vantis desires to develop and sell programmable logic semiconductor devices and AMD desires to fabricate such semiconductor devices (the "WAFERS") at the Facilities.

1.4 PURPOSE OF AMENDED AGREEMENT. In connection with the Purchase, AMD and Vantis have agreed to amend and restate, in this Agreement, the Wafer Fabrication Agreement between them dated as of September 27, 1997, as amended, to be effective as of the Closing Date (as defined in the Purchase Agreement), so as to assure that during the term of this Agreement AMD will continue to provide to Vantis, for the benefit of Lattice, wafer fabrication services following the Closing (as defined in the Purchase Agreement).

AGREEMENT

NOW, THEREFORE, in consideration of the premises and for other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the parties agree as follows:

2. DEFINITIONS

2.1. "ACCEPTANCE CRITERIA" has the meaning specified in Article 7.3.2.

2.2. "ANNUAL FORECAST" has the meaning specified in Article 9.1.

2.3. "BASE AMOUNT" has the meaning specified in Article 9.2.2.

2.4. "BASE WAFER PRICE" has the meaning specified in Exhibit E.

2.5. "BUSINESS" has the meaning specified in Article 1.3.

2.6. "CHANGE IN CONTROL" means, with respect to an entity: (i) the sale, lease, transfer, conveyance or other disposition (other than by way of merger or consolidation), in one or a series of related transactions, of all or substantially all of the assets of the entity and its subsidiaries taken as a whole to any Person or (ii) the consummation of any transaction (including without limitation any merger or consolidation) the result of which is that any Person becomes the direct or indirect "beneficial owner" (as such term is defined in Rule 13d-3 and Rule 13d-5 under the Exchange Act) of more than 50% of the voting stock of the entity.

2.7. "COMMERCIALLY REASONABLE EFFORTS" means such efforts taken by or expected to be taken by a prudent commercial entity in the same or similar business as the party being held to such standard, acting under like circumstances.

2.8. "COMMITTED BUILD AMOUNT" has the meaning specified in Article 9.3.

2.9. "COMMUNICATION" has the meaning specified in Article 9.2.1.

2.10. "CONFIDENTIAL INFORMATION" has the meaning specified in Article 12.1.

2.11. "DEVICE" means any integrated circuit comprising [*].

2.12. "DIE" means one of the semiconductor devices on a Wafer.

2.13. "DIRECT COMPETITOR" of an entity means a Person who designs, manufactures or sells products which compete with those designed, manufactured or sold by the entity at the time of determination.

2.14. "[*] PROCESS" means any of the Processes commonly referred to as [*].

2.15. "ENGINEERING WAFERS" has the meaning specified in Article 7.3.1.

2.16. "EXCESS CAPACITY LOSS" for any period means the amount equal to (i) the aggregate Base Wafer Price of all Wafers comprising the Minimum Purchased Capacity Amount of Wafers for such period MINUS (ii) the aggregate Base Wafer Price of all Wafers comprising the Purchased Products for such period; PROVIDED, that any such amount shall be reduced by the aggregate Base Wafer Price of all Wafers comprising the Minimum Purchased Capacity Amount of Wafers that would have been built for Vantis using the production capacity used or filled by AMD in accordance with Article 5.2 or Article 9.2.4.

2.17. "EXCHANGE ACT" means the Securities Exchange Act of 1934.

2.18. "EXPECTED NET DIE PER WAFER" has the meaning specified in Exhibit A.

2.19. "EXPIRATION DATE" has the meaning specified in Article 13.1.

2.20. "[*]" has the meaning specified in Article 1.1.

2.21. "[*]" has the meaning specified in Article 1.1.

2.22. "FACILITIES" has the meaning specified in Article 1.1

2.23. "FORECASTED AMOUNT" has the meaning specified in Article 9.2.2(b).

2.24. "FORECASTED ANNUAL AMOUNT" has the meaning specified in Article 9.2.2(a).

2.25. "[*] OUT MINIMUM" means, for any [*], [*] of the Forecasted Amount specified for such [*] in the Communication responding to the Rolling [*] Forecast in which that [*] was the fourth full [*] of the forecast.

2.26. "HOT LOT" means a Wafer fabrication lot processed at two-thirds standard cycle time (as defined in Exhibit C).

2.27. "LONG-TERM COMMITTED CAPACITY AMOUNT" has the meaning specified in Article 9.2.1(a).

2.28. "MAXIMUM CAPACITY AMOUNT" means, for any period, the aggregate of the Maximum Fab Capacity Amount of all Facilities.

2.29. "MAXIMUM COMMITTED CAPACITY AMOUNT" means, for any Facility and Process in 1999, 2000 and 2001, the amount of Wafers specified in any of those years for such Facility and Process on Schedule 2.29.

2.30. "MAXIMUM FAB CAPACITY AMOUNT" means, for any period, the maximum amount of Wafers that may be fabricated using all of AMD's wafer fabrication production capacity at a particular Facility during such period.

2.31. "MINIMUM ANNUAL PURCHASED CAPACITY AMOUNT" means, for any calendar year, the largest of the Next Year Minimum, Second Year Minimum and Third Year Minimum for such calendar year.

2.32. "MINIMUM [*] PURCHASED CAPACITY AMOUNT" means, for any [*], the largest of the [*] Minimums applicable to such [*]; PROVIDED, HOWEVER, THAT if in any monthly Communication AMD states that a [*] Minimum previously applicable to any [*] is waived, the Minimum [*] Purchased Capacity Amount for any such [*] shall be calculated only with reference to the [*] Minimum contained in the Communication from AMD for such [*] in lieu of the waived [*] Minimum(s) previously applicable to such [*].

2.33. "MINIMUM PURCHASED CAPACITY AMOUNT" means, for any [*], the Minimum [*] Purchased Capacity Amount, and for any [*], the Minimum [*] Purchased Capacity Amount.

2.34. "MONTH" means an AMD fiscal month.

2.35. "[*] MINIMUM" means, for any [*], the [*] Out Minimum, [*] Out Minimum, [*] Out Minimum or [*] Out Minimum applicable to such [*].

2.36. "[*] OUT MINIMUM" means, for any [*], [*] of the Forecasted Amount specified for such [*] in the Communication responding to the Rolling [*] Forecast in which that [*] was the first full [*] of the forecast.

2.37. "NEXT YEAR MINIMUM" means, for [*], [*], for [*], [*] and for [*], [*], of the Long-Term Committed Capacity Amount of Die specified for such year in the Communication responding to the [*] Forecast in which that [*] was the first [*] of the forecast.

2.38. "PERSON" means any individual, firm, sole proprietorship, partnership, joint venture, trust, incorporated organization, association, corporation, institution, public benefit corporation, entity, government (whether federal, state, county, city, municipal or otherwise, including, without limitation, any instrumentality, division, agency, body or department thereof) or group (as such term is defined in Section 13(d)(3) of the Exchange Act).

2.39. "PRICING PERIOD" has the meaning specified in Article 8.1.5.

2.40. "PRIOR LONG-TERM COMMITTED CAPACITY AMOUNT" has the meaning specified in Article 9.2.2.

2.41. "PRIOR SHORT-TERM COMMITTED CAPACITY AMOUNT" has the meaning specified in Article 9.2.2.

2.42. "PROCESS" means any semiconductor wafer, semiconductor die or integrated circuit fabrication process owned, licensed or developed by AMD. Each Process is comprised of (a) all process flows, process steps, process conditions (and modifications thereto) used to manufacture Wafers at the Facilities as well as (b) all methods, formulae, procedures, technology and know-how associated with such process flows, process steps and process conditions. The Processes do not and shall not include any methods, formulae, procedures, technology or know-how licensed or received from Vantis under this Agreement or other existing agreements between the parties or executed between the parties in the future, unless otherwise agreed in writing.

2.43. "PROCESS FORECAST LEAD TIME" for any Process means [*] plus the cycle time in days specified for such Process in Exhibit C as of the date of determination.

2.44. "PRODUCTS" means the various types of Wafers and/or Die fabricated at the Facilities pursuant to this Agreement using different Processes and identified by unique series or product names or numbers. The list of Products fabricated pursuant to this Agreement is set forth in Exhibit F, which list shall be deemed to include, even if not expressly listed, all Products which have been fabricated by AMD for Vantis from September 27, 1997 to the date of this Agreement. Any additional products that the parties desire to fabricate at the Facilities shall be determined by the mutual agreement of AMD and Vantis. The parties acknowledge, however, that the final determination of what Products shall be fabricated may depend on the results of joint development and product qualification and shall be limited to Products to be sold in the Business.

2.45. "PRODUCT SPECIFIC HARDWARE" has the meaning specified in Article 7.8.1.

2.46. "PURCHASE" has the meaning specified in Article 1.3.

2.47. "PURCHASE AGREEMENT" has the meaning specified in Article 1.3.

2.48. "PURCHASE ORDER" means a [*] blanket purchase order for an amount of Die equivalent to the Minimum [*] Purchased Amount of Die for the next [*]placed by Vantis with AMD in accordance with Article 8.4.1, which purchase order shall be for the convenience of the parties and shall not constitute a request by Vantis to purchase Die and/or Wafers.

2.49. "PURCHASED PRODUCTS" means, for any period, Wafers and/or Die delivered in such period by AMD to Vantis (and accepted by Vantis) pursuant to Vantis Purchase Orders.

2.50. "RELATED AGREEMENTS" means this Agreement, the Amended and Restated Assembly, Test, Mark and Pack Agreement by and between AMD and Vantis dated as of April 21, 1999, the Amended and Restated Administrative Services Agreement by and between AMD and Vantis dated as of April 21, 1999 and the Amended and Restated Patent Cross License Agreement by and among AMD, Vantis and Lattice dated April 21, 1999.

2.51. "REPURCHASED CAPACITY AMOUNT" means, for any [*] in which AMD fails to supply the Committed Build Amount pursuant to Article 4.3.5, the product of (x) [*] TIMES (y) [*].

2.52. "RISK PRODUCTION LOTS" has the meaning specified in Article 7.2.7.

2.53. "ROCKET LOT" means a Wafer fabrication lot processed at one-and-one-half times theoretical cycle time (as defined in Exhibit C).

2.54. "ROLLING [*] FORECAST" has the meaning specified in Article 9.1.

2.55. "[*] OUT MINIMUM" means, for any [*], [*] of the Forecasted Amount specified for such [*] in the Communication responding to the Rolling [*] Forecast in which that [*] was the second full [*] of the forecast.

2.56. "[*] Minimum" means, for [*], [*] and for [*], [*] of the Long-Term Committed Capacity Amount of Die specified for such [*] in the Communication responding to the [*] Forecast in which that [*] was the [*] of the forecast.

2.57. "SHORT-TERM COMMITTED CAPACITY AMOUNT" has the meaning specified in Article 9.2.1(b).

2.58. "SUBSIDIARY" means any corporation, partnership, joint venture or other legal entity whose ownership rights are 100% owned or controlled directly or indirectly, by AMD or Vantis, as the case may be.

2.59. "TERM" has the meaning specified in Article 13.1.

2.60. "TERMINATING [*]" has the meaning specified in Article 13.6.

2.61. "[*] OUT MINIMUM" means, for any [*], [*] of the Forecasted Amount specified for such [*] in the Communication responding to the Rolling [*] Forecast in which that [*] was the third full [*] of the forecast.

2.62. "[*] MINIMUM" means, for 2001, [*] of the Long-Term Committed Capacity Amount of Die specified for such year in the Communication responding to the Five Year Forecast in which that year was the third full calendar year of the forecast.

2.63. "WAFERS" means the semiconductor wafers fabricated by AMD at the Facilities for Vantis. Vantis agrees that the Wafers fabricated by AMD for Vantis shall be utilized solely in the production of Programmable Logic Devices for sale by Vantis and/or Lattice.

2.64. "WAFER SORT EQUIPMENT" means the Wafer sort testers and other Wafer sorting equipment owned by Vantis and installed in the Facilities for purposes of electrically testing individual Die or Wafers.

2.65. "WAFER SPECIFICATIONS" means the design and quality specifications for Wafers contained in AMD Specification Nos. [*], as currently in effect.

3. REPRESENTATIONS

3.1. REPRESENTATIONS OF AMD. In order to induce Vantis to enter into this Agreement, AMD hereby represents and warrants that:

3.1.1 CORPORATE STATUS. (a) AMD is duly organized, validly existing and in good standing under the laws of Delaware, (b) has the corporate power to own or lease its assets and to transact the business in which it is currently engaged and (c) is in compliance with all requirements of law except to the extent that the failure to comply therewith shall not materially affect the ability of AMD to perform its obligations under this Agreement.

3.1.2 CORPORATE AUTHORITY. (a) AMD has the corporate power, authority and legal right to execute, deliver and perform this Agreement and has taken as of the date hereof all necessary corporate action to execute this Agreement, (b) the person executing this Agreement has actual authority to do so on behalf of AMD and (c) there are no outstanding assignments, grants, licenses, encumbrances, obligations or agreements, either written, oral or implied, that prohibit execution of this Agreement.

3.2. REPRESENTATIONS OF VANTIS. In order to induce AMD to enter into this Agreement, Vantis hereby represents and warrants that:

3.2.1 CORPORATE STATUS. Vantis (a) is duly organized, validly existing and in good standing under the laws of Delaware, (b) has the corporate power to own or lease its assets and to transact the business in which it is currently engaged and (c) is in compliance with all requirements of law except to the extent that the failure to comply therewith shall not materially affect the ability of Vantis to perform its obligations under this Agreement.

3.2.2 CORPORATE AUTHORITY. (a) Vantis has the corporate power, authority and legal right to execute, deliver and perform this Agreement and has taken as of the date hereof all necessary corporate action to execute this Agreement, (b) the person executing this Agreement has actual authority to do so on behalf of Vantis and (c) there are no outstanding assignments, grants, licenses, encumbrances, obligations or agreements, either written, oral or implied, that prohibit execution of this Agreement.

4. WAFER BUILD AND SUPPLY COMMITMENT

4.1. CAPACITY AND BUILD COMMITMENTS.

4.1.1 CAPACITY COMMITMENT. Subject to the terms and conditions set forth in this Agreement, each [*] shall reserve capacity at the Facilities sufficient to fabricate an amount of Die equivalent to the lesser of (a) the Maximum Committed Capacity Amount of Die applicable to such [*], (b) the Long-Term Committed Capacity Amount of Die for such [*] and (c) the Short-Term Committed Capacity Amount of Die for such [*] determined in accordance with the provisions of Article 9.2.

4.1.2 BUILD COMMITMENT. Each [*] AMD shall fabricate and deliver to Vantis an amount of Die equivalent to the Committed Build Amount of Die for such [*] determined in accordance with the provisions of Article 9.3.

4.2. ADDITIONAL CAPACITY. At the request of Vantis, AMD shall use Commercially Reasonable Efforts to make production capacity at the Facilities available to Vantis that is in addition to the production capacity necessary for AMD to fabricate the Committed Build Amount of Die; PROVIDED, HOWEVER, that in no event shall AMD be required by this Agreement to produce Wafers in any period in excess of the Maximum Capacity Amount for such period.

4.3. FAILURE TO FABRICATE COMMITTED BUILD AMOUNT OF DIE.

4.3.1 FAILURE DUE TO AMD'S ERROR OR MISPROCESSING OF MATERIAL. In the event that (a) AMD fails to fabricate the Committed Build Amount of Die applicable to a specific [*] in the manner specified by this Agreement by the end of such [*] or (b) AMD believes that it will be unable to fabricate the Committed Build Amount of Die applicable to such [*] end of such [*], and, in each case, such failure is due to AMD's error or misprocessing of material, then AMD shall take the following measures:

First, AMD shall promptly describe the nature of the difficulty to Vantis and provide a corrective action plan.

Second, AMD shall use Commercially Reasonable Efforts to remedy the difficulty in an expeditious manner before the end of the second full [*] following the Month in which AMD was unable to fabricate the Committed Build Amount of Die.

Third, (a) with respect to any such failure affecting a Product fabricated in [*], AMD shall use its best efforts and (b) with respect to any deficiency affecting a Product fabricated in [*], AMD shall use Commercially Reasonable Efforts, to make available during the above-referenced period sufficient production capacity at the affected Facilities to cover the difference between the Committed Build Amount of Die applicable to such period and the

amount of Wafers needed to make up the deficiency experienced in the previous Month, including, but not limited to, allocating additional Hot Lot or Rocket Lot capacity to Vantis without any additional charge or premium normally associated with the provision of such capacity and making production capacity available to Vantis that is in addition to the production capacity necessary for AMD to fabricate the Committed Build Amount of Die applicable to such period.

Fourth, in the event that the above measures are insufficient, Vantis may cancel or reallocate any outstanding orders for Wafers up to an amount of Wafers equivalent to the deficiency experienced in the [*] of AMD's failure; PROVIDED, HOWEVER, that the aggregate amount of any Wafers not purchased as a result of such cancellation or reallocation of orders shall be counted as Purchased Products when calculating the obligations of Vantis pursuant to Article 5.1.2, if any, for the period in which the deficiency occurred.

4.3.2 CONTINUAL FAILURE DUE TO AMD'S ERROR OR MISPROCESSING OF MATERIAL. In the event that AMD fails to fabricate the Committed Build Amount of Die for [*] consecutive [*], and, in each [*], such failure is due to AMD's error or misprocessing of material, then (a) AMD shall use Commercially Reasonable Efforts to find an alternative source of Wafers for Vantis' forecasted needs and (b) Vantis may terminate this Agreement without liability upon [*] prior written notice to AMD.

4.3.3 FAILURE DUE TO VANTIS. Notwithstanding anything contained in this Article 4.3 to the contrary, in the event that AMD fails to fabricate the Committed Build Amount of Die in any [*] due to (a) design defects caused by Vantis, (b) design changes requested by Vantis, (c) process flow changes requested by Vantis or (d) any other reason caused by Vantis, AMD shall only be required to make reasonable efforts to fabricate the Committed Build Amount of Die in such [*].

4.3.4 FAILURE DUE TO BOTH PARTIES. Notwithstanding anything contained in Article 4.3.1, 4.3.2, 4.3.3 or 5.1 to the contrary, in the event that AMD fails to fabricate the Committed Build Amount of Die in any [*] due to difficulties caused jointly by Vantis and AMD, the parties shall each use Commercially Reasonable Efforts to mutually agree in writing upon a fair and equitable solution.

4.3.5 FAILURE BY AMD TO SUPPLY A PORTION OF THE CAPACITY COMMITTED TO VANTIS. If at any time prior to June 30, 2001, AMD fails to supply the capacity at the Facilities previously reserved for Vantis pursuant to Article 4.1.1 for any specific [*] as a result of (a) an intentional reallocation by AMD of such reserved capacity to a Person, including AMD, other than Vantis (other than in accordance with Article 9.2.4) or (b) an intentional act, omission or failure to act by AMD intended to cause AMD to not comply with the standards imposed on AMD in Article 7.8.2 of this Agreement, in each case such that AMD fails to deliver the Committed Build Amount of Die applicable to such [*] by the end of such [*], then AMD shall pay Vantis the Repurchased Capacity Amount. Nothing set forth herein shall in any way limit AMD's obligation to maintain and make available to Vantis the capacity set forth in this Agreement; PROVIDED, HOWEVER, that the payment of the Repurchased Capacity Amount shall constitute the sole remedy of Vantis, and the sole obligation of AMD, with respect to the acts described in clauses (a) and (b) of this Article 4.3.5. The Repurchased Capacity Amount for any

[*] shall be paid by AMD to Vantis, in cash, not later than [*] from the due date of the Vantis invoice therefor.

5. PURCHASE COMMITMENT; DISPOSITION OF EXCESS CAPACITY

5.1. PURCHASE OF DIE AND/OR FABRICATED WAFERS; MINIMUM PURCHASE COMMITMENT; LIQUIDATED DAMAGES.

5.1.1 PURCHASE OF DIE AND/OR FABRICATED WAFERS. Each [*], Vantis agrees to purchase from AMD an amount of Die and/or Wafers equal to the Committed Build Amount of Die specified in the Communication from AMD to Vantis for such [*].

5.1.2 MINIMUM [*] PURCHASED CAPACITY AMOUNT OF WAFERS; [*] EXCESS CAPACITY LOSS. If during any [*] during the Term the aggregate number of Purchased Products in such [*] is less than the Minimum [*] Purchased Capacity Amount of Wafers for such [*] determined in accordance with Exhibit B, then Vantis shall pay AMD, as liquidated damages, the Excess Capacity Loss for such [*]. The Excess Capacity Loss for such [*] shall be paid by Vantis to AMD, in cash, not later than [*] from the date of the AMD invoice therefor.

5.1.3 MINIMUM [*] PURCHASED CAPACITY AMOUNT OF WAFERS; [*] EXCESS CAPACITY LOSS. If during any calendar year during the Term, or for 1999, during the period specified in Exhibit B, the aggregate number of Purchased Products in such calendar year or period is less than the Minimum Annual Purchased Capacity Amount of Wafers for such calendar year or period determined in accordance with Exhibit B, then Vantis shall pay AMD, as liquidated damages, the Excess Capacity Loss for such [*] or period. The Excess Capacity Loss for such [*] or period shall be paid by Vantis to AMD, in cash, not later than [*] from the date of the AMD invoice therefor.

5.1.4 OFFSET AGAINST ANNUAL EXCESS CAPACITY LOSS. The [*] Excess Capacity Loss, if any, payable by Vantis pursuant to Article 5.1.3 for any [*] shall be offset by the [*] Excess Capacity Loss, if any, paid by Vantis pursuant to Article 5.1.2 for each of the [*] in such [*].

5.2. DISPOSITION OF EXCESS CAPACITY. AMD shall use Commercially Reasonable Efforts to sell excess production capacity to other customers or to utilize such excess capacity for AMD's own readily suitable capacity needs in accordance with Article 9.2.4.

6. WARRANTY

AMD warrants that Die and/or Wafers delivered hereunder will meet the applicable specifications and shall be free from defects in material and workmanship under normal use and service for [*] calendar months from shipment from AMD. If, during such period (i) AMD is notified promptly in writing upon discovery of any defect in the Die and/or Wafers, including a detailed description of such defect, (ii) samples of such Die and/or Wafers are returned to AMD; and (iii) AMD's examination of such Die and/or Wafers discloses that such Die and/or Wafers are defective and such defects are not caused by accident, abuse, misuse, neglect, improper installation, repair, alteration or other action by someone other than AMD, improper testing or use contrary to any instructions issued by AMD or Vantis, within a reasonable time, AMD shall,

at AMD's sole option, either replace or credit Vantis for such Die and/or Wafers. AMD shall return any Die and/or Wafers replaced under this warranty to Vantis, transportation prepaid. The foregoing warranty constitutes AMD's exclusive liability, and the exclusive remedy of Vantis, for any breach of any warranty or other nonconformity of the Die and/or Wafers. Prior to any return of Die and/or Wafers by Vantis pursuant to this Article 6, Vantis shall afford AMD the opportunity to inspect such Die and/or Wafers at Vantis' location, and any such Die and/or Wafers so inspected shall not be returned to AMD without its prior written consent. THIS WARRANTY IS EXCLUSIVE AND IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, WHICH ARE HEREBY EXPRESSLY DISCLAIMED.

7. FABRICATION AND PURCHASE AND SALE OF PRODUCTS

7.1. START OF PRODUCTION. Qualification testing for the Products shall be conducted in the manner to be mutually agreed upon in writing by the parties. Once any Product has been qualified, AMD shall begin mass production of such Product in accordance with the Wafer Specifications for such Product.

7.2. PRODUCTION CONTROL.

7.2.1 OPERATION OF FACILITIES TO PERFORMANCE METRICS. Without otherwise limiting its obligations hereunder, AMD shall operate the Facilities in the production of Wafers in accordance with the performance metrics specified in Exhibit C.

7.2.2 FAST TRACK COMMITMENT. As requested by Vantis from time to time because of business needs and as otherwise reasonably agreed to by AMD, AMD shall provide Vantis with expedited production cycle times ("HOT LOT" and "ROCKET LOT" capacity) for engineering qualification and other expedited production needs. AMD shall make available an aggregate of at least [*] Hot Lots and at least [*] Rocket Lots at each Facility (other than [*]). Vantis shall have the right to use a percentage of the Hot Lots available at each Facility (other than [*]) equivalent to the percentage determined by dividing (a) the Committed Build Amount of Wafers in the applicable Facility by (b) such Facility's Maximum Fab Capacity Amount of Wafers (rounded down to the nearest whole lot, but not less than one lot). Vantis shall have a right to use a percentage of the Rocket Lots available at each Facility (other than [*]) equivalent to the percentage determined by dividing (x) the Committed Build Amount of Wafers in the applicable Facility by (y) such Facility's Maximum Fab Capacity Amount of Wafers (rounded down to the nearest whole lot, but not less than one lot). In addition to the minimum commitments specified in this Article 7.2.2, AMD shall use Commercially Reasonable Efforts, based on then current work-in-process, to meet Vantis' Hot Lot and Rocket Lot requirements.

7.2.3 WAFER PACKAGING; PRODUCT SHIPMENT. AMD shall package the Wafers in accordance with AMD's packaging specifications set forth in AMD Specification No. [*], as amended, supplemented or replaced by AMD from time to time. Products which have completed the wafer fabrication and wafer sort Processes and met all Acceptance Criteria shall be delivered to the custody of a designated carrier pursuant to Article 8.3 within one business day of meeting all Wafer Acceptance Criteria in accordance with AMD Specification Nos. [*], as amended, supplemented or replaced by AMD from time to time.

7.2.4 NOTIFICATION EVENTS. AMD shall promptly notify Vantis of the following: (a) any issues known to AMD which will adversely affect AMD's ability to fabricate the Committed Build Amount of Die in any period or otherwise adversely affect performance and/or quality of the Products; (b) intended changes to Processes or materials used to fabricate the Wafers, except to the extent that minor changes may be made to such Processes, Acceptance Criteria or related materials pursuant to AMD Specification Nos. [*], as amended, supplemented or replaced by AMD from time to time; (c) intended changes in any of the material suppliers which supply AMD with raw wafers, aluminum targets and photomasks; and (d) intended closure of any Facility or cessation of all Wafer fabrication activities at any Facility.

7.2.5 PREAPPROVAL RIGHTS. AMD shall not take any of the following actions without the prior written approval of Vantis (which approval may not be unreasonably withheld): (a) change any Processes or Acceptance Criteria, or material used to fabricate the Wafers, except to the extent that minor changes may be made to such Processes, Acceptance Criteria or related materials pursuant to AMD Specification Nos. [*], as amended, supplemented or replaced by AMD from time to time; (b) change any of the material suppliers which supply AMD with raw wafers, aluminum targets and photomasks; (c) change any AMD Specification used in connection with fabrication of the Wafers; and (d) change the Facility at which a Product is fabricated. Vantis agrees to cooperate with AMD to use Commercially Reasonable Efforts to approve changes which will result in improved yields of Wafers and/or Products and/or reduced fabrication costs and which will not materially adversely impact Product performance.

7.2.6 PRODUCT/DESIGN QUALIFICATION. AMD shall not commence production of Products on new fabrication Processes or mask sets without obtaining the prior qualification and release of such Processes and mask sets from Vantis.

7.2.7 RISK PRODUCTION LOT STARTS. Prior to completion of full qualification of fabrication Processes and/or mask sets for a particular Product, Vantis may authorize AMD in writing to start fabrication of additional Wafers for such Product ("RISK PRODUCTION LOTS"). Vantis shall bear, and pay to AMD upon request, all costs and financial risk for Wafers from Risk Production Lots which ultimately do not meet Wafer Acceptance Criteria; PROVIDED, HOWEVER, that Vantis shall have no liability to AMD for Wafers from Risk Production Lots which fail Wafer Acceptance Criteria because of a defect in material or workmanship unrelated to implementation of the new fabrication Process and/or mask sets.

7.3. ENGINEERING.

7.3.1 DEVELOPMENT ENGINEERING LOTS. At the request of Vantis, AMD shall fabricate Wafers for use by Vantis in conducting engineering studies ("ENGINEERING WAFERS") subject to the maximum amount of Wafers that may be fabricated using the wafer production capacity dedicated by AMD for conducting such development engineering work. Prices for Engineering Wafers shall be as specified in Article 8.1.4. Engineering Wafer lots shall be processed with altered processing conditions specified by Vantis, and AMD shall not further alter such processing conditions without prior written authorization from Vantis. The cycle time for Engineering Wafer lots shall be as follows:

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(a) The cycle time for Engineering Wafer lots fabricated with minor parametric variations or minor alterations in Process conditions (e.g., "corner lots") shall be not more than [*] of the standard production cycle time specified in Exhibit C.

(b) The cycle time for Engineering Wafer lots fabricated with changes in Process flow or major alterations in Process conditions shall be as agreed in each instance between the Parties.

Vantis shall bear, and pay to AMD upon request, all costs and financial risk for Wafers from Engineering Wafer lots which ultimately do not meet Acceptance Criteria; PROVIDED, HOWEVER, that Vantis shall have no liability to AMD for Wafers from Engineering Wafer lots which fail Acceptance Criteria because of a defect in material or workmanship unrelated to the altered processing conditions specified by Vantis for such lots.

7.3.2 ACCEPTANCE CRITERIA; DELIVERY OF WAFERS TO VANTIS. Except for Risk Production Lots and Engineering Wafer Lots contemplated by Article 7.2.7 and 7.3.1, every Wafer lot (and every Wafer where 100% testing is required) shall meet the acceptance requirements documented in the sampling plan specified in AMD Specification Nos. [*], as amended by AMD in writing (and as approved by Vantis in writing pursuant to Article 7.2.5) or as supplemented or replaced by Vantis in writing (and as approved by AMD in writing) from time to time and all other AMD acceptance requirements which vary from the foregoing specifications by Product number (the "ACCEPTANCE CRITERIA"). AMD shall not make any exceptions to the Acceptance Criteria without written authorization from Vantis. Vantis shall accept, and shall not have the right to reject, Wafers delivered to Vantis by AMD which have passed the Acceptance Criteria.

7.3.3 CONTINUOUS YIELD IMPROVEMENT TEAM. AMD and Vantis shall each designate one person to lead a Continuous Yield Improvement Team. The person designated by Vantis shall be the team leader. The overall goal of the team shall be to increase the Expected Net Die Per Wafer for each Product and Process. Specific responsibilities of the Continuous Yield Improvement Team shall include: setting yield targets by Product and monitoring progress toward such yield targets; identifying and driving yield improvement opportunities by Product and Process; establishing statistical process control targets for critical Process parameters and ensuring performance remains within such statistical control targets; and reporting continuous yield improvement progress at the [*] Management Review Meeting.

7.3.4 COOPERATION CLAUSE. In the event of unusually high customer returns of Product or other unspecified degradation of Product performance, AMD and Vantis agree to cooperate to improve the manufacturability and yield of such Product by (a) reviewing the fabrication process, including any AMD Processes and AMD specifications and (b) proposing possible revisions to such Processes and specifications.

7.3.5 WAFER LEVEL RELIABILITY TESTING. At least [*], AMD shall conduct routine wafer level reliability testing at each Facility, including, but not limited to, [*].

7.3.6 AMD PROVIDED ENGINEERING SERVICES. AMD shall provide engineering services to the Facilities as necessary to maintain adequate production capacity and consistent Wafer yield, Product and quality performance.

7.4. INFORMATION ACCESS.

7.4.1 MANUFACTURING INFORMATION. AMD and Vantis shall consult and cooperate to develop a mechanism to provide Vantis with daily electronic access to all manufacturing, inventory, and engineering data related to the Wafers manufactured in the Facilities pursuant to this Agreement. AMD shall provide Vantis with a performance report of Wafer fabrication work in process at each Facility for each Product weekly, including statistical process control data relating to such work in process, the details to be as agreed upon by the parties. To enable Vantis to track process control, AMD shall provide Vantis with regular, at least quarterly, updates to forecasted, actual and estimated parametric measurements and trends for each of the AMD manufacturing Processes used to manufacture Wafers and/or Die for Vantis. Specific measurements and the format of information to be provided shall be defined by the Continuous Yield Improvement Team.

7.4.2 [*] MANAGEMENT REVIEW MEETING. Each [*] during the Term of the Agreement, Vantis and AMD shall conduct a "[*] Management Review Meeting." The purpose of the [*] Management Review Meeting shall be to review the immediately preceding [*] performance relative to the metrics set forth in Exhibit C, as well as discuss Vantis' future Wafer fabrication requirements.

7.4.3 RETENTION OF DOCUMENTS. In accordance with AMD Policy No. [*], AMD shall retain all records, reports, logs, test data, calculations and estimates generated in connection with fabrication of the Wafers for Vantis pursuant to this Agreement. Upon termination of this Agreement, AMD shall archive such materials in accordance with AMD Specification No. [*]. AMD shall notify Vantis before destroying or otherwise disposing of such materials.

7.5. FACILITIES ACCESS.

7.5.1 ON SITE INSPECTION. Vantis representatives shall be allowed to visit the Facilities during normal working hours upon at least three business days' advance notice to AMD.

7.5.2 AUDITS. AMD shall allow Vantis to perform an audit of each Facility [*] during the Term; PROVIDED, that AMD shall have received written notice from Vantis at least [*] prior to the commencement of each such audit; and provided further that each such audit shall be conducted during AMD's regular business hours and without undue disruption of AMD's business. At the request of Vantis, AMD shall allow customers of Vantis to perform audits of the Facilities, subject to the mutual agreement of AMD, Vantis and such customer as to the timing, scope and details of such an audit.

7.5.3 VANTIS RESIDENT ENGINEERS. Vantis shall have the right to locate at the Facilities up to [*] resident engineers employed by Vantis, mutually acceptable to both AMD and Vantis, to work cooperatively with AMD's employees at the Facilities. AMD shall provide to such engineers, at the expense of AMD: (i) office space located at the Facilities; and (ii) the ordinary services, including, but not limited to, secretarial services (but not including a reserved or exclusive secretary) provided to other similarly situated AMD employees.

7.6. SAFEGUARDING OF INVENTORY AND PHOTOMASKS. AMD shall use Commercially Reasonable Efforts to safeguard against loss or damage to its finished and unfinished Wafer inventory and any inventory of photomasks supplied by Vantis for the manufacture of Wafers.

7.7. PHOTOMASK SUPPLY. Vantis shall bear all costs to produce the initial photomask set to manufacture any Wafer or new photomasks to complete design or process changes initiated by Vantis. Vantis may obtain photomasks directly or through the AMD photomask procurement process specified in AMD Specification [*], as amended, supplemented or replaced from time to time. Vantis will bear all costs for replacement of photomasks damaged or worn during production (except to the extent such damage results from AMD's negligence or misconduct).

7.8. EQUIPMENT.

7.8.1 EQUIPMENT OWNERSHIP AND INSTALLATION. The parties acknowledge and agree that AMD is the owner of the semiconductor wafer fabrication equipment installed at the Facilities. The parties acknowledge and agree that Vantis is the owner of (a) the Wafer Sort Equipment (including all associated calibration and host computer systems) installed at the Facilities and listed on Schedule 7.8.1(a) (as it may be amended from time to time to reflect additions to or removals from service) and (b) the Product specific hardware ("PRODUCT SPECIFIC HARDWARE"), installed or located at the Facilities and listed on Schedule 7.8.1(b) (as it may be amended from time to time to reflect additions to or removals from service) (collectively, the "VANTIS EQUIPMENT"). Any Vantis Equipment installed at the Facilities shall be installed in a manner satisfactory to AMD. The parties acknowledge and agree that the Vantis Equipment installed at the Facilities as of the date of this Agreement has been installed in a satisfactory manner.

7.8.2 AMD EQUIPMENT MAINTENANCE; CAPITAL PURCHASES. AMD shall be responsible for (a) conducting routine maintenance and upkeep on its wafer fabrication equipment and Vantis' Wafer Sort Equipment and (b) providing all wafer fabrication equipment, and obtaining all raw materials and other supplies necessary for the production of Wafers using any EE Process, required for AMD to maintain production capacity necessary to fabricate the Committed Build Amount of Die applicable to a specific period, including any capital equipment purchases necessary to maintain adequate production capacity. AMD's routine maintenance and upkeep shall be sufficient to ensure that the system availability metrics listed in Exhibit C for Vantis' Wafer Sort Equipment are met or exceeded.

7.8.3 VANTIS EQUIPMENT OWNERSHIP; MAINTENANCE; CAPITAL PURCHASES. Vantis shall be responsible for (a) conducting routine maintenance and upkeep on the Vantis Equipment, other than the Wafer Sort Equipment and (b) providing all Vantis Equipment required for AMD to maintain production capacity necessary to sort the Committed Build Amount of Die applicable to a specific period, including any capital equipment purchases necessary to maintain adequate production capacity. Vantis will bear all costs for replacement and repair of Vantis Equipment damaged or worn during production (except to the extent such damage results from AMD's gross negligence or misconduct). AMD shall not be obligated to supply or maintain any Product Specific Hardware, including, without limitation, load boards, DUT boards and device probe cards, that may be necessary or desirable for AMD to fabricate the Committed Build Amount of Die applicable to a specific period.

7.9. PROCEDURES CONCERNING DELIVERY OF PHOTOMASKS AND WAFERS. Prior to the delivery of photomasks to AMD by Vantis or Wafers and/or Die to Vantis by AMD, Vantis shall have agreed upon specific procedures (or the absence of specific procedures) for any such delivery with AMD operating personnel responsible for such deliveries, which procedures may include, but shall not be limited to, scheduling, warehousing and special handling requirements, if any.

8. WAFER PRICING, PAYMENT, SHIPPING AND PURCHASE ORDERS.

8.1. BASE WAFER PRICE.

8.1.1 STABLE SORT YIELDS. Notwithstanding anything to the contrary contained herein, the parties acknowledge and agree that pricing and all purchases of Products manufactured pursuant to Processes that have exhibited a stable sort yield shall be made on a "per die" basis. Accordingly, the price of sorted Die shall equal (x) the Base Wafer Price applicable to a Process (as indicated on Exhibit E hereto), divided by (y) the Expected Net Die Per Wafer for such Process (as indicated on Exhibit A hereto); provided, however, that the price per die for the 1999 calendar year shall be as indicated on Exhibit F hereto; and provided further, that if in 1999 a particular die price is not identified on Exhibit F, then such price shall be determined using the formula set forth in this Article 8.1.1.

8.1.2 SORT YIELDS NOT YET ESTABLISHED. The price of Wafers manufactured pursuant to Processes for which an Expected Net Die Per Wafer has not yet been established, but for which the defect density is following on the expected defect density curve for such Process, shall equal the Base Wafer Price applicable to such Process.

8.1.3 UNSTABLE YIELDS. The price of Wafers manufactured pursuant to Processes which have not yet demonstrated stable yields shall be as agreed in each instance between the parties.

8.1.4 ENGINEERING WAFERS. The price of Engineering Wafers shall be as follows:

(a) The price of Engineering Wafers fabricated with minor parametric variations or minor alterations in Process conditions (e.g., "corner lots") shall equal the Base Wafer Price applicable to the Process pursuant to which such Wafers are fabricated.

(b) The price of Engineering Wafers fabricated with changes in Process flow or major alterations in Process conditions shall be as agreed in each instance between the parties.

8.1.5 EFFECTIVENESS OF WAFER PRICES. Expected Net Die Per Wafer standards, Facilities performance metrics and Base Wafer Prices (as indicated on Exhibits A, C and E, as amended, supplemented or replaced by the parties from time to time) shall be in effect for a [*]-month period (the "PRICING PERIOD") from the date of execution of any amendment to this Agreement attaching the newly agreed standards, metrics and pricing terms during the Term. Once every [*], commencing in the calendar [*] after the Closing, the parties shall proceed to negotiate in good faith as to any modifications to the Expected Net Die Per Wafer standards, Facilities performance metrics and Base Wafer Prices then in effect. If the parties are unable to agree as to any modifications to the standards, metrics and prices in effect during a Pricing

Period before the end of such Pricing Period, the Expected Net Die Per Wafer standards, Facilities performance metrics and Base Wafer Prices in effect on the last day of such Pricing Period shall automatically become the Expected Net Die Per Wafer standards, Facilities performance metrics and Base Prices in effect for the next Pricing Period unless and until the parties otherwise agree.

8.1.6 COST REDUCTIONS ([*] OR MORE). Declines in the cost of a Wafer which in the aggregate equal [*] or more of the cost of a Wafer applicable immediately prior to implementation of the cost reducing improvement and increases in the actual net die per Wafer which in the aggregate equal [*] or more of the Expected Net Die Per Wafer then specified in Exhibit A, shall be shared equally by AMD and Vantis. Vantis' share in any such Wafer cost reductions or yield improvements shall be immediately reflected in a corresponding decrease in the Base Wafer Price or a corresponding increase in the Expected Net Die per Wafer.

8.2. PAYMENT TERMS. Vantis shall pay AMD the Base Wafer Price applicable to each Purchased Product. All prices shall be quoted and invoices shall be rendered and paid in United States currency. All invoices for Purchased Products shall be accumulated by AMD for a given [*] and rendered to Vantis within [*] of the end of such [*]. Each invoice shall be paid by Vantis no later than the [*] day after receipt by Vantis of such invoice.

8.3. SHIPPING. Delivery of Wafers from AMD to Vantis shall be made C.P.T. ("carriage paid to") the default shipping location for each Product specified in AMD Specification [*], as amended, supplemented or replaced by AMD from time to time, or any other destination identified by Vantis to AMD in writing at least three days before delivery of the completed Die and/or Wafers to the custody of a designated carrier. Title to the completed Die and/or Wafers and risk of loss of, or damage to, the Die and/or Wafers shall pass to Vantis upon delivery of the completed Die and/or Wafers to the custody of a designated carrier.

8.4. PURCHASE ORDERS AND ACKNOWLEDGMENTS.

8.4.1 [*] PURCHASE ORDERS. At least two weeks before the end of each [*], Vantis shall issue to AMD a blanket Purchase Order expressed in Die equivalent to the Committed Capacity Amount of Die for the next [*] period. AMD shall manufacture and ship against each Purchase Order. Each Purchase Order shall indicate the then current Base Wafer Price and, if applicable, sorted Die price for each respective Process.

8.4.2 ACCEPTANCE. All Wafers and/or Die manufactured and delivered by AMD pursuant to Purchase Orders submitted by Vantis to AMD shall be counted as Purchased Products when delivered by AMD and accepted by Vantis pursuant to Article 7.3.2.

8.4.3 NO EFFECT ON THIS AGREEMENT. The terms of this Agreement shall govern any sales contract between the parties for the sale and purchase of the Wafers and/or Die. Any terms or conditions printed on the face or the reverse side of a Purchase Order or Communication shall not be part of this Agreement nor shall they constitute the terms and conditions of the sales contract for the Wafers even in the event that such Purchase Order or Communication is signed and returned by AMD to Vantis or Vantis to AMD.

9. FORECASTS; ACCEPTANCE; COMMITTED BUILD AMOUNT.

9.1. DIE DEMAND FORECASTS.

9.1.1 ANNUAL FORECASTS. At least six Months before the end of each AMD fiscal year, Vantis shall furnish AMD with a non-binding three-year forecast plan of Vantis' Die and Wafer demand needs by Process, with [*] detail Wafer demand for the first year and annual detail Wafer demand for each calendar year (each an "ANNUAL FORECAST"). The existing Annual Forecast for calendar years 1999, 2000 and 2001 is set forth on Schedule 9.1.1. By [*] of each calendar year, Vantis shall furnish AMD with a binding final update of the Annual Forecast.

9.1.2 ROLLING [*] FORECASTS. At least the amount of time equal to the applicable Process Forecast Lead Time prior to the end of each [*], Vantis shall provide AMD with a rolling [*] forecast plan of Vantis' Die and Wafer demand needs by Process, with [*] detail Die and Wafer demand for each [*] ("ROLLING [*] FORECAST"); PROVIDED, HOWEVER, that the Rolling [*] Forecast for [*] is set forth on Schedule 9.1.2.

9.2. ACCEPTANCE OF FORECASTED DIE DEMAND AMOUNTS.

9.2.1 AMD COMMUNICATION OF COMMITTED CAPACITY AMOUNTS.

(a) At least [*] weeks before the end of each calendar year, AMD shall send Vantis a written notification (a "COMMUNICATION") specifying for each year in the updated Annual Forecast provided by Vantis by October 1 of such year (1) for the years [*]: the amount of Wafers for each period in the Annual Forecast that AMD commits to fabricate, determined in accordance with Exhibit B (the "LONG-TERM COMMITTED CAPACITY AMOUNT") and (2) for the years [*]: the amount of Wafers for each period in the Annual Forecast that AMD, on a good-faith non-binding basis, is willing to fabricate. Any Communication responding to an Annual Forecast shall be signed by AMD's Group Vice President, Wafer Fabrication Group, or an officer of AMD holding similar functions.

(b) If for any year, the Long-Term Committed Capacity Amount for such year determined in accordance with Exhibit B would exceed the Maximum Committed Capacity Amount applicable to such year, (1) the Long-Term Committed Capacity Amount for such year shall equal the Maximum Committed Capacity Amount applicable to such year and (2) Vantis may request additional production capacity from AMD in accordance with Article 4.2.

(c) Within three weeks of AMD's receipt of Vantis' Rolling [*] Forecast, AMD shall send Vantis a Communication specifying for each [*] in such updated Rolling [*] Forecast provided by Vantis, the amount of Die and/or Wafers for each [*] in the Rolling [*] Forecast that AMD commits to fabricate, determined in accordance with Exhibit B (the "SHORT-TERM COMMITTED CAPACITY AMOUNT"). Any Communication responding to a Rolling [*] Forecast shall be signed by AMD's Director of Strategic Planning or any other representative of AMD authorized to sign such Communication on behalf of AMD.

(d) If for any [*], the Short-Term Committed Capacity Amount for such [*] determined in accordance with Exhibit B would exceed the Maximum Committed Capacity Amount applicable to such [*], (1) the Short-Term Committed Capacity Amount for such [*]

shall equal the Maximum Committed Capacity Amount applicable to such [*] and (2) Vantis may request additional production capacity from AMD in accordance with Article 4.2.

9.2.2 MINIMUM COMMITTED CAPACITY AMOUNTS.

(a) During the portion of the Term up to and including [*]: The Long-Term Committed Capacity Amount for each year in any Communication responding to a Annual Forecast shall not be less than the lower of (i) the Maximum Committed Capacity Amount applicable to such year or (ii) the Long-Term Committed Capacity Amount for such year specified by AMD in the Communication responding to the immediately preceding Annual Forecast (the "PRIOR LONG-TERM COMMITTED CAPACITY AMOUNT"); PROVIDED, HOWEVER, that if the forecasted die demand amount for such year (the "FORECASTED ANNUAL AMOUNT") is less than the lower of (I) the Maximum Committed Capacity Amount applicable to such year or (II) the Prior Long-Term Committed Capacity Amount for such year, the Long-Term Committed Capacity Amount for such year may be lower than the Maximum Committed Capacity Amount applicable to such year or Prior Long-Term Committed Capacity Amount, but in any event shall not be less than the Forecasted Annual Amount.

(b) During the portion of the Term up to and including [*]: The Short-Term Committed Capacity Amount for each [*] in any Communication responding to a Rolling [*] Forecast shall not be less than the lower of (i) the Long-Term Committed Capacity Amount specified for such [*] in the Communication responding to the Annual Forecast immediately preceding such Rolling [*] Forecast (the "BASE AMOUNT") or (ii) the Short-Term Committed Capacity Amount for such [*] specified by AMD in the Communication responding to the immediately preceding Rolling [*] Forecast (the "PRIOR SHORT-TERM COMMITTED CAPACITY AMOUNT"); PROVIDED, HOWEVER, that if the forecasted die demand amount for such [*] (the "FORECASTED AMOUNT") is less than the lower of (I) the Base Amount for such [*] or (II) the Prior Short-Term Committed Capacity Amount for such [*], the Short-Term Committed Capacity Amount for such [*] may be lower than the Base Amount or Prior Short-Term Committed Capacity Amount but in any event shall not be less than the appropriate percentage of the [*] Minimum for such [*] determined in accordance with Exhibit B.

(c) During the portion of the Term from and after [*]: The Short-Term Committed Capacity Amount for each [*] in any Communication responding to a Rolling [*] Forecast shall not be less than (i) the lower of the appropriate percentage of the [*] Minimum for such [*] determined in accordance with Exhibit B or (ii) the Prior Short-Term Committed Capacity Amount.

9.2.3 WAIVER OF PRIOR COMMITTED CAPACITY AMOUNTS.

(a) In the event that, in accordance with Article 9.2.2(a), the Long-Term Committed Capacity Amount for a [*] specified by Vantis is less than the Prior Long-Term Committed Capacity Amount for such year, AMD shall have the right to waive the Prior Long-Term Committed Capacity Amount for such year for purposes of calculating the Minimum Annual Purchased Capacity Amount of Wafers applicable to such year. Any such waiver shall be contained in writing in the Communication specifying the new Long-Term Committed Capacity Amount for such year.

(b) In the event that, in accordance with Article 9.2.2 (b) or (c), the Short-Term Committed Capacity Amount for a [*] specified by Vantis is less than the Prior Short-Term Committed Capacity Amount for such [*], AMD shall have the right to waive the Prior Short-Term Committed Capacity Amount for such [*] for purposes of calculating the [*] Minimum Quarterly Purchased Capacity Amount of Wafers applicable to such [*]. Any such waiver shall be contained in writing in the Communication specifying the new Short-Term Committed Capacity Amount for such [*].

9.2.4 DISPOSITION OF EXCESS WAFER CAPACITY. If, after Vantis delivers the latest Rolling [*] Forecast, a [*] Minimum applicable to any [*] is lower than the [*] Minimum previously applicable to such [*], but AMD does not waive the [*] Minimum for such [*] for purposes of calculating the Minimum [*] Purchased Capacity Amount of Wafers applicable to such [*], AMD shall use Commercially Reasonably Efforts to use, or cause to be used, the amount of production capacity that AMD would need to maintain to fabricate a quantity of Wafers equivalent to the difference between the [*] Minimum previously applicable to such [*] and the latest [*] Minimum.

9.3. COMMITTED BUILD AMOUNT; MAXIMUM COMMITTED BUILD AMOUNT. AMD shall set forth in each Communication responding to a Rolling [*] Forecast an amount of Wafers equal to [*] of the [*] Minimum for the next [*] that AMD shall fabricate (the "COMMITTED BUILD AMOUNT"). AMD shall not be under any obligation to set forth in any Communication a Committed Build Amount for the next [*] in excess of a Short-Term Committed Capacity Amount for such [*] specified in a Communication responding to a prior Rolling [*] Forecast.

9.4. COOPERATION CLAUSE. If and when requested by AMD, Vantis shall use Commercially Reasonable Efforts to submit its Die and/or Wafer demand needs to AMD in a format which is compatible with AMD's Total Order Management ("TOM") planning methodology.

10. SUPPLY EXCLUSIVITY

10.1. SUPPLY EXCLUSIVITY. During the Term AMD shall not, other than on behalf of Vantis pursuant to this Agreement, use any EE Process to manufacture Wafers for use in the production of Devices.

11. INTELLECTUAL PROPERTY; TRANSFER OF FABRICATION ACTIVITY; PROCESS SHARING.

11.1. INTELLECTUAL PROPERTY RIGHTS AND INDEMNITIES.

11.1.1 AMD'S MANUFACTURING RIGHTS. AMD warrants that it has all necessary rights to manufacture and sell to Vantis the Wafers.

11.1.2 AMD'S INDEMNIFICATION OF VANTIS. AMD will, at its sole cost and expense, indemnify, defend, and hold Vantis harmless from and against any cost, loss, expense, or liability arising from any actual or alleged infringement of any patent, mask work right, copyright, trademark, or other intellectual property right to the extent such actual or alleged infringement arises from AMD Processes.

11.1.3 VANTIS' INDEMNIFICATION OF AMD. Vantis will, at its sole cost and expense, indemnify, defend, and hold AMD harmless from and against any cost, loss, expense, or liability arising from any actual or alleged infringement of any patent, mask work right, copyright, trademark, or other intellectual property right to the extent such actual or alleged infringement arises from AMD's compliance with any of Vantis' designs, specifications, instructions, or other contribution of Vantis to the design (or AMD's manufacture or sale) of Wafers for (or to) Vantis. The foregoing indemnification shall not apply to any liability arising prior to the Closing Date or to any claims based on any act or omission occurring prior to the Closing Date.

11.1.4 INDEMNIFICATION PROCEDURE. The indemnifying party shall defend, at its sole costs and expense, including attorneys' fees, any action brought against the indemnified party alleging any such infringement, and the indemnified party agrees (i) to give prompt notice of any such action to the indemnifying party, (ii) to allow the indemnifying party, through competent counsel of its choice (and personally acceptable to the indemnified party), to defend such action, and (iii) to provide the indemnifying party all reasonable information, assistance, and authority requested by the indemnifying party, at the indemnifying party's expense, for the indemnifying party to defend such action.

11.1.5 MITIGATION. In the event that an injunction is issued in support of the infringement claim or the indemnified party otherwise reasonably believes that the infringement claim is likely to be upheld: (a) the indemnifying party shall, at its expense, use Commercially Reasonable Efforts to avoid the infringement claim, either by modifying its technology and/or design or by obtaining a license or nonassertion covenant from the claimant; (b) if Vantis is the indemnified party, it shall have the right to return any allegedly infringing Products to AMD and receive a full refund for the cost to Vantis of the Die contained in such Products; and (c) if AMD is the indemnified party, it shall have the right to stop production of any allegedly infringing Wafers by giving written notice to Vantis, and Vantis shall pay AMD for all Wafers started prior to such notice at the established purchase price (such purchase price to be prorated based on the percentage of completion of such Wafers).

11.1.6 GENERAL. The foregoing Article 11.1 states the entire obligation and the exclusive remedy of each party with respect to any alleged infringement of intellectual property rights by any Wafer furnished under this Agreement.

11.2. AMD INITIATED TRANSFER OF WAFER FABRICATION BETWEEN AMD FACILITIES; SALE/SHUTDOWN OF A FACILITY.

11.2.1 AMD'S RIGHT TO TRANSFER. Subject to Article 7.2.5(d), AMD may at any time transfer any portion of its wafer fabrication activity hereunder from one Facility to another Facility.

11.2.2 RESPONSIBILITY FOR TRANSFER OF PROCESSES BETWEEN AMD'S FACILITIES. If AMD initiates a transfer of any portion of its wafer fabrication activity hereunder from one Facility to another Facility, AMD shall be responsible for effecting the transfer of any Process associated with such fabrication to the new Facility and otherwise implementing such Process in the new Facility, and AMD shall bear [*] costs and expenses associated with such transfer, including mask tooling expenses and Process and Product qualification costs for Vantis' Products (including the cost of Wafers used in the qualification process, assembly and test

expenses related to qualifying Wafers and reliability expenses). AMD shall provide Vantis engineering support [*] to assist Vantis in the Process and Product qualifications related to such transfer and to otherwise assist Vantis in the implementation in the new Facility of each Process transferred.

11.2.3 SALE OF A FACILITY. If AMD sells or otherwise transfers the rights to operate a Facility to a third party (other than Lattice), an express condition to the consummation of such transaction shall be the assumption by the third party for the remaining Term of this Agreement of AMD's obligations under this Agreement with respect to the Products fabricated in such Facility at the time of consummation of such transaction, including without limitation AMD's commitment to reserve capacity at such Facility sufficient to fabricate an amount of Die equivalent to the Committed Capacity Amount of Die each [*] relating to any affected Products. Vantis shall have the right to approve any potential purchaser or operator of a Facility that is a Direct Competitor of Vantis; PROVIDED, HOWEVER, that Vantis' approval of any such third party shall not be unreasonably withheld.

11.2.4 CONTINUED SUPPLY OBLIGATION AFTER FACILITY SHUTDOWN. If AMD elects to close any Facility or cease all Wafer fabrication activities at any Facility, AMD remains subject to its obligations under this Agreement with respect to any affected Products, including without limitation AMD's commitment to reserve capacity at its other Facilities sufficient to fabricate an amount of Die equivalent to the Committed Capacity Amount of Die each [*] relating to any affected Products and AMD's obligation to fabricate and deliver to Vantis an amount of Die equivalent to the Committed Build Amount of Die for each [*] relating to any affected Products.

11.2.5 TRANSFER OF [*] PROCESS FROM [*] TO [*]. Pursuant to Article 7.2.5(d), Vantis hereby approves the transfer of the [*] Process and all related Product Wafer fabrication activities from [*] to [*]. In accordance with Article 11.2.2, AMD shall be responsible for effecting the transfer of the [*] Process associated with such fabrication to [*] and otherwise implementing such Process in [*], and AMD shall bear all costs and expenses associated with such transfer. AMD shall use Commercially Reasonable Efforts to complete all Process and Product Qualifications related to such transfer by December 31, 1999. Within one calendar quarter after the Month in which all Process and Product Qualifications are completed in [*], the cycle time in [*] shall be as specified in Exhibit C. Until completion of all [*] Process and Product Qualifications in [*], the performance metrics specified in Exhibit C for [*] shall continue to be effective and AMD shall continue to reserve capacity at [*] sufficient to fabricate an amount of Die equivalent to the Short-Term Committed Capacity Amount of Die each month relating to any Products affected by the Transfer of the [*] Process from [*] to [*].

11.3. VANTIS INITIATED TRANSFER OF WAFER FABRICATION OUT OF AMD FACILITIES.

11.3.1 VANTIS' RIGHT TO TRANSFER.

(a) [*] PROCESSES. Subject to Article 11.3.1(b), Vantis may at any time designate a third party to fabricate on behalf of Vantis, pursuant to [*] Processes, semiconductor wafers for which the designs, specifications and working drawings for the wafers are furnished by, and originate with, Vantis or were prepared by a contractor of Vantis on behalf of Vantis, and

such designs, specifications and working drawings are in sufficient detail that no additional designing by the manufacturer is required other than adaptation to the production processes and standards normally used by the manufacturer which changes the characteristics of the wafers only to a negligible extent.

(b) AMD'S RIGHT TO APPROVE VANTIS TRANSFEREES.

(1) [*] AND LOWER PROCESSES. AMD shall have no right to approve any third party designated by Vantis pursuant to Article 11.3.1(a) to fabricate semiconductor wafers pursuant to [*] Processes.

(2) [*] PROCESSES. Until September 30, 1999, AMD shall have the right to approve any third party designated by Vantis pursuant to Article 11.3.1(a) to fabricate semiconductor wafers pursuant to [*] Process; PROVIDED, HOWEVER, that AMD's approval of any such third party shall not be unreasonably withheld. Thereafter, AMD shall have no right to approve any third party designated by Vantis to fabricate semiconductor wafers pursuant to [*] Processes.

11.3.2 RESPONSIBILITY FOR TRANSFER OF PROCESSES INTO THIRD PARTY FACILITIES (TRANSFER INITIATED BY VANTIS). In the event that Vantis enters into a contract in accordance with Article 11.3.1(a) for the fabrication by a third party of semiconductor wafers pursuant to [*], Vantis shall be responsible for effecting the transfer of any Process associated with such fabrication to the third party and otherwise implementing such Process in the third party's fabrication facilities, and Vantis shall bear all costs and expenses associated with such transfer, including the Process and Product qualification costs for Vantis' Products; PROVIDED, that AMD shall have no obligation to make any modifications to any Process in connection with implementation of any such Process in a third party's fabrication facilities.

11.3.3 EFFECT OF TERMINATION ON TRANSFERRED PROCESSES. The termination of this Agreement shall not affect the continued use of any Process to fabricate wafers on behalf of Vantis implemented in, or being transferred to, a third party's fabrication facilities at the time of such termination; PROVIDED, that, upon termination of this Agreement, AMD shall not be obligated to further assist Vantis with the transfer of any Process which is in the course of being transferred into a third party's fabrication facilities at the time of such termination.

12. CONFIDENTIAL INFORMATION

12.1. CONFIDENTIAL INFORMATION. Each party acknowledges that the information disclosed in connection with any transactions between the parties, including any transactions contemplated by the Related Agreements, may contain confidential information, know-how and trade secrets of the disclosing party ("CONFIDENTIAL INFORMATION"), and that any such Confidential Information shall remain the property of the disclosing party. A recipient party shall use Commercially Reasonable Efforts to keep and hold any such Confidential Information of the disclosing party in strict confidence as it would its own similar Confidential Information and shall not disclose such Confidential Information of the disclosing party to any Person without the prior written consent of the disclosing party, except as provided herein. A recipient party shall not, except as may be authorized by the disclosing party in writing or by the express terms of any of the Related Agreements, use any Confidential Information of the disclosing party

except for the purpose for which it was disclosed in connection with the Related Agreements. Notwithstanding the foregoing, no written information shall be considered Confidential Information unless identified and marked as confidential. Information disclosed orally or visually under circumstances reasonably identifying such information as confidential shall be presumed to be Confidential Information unless otherwise agreed in writing by both parties.

12.2. EMPLOYEES AND CONSULTANTS. A recipient party shall limit dissemination of and access to any Confidential Information of the disclosing party to those employees or consultants of the recipient party who have a good faith need for such access to effectuate a transaction between the parties, including any transactions contemplated by the Related Agreements, and who have executed a standard nondisclosure agreement with the recipient party.

12.3. SURVIVAL. Each party agrees to maintain confidentiality in a manner given to such party's own similar Confidential Information for two years after the date of expiration or termination of the last of the Related Agreements to expire or terminate.

12.4. SUBCONTRACTORS. The recipient party may disclose Confidential Information to subcontractors performing services for the recipient party, to the extent such disclosure is necessary to perform the recipient party's duties in a transaction between the parties, including any transactions contemplated by the Related Agreements. The recipient party shall cause its permitted subcontractors to sign a confidentiality agreement with the recipient party in substantially the same terms and conditions of this Article 12 prior to disclosing Confidential Information of the disclosing party to such subcontractors.

12.5. PERMITTED DISCLOSURE. Neither party shall have any obligation to the other party with respect to any Confidential Information of the other party or any portion thereof which:

(a) is or hereafter becomes publicly known through no wrongful act of the first party;

(b) is rightfully received from a third party without restriction on disclosure and without breach of this Agreement;

(c) is now or hereafter independently developed by the first party and without reliance in any degree upon any Confidential Information of the other party; or

(d) is revealed by the first party pursuant to a requirement of a governmental agency or law, provided that the first party provides prompt written notice of such requirement or law so as to afford the other party an opportunity to intervene and oppose disclosure.

12.6. REMEDIES. The parties agree that any material breach of this Article 12 shall cause irreparable injury and that, notwithstanding any dispute resolution provisions herein to the contrary, injunctive relief in a court of competent jurisdiction shall be appropriate to prevent either an initial or continuing breach of such nondisclosure and confidentiality provisions herein in addition to any other relief to which the owner of such Confidential Information may be entitled.

12.7 RESIDUALS. Notwithstanding any other provision of this Agreement, the recipient party shall be free to use Residuals for any purpose; PROVIDED that the recipient party shall

maintain the confidentiality of Confidential Information as set forth herein. For purposes hereof, "RESIDUALS" shall mean information retained in the unaided memory of an individual who has had access to or worked with Confidential Information, unless such individual has made a conscious attempt to memorize such Confidential Information for purposes of applying this Article 12.7. The foregoing shall not be deemed to grant to the recipient party a license under the disclosing party's intellectual property.

13. TERM AND TERMINATION OF AGREEMENT

13.1. TERM; RENEWAL BY MUTUAL AGREEMENT. The term of this Agreement (the "TERM") shall commence on the date first written above and expire at 11:59 p.m. on [*] (the "EXPIRATION DATE"), unless terminated earlier pursuant to Article 13.2, 13.3, 13.4 or 13.5. Either party may, by written notice to the other party delivered no earlier than [*] calendar months before the Expiration Date, propose that the Expiration Date be extended on mutually agreeable terms, unless terminated earlier pursuant to Article 13.2, 13.3, 13.4 or 13.5. This Agreement shall terminate on the originally scheduled Expiration Date, unless the parties agree in writing no later than [*] calendar months before the Expiration Date upon the terms and conditions of such an extension of the Expiration Date.

13.2. IMMEDIATE TERMINATION EVENTS. Either party may terminate or suspend this Agreement immediately and without liability upon written notice to the other party if any one of the following events occurs:

(a) the other party files a voluntary petition in bankruptcy or otherwise seeks protection under any law for the protection of debtors;

(b) a proceeding is instituted against the other party under any provision of any bankruptcy law which is not dismissed within ninety (90) days;

(c) the other party is adjudged bankrupt;

(d) a court assumes jurisdiction of all or a substantial portion of the assets of the other party under a reorganization law;

(e) a trustee or receiver is appointed by a court for all or a substantial portion of the assets of the other party;

(f) the other party becomes insolvent or ceases or suspends all or substantially all of its business; or

(g) the other party makes an assignment of the majority of its assets for the benefit of creditors.

13.3. TERMINATION UPON CHANGE IN CONTROL TO A DIRECT COMPETITOR. Within 5 days of the earlier of (a) the signing of definitive documentation relating to a proposed Change in Control of Vantis or its ultimate parent entity or (b) the consummation of a Change in Control of Vantis or its ultimate parent entity, Vantis shall provide AMD with written notice of such event. Within 15 days of the receipt of such notice, AMD may then immediately terminate this Agreement in accordance with the provisions of Article 13.6 by providing Vantis with written

notice of AMD's determination that the acquirer or proposed acquirer of Vantis or its ultimate parent entity is a Direct Competitor of AMD.

13.4. TERMINATION FOR BREACH. Except as provided in Articles 4.3.2, 6 and 11.1.6, if AMD fails to perform or violates any material obligation of this Agreement or Vantis fails to pay an invoice within [*] of the due date for such invoice, then the parties shall first attempt in good faith to resolve such breach pursuant to the dispute resolution process specified in Article 14.2. Thirty days after delivery of written notice to the breaching party that a breach described in this Article 13.4 has occurred, the non-breaching party may terminate this Agreement without liability for such termination; PROVIDED, that if the breaching party has begun substantial corrective action to remedy the breach, the non-breaching party may only terminate this Agreement without liability for such termination [*] days after delivery of its written notice to the breaching party, if such breach remains uncured as of such date; PROVIDED, HOWEVER, that if allowing [*] for the breaching party to cure the breach would cause irreparable harm to the business prospects of the non-breaching party, notwithstanding any dispute resolution provisions herein to the contrary, temporary or preliminary injunctive relief in a court of competent jurisdiction shall be appropriate to prevent either an initial or continuing breach in addition to any other relief to which the non-breaching party may be entitled.

13.5. TERMINATION BY VANTIS ON [*] NOTICE. At any time, Vantis may unilaterally terminate this Agreement, without liability, upon [*] prior written notice to AMD.

13.6. RAMPDOWN UPON CERTAIN TERMINATION EVENTS. In the event that AMD terminates this Agreement pursuant to Article 13.3 or Vantis terminates this Agreement pursuant to Article 13.5:

(a) the Minimum [*] Purchased Amount applicable to the [*] in which the notice of termination is received (the "TERMINATING [*]") shall remain unchanged;

(b) the Minimum [*] Purchased Capacity Amounts applicable to the [*] remaining in the Term (other than the Terminating [*]) shall be restated to ramp down linearly from the Short-Term Committed Capacity Amount of Die in the Terminating [*] as follows:

Minimum [*] Purchased Capacity Amounts as a Percentage of Short-Term Committed Capacity Amount of Die in the Terminating [*]

[*]	PERCENT
[*]	[*]%
[*]	[*]%
[*]	[*]%
[*]	[*]%
[*]	[*]%

13.7. ADDITIONAL REMEDY OF AMD. In the event AMD terminates this Agreement as provided in Article 13.2 or 13.4, AMD, upon written notice to Vantis, may also declare immediately due and payable from Vantis, in whole or in part, (a) all unpaid obligations, and prorated portions thereof, of Vantis to AMD hereunder and (b) reimbursement for all reasonable

direct costs and expenses incurred by AMD in connection with the termination of work then in progress.

13.8. ADDITIONAL REMEDY OF VANTIS. In the event Vantis terminates this Agreement as provided in Article 4.3.2, 4.3.5, 13.2, 13.4 or 13.5, Vantis, upon written notice to AMD, may also remove the Wafer Sort Equipment from the Facilities, on or after the termination of this Agreement, in its then "as is" condition. Vantis shall be responsible to pay the reasonable cost to remove the Wafer Sort Equipment from the Facilities and to return any affected portion of the Facilities to good order (normal wear and tear excepted) and in a structurally sound condition (and shall post a bond or deposit reasonably adequate to do so, prior to commencing removal). Any immaterial components, parts or items of the Wafer Sort Equipment which no longer exist at such time shall no longer be considered part of the Wafer Sort Equipment.

13.9. SURVIVAL OF OBLIGATIONS. The following Articles shall survive any expiration, termination or cancellation of this Agreement, and the parties shall continue to be bound by the terms and conditions thereof: 10, 11, 12, 13.7, 13.8 and 13.9.

14. MISCELLANEOUS

14.1. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the laws of the State of California, without reference to or application of conflicts of law principles.

14.2. DISPUTE RESOLUTION. The parties shall attempt in good faith to resolve any dispute arising out of or relating to this Agreement or the Exhibits and Schedules attached hereto. In particular, those executives of the respective parties who have authority to settle the controversy and have direct responsibility for administration of the relationships established pursuant to this Agreement shall attempt in good faith to negotiate a settlement pursuant to the following process:

14.2.1 Any party having a dispute or claim shall give the other party written notice stating the nature of the dispute in reasonable detail. Within five business days after delivery of the notice, the receiving party shall submit to the other a written response also in reasonable detail. Within five business days after delivery of the written response, decisionmakers from both parties shall meet (in person or by telephone) at a mutually acceptable time and place (including telephonic conference), and thereafter as often as they reasonably deem necessary, to attempt to resolve the dispute. All reasonable requests for information made by one party to the other shall be honored.

14.2.2 If the matter has not been resolved by the persons referred to above within ten days of the first meeting of such persons, the dispute shall be referred to more senior executives of each party who have authority to settle the dispute and who shall likewise meet (in person or by telephone) to attempt to resolve the dispute. Within five business days after the referral of the dispute to more senior executives of each party, the senior executives of both parties shall meet at a mutually acceptable time and place (including telephonic conference), and thereafter as often as they reasonably deem necessary, to attempt to resolve the dispute.

14.2.3 If the matter has not been resolved within ten days from the referral of the dispute to such senior executives, then the parties may pursue litigation or, if mutually agreed, alternative dispute resolution mechanisms.

14.3. NO CONSEQUENTIAL DAMAGES. IN NO EVENT SHALL EITHER PARTY BE LIABLE TO THE OTHER PARTY FOR ANY INDIRECT, SPECIAL, CONSEQUENTIAL OR INCIDENTAL DAMAGES (INCLUDING LOST PROFITS) WHETHER BASED ON WARRANTY, CONTRACT, TORT OR ANY OTHER LEGAL THEORY REGARDLESS OF WHETHER SUCH PARTY HAD ACTUAL OR CONSTRUCTIVE NOTICE OF SUCH DAMAGES.

14.4. INJUNCTION. Either party may seek a preliminary injunction or other preliminary judicial relief if, in its judgment, such action is necessary to avoid irreparable damage.

14.5. ASSIGNMENT. Without the prior written consent of the other party, which consent may not be unreasonably withheld, neither party, either voluntarily or by operation of law, shall assign, transfer or otherwise dispose of (collectively "Transfer") this Agreement in whole or in part; PROVIDED, HOWEVER, that this Agreement may be Transferred (i) without the consent of a party, to any subsidiary of the other party; (ii) without the consent of AMD, by Vantis to Lattice, or any affiliate controlled by Lattice; (iii) without the consent of Vantis, in connection with a Change in Control of AMD; and (iv) without the consent of AMD, in connection with a Change in Control of Vantis or its ultimate parent entity. Any attempted or purported Transfer of this Agreement which does not comply with this Article 14.5 shall be null and void, have no force or effect, and confer no rights upon any third parties. Subject to compliance with the provisions of this Article 14.5, the provisions of this Agreement shall be binding upon and inure to the benefit of the parties and their respective successors, assigns and Transferees.

14.6. PUBLIC ANNOUNCEMENTS. Neither party shall publicly disclose the terms and conditions of this Agreement without first submitting the text of such announcement to the other party and receiving the approval of the other party of such text, which approval, unless public disclosure is required by a court or a government agency, may be withheld for any reason. However, either party or Lattice may disclose the existence and the terms of this Agreement (i) in a registration statement or other document filed by either party or Lattice with the Securities and Exchange Commission, (ii) in accordance with generally accepted accounting procedures if required under the rules of the Securities and Exchange Commission or National Association of Securities Dealers Automated Quotation System or (iii) in connection with any confidential due diligence necessary and associated with a financing, Change in Control or other significant corporate transaction not in the ordinary course, and such disclosure is reasonably required for the accomplishment of the transaction.

14.7. NOTICE AND COMMUNICATIONS. All notices and other communications hereunder shall be in writing and shall be sent by personal delivery, by telecopy, or by registered or certified mail (return receipt requested). Notice shall be deemed to have been duly given (a) upon receipt if delivered personally, (b) upon completion of the transmission if telecopied (with confirmation from the sending device that the entire notice or other communication was received by the addressee) or (c) upon execution of the return receipt if mailed by registered or certified mail (return receipt requested); in each case, the notice or other communication must be directed to the parties at the following addresses (or at such other address for a party as shall be specified

by like notice):

To AMD:

P.O. Box 3453
Sunnyvale, California 94088-3453
Attention: General Counsel
Facsimile: (408) 774-7399

To Vantis:

995 Stewart Drive
Sunnyvale, California 94088
Attention: Director of Legal Affairs
Facsimile: (408) 616-7800

With a copy to:

Lattice Semiconductor Corporation
5555 NE Moore Court
Hillsboro, Oregon 97124
Attention: General Counsel
Facsimile: (503) 268-8077

14.8. RELATIONSHIP OF THE PARTIES. At such time or times as AMD directly or indirectly owns or controls less than 100% of the ownership rights of Vantis: (i) AMD and Vantis shall be independent contractors and neither of them shall be nor represent themselves to be the legal agent, partner or employee of the other party for any purpose; (ii) neither party has the authority to make any warranty or representation on behalf of the other party nor to execute any contract or otherwise assume any obligation or responsibility in the name of or on behalf of the other party; and (iii) neither party shall be bound by, nor liable to, any third Person for any act or any obligation or debt incurred by the other party, except to the extent specifically agreed to in writing by the parties.

14.9. WAIVER. Failure by either party, at any time, to require performance by the other party or to claim a breach of any provision of this Agreement shall not be construed as a waiver of any right accruing under this Agreement, nor shall it affect any subsequent breach or the effectiveness of this Agreement or any part hereof, or prejudice either party with respect to any subsequent action. A waiver of any right accruing to either party pursuant to this Agreement shall not be effective unless given in writing.

14.10. SEVERABILITY. In the event that any provision of this Agreement shall be unlawful or otherwise unenforceable, such provision shall be severed, and the entire agreement shall not fail on account thereof, the balance continuing in full force and effect, and the parties shall endeavor to replace the severed provision with a similar provision that is not unlawful or otherwise unenforceable.

14.11. RIGHTS AND REMEDIES CUMULATIVE. Except to the extent expressly set forth to the contrary in Articles 4.3.3, 4.3.5, 6, and 11.1.6 the rights and remedies provided herein shall be cumulative and not exclusive of any other rights or remedies provided by law or otherwise.

14.12. HEADINGS. The Article headings in this Agreement are for convenience only, and shall not be considered a part of, or affect the interpretation of, any provision of this Agreement.

14.13. NO THIRD-PARTY BENEFICIARIES. No Person not a party to this Agreement, other than Lattice, shall have any rights under this Agreement as a third-party beneficiary or otherwise other than Persons entitled to indemnification as expressly set forth herein.

14.14. FORCE MAJEURE.

14.14.1 "Force Majeure" shall mean causes beyond the reasonable control of a party, including, without limitation, acts of God; acts of a public enemy; war; rebellion; insurrection; riot; epidemic; quarantine restrictions; acts of any governmental authority or any political subdivision or any department or regulatory agency thereof or entity created thereby; orders of any court or arbitral body, acts of any Person or Persons engaged in subversive activity or sabotage; fires, floods, explosions, storms, earthquakes, or other catastrophes; strikes or labor disputes; embargoes; unavoidable delays or inability to obtain equipment, labor, fuel, steam, water, electricity or materials or anything else necessary to operate the Facilities.

14.14.2 In the event either party hereto is prevented or delayed in the performance of any material term, condition or obligation under this Agreement (other than the payment of money) due to Force Majeure, such party shall give prompt notice to the other of the commencement, expected duration and termination of any such Force Majeure contingency. Except as otherwise provided below, such party's nonperformance shall be excused and the time for performance extended for the period of delay or inability to perform due to such Force Majeure.

14.14.3 Notwithstanding Article 14.14.2, whenever the total of all periods of delay or inability to perform due to Force Majeure exceeds 30 days, the party not failing to perform due to Force Majeure shall have the right to either terminate this Agreement or continue to excuse the other's nonperformance and extend the time for such party's performance for the period or periods of any delay or inability to perform due to Force Majeure.

14.14.4 Any termination of this Agreement pursuant to this Article 14.14 shall be without liability to either party and, upon such termination, all prior nonperformance of AMD, Vantis or both AMD and Vantis due to Force Majeure shall be excused.

14.14.5 Whenever possible, the party claiming a Force Majeure shall endeavor to use reasonable diligent efforts to perform in spite of the Force Majeure.

14.15. COUNTERPARTS. This Agreement may be executed in any number of counterparts, each of which shall be an original, with the same effect as if the signatures thereto and to this Agreement were upon the same instrument.

14.16. INTEGRATION. This Agreement sets forth the entire agreement and understanding between the parties as to its subject matter and supersedes all prior agreements, understandings

and negotiations, both written and oral, between the parties with respect thereto. No amendments or supplements to this Agreement shall be effective for any purpose unless executed in writing by the parties.

14.17. EXPORT CONTROL.

14.17.1 PRODUCTS AND TECHNICAL DATA. Each party hereby assures the other that it shall not knowingly, without prior authorization of the Office of Export Administration of the U.S. Department of Commerce, if required, export or re-export (as defined in Section 779.1 (b)-(c) of the Export Administration Regulations and any amendments thereto) technical data relating to this Agreement or direct products thereof.

14.17.2 OTHER RESTRICTIONS. In exercising its rights under this Agreement, each party agrees to comply strictly and fully with all other export controls imposed on technology and products by any country or organization or nations within whose jurisdiction each party operates or does business. Each party agrees not to export or permit export of any technical data relating to this Agreement or any direct product of any such technical data, without complying with the export control laws in the relevant jurisdiction.

14.18. NO IMPLIED LICENSES. No licenses are granted hereunder by implication, estoppel or otherwise. Each party may make reasonable references by name to any other party in its advertising material relative to Wafers, provided that the advance written consent of an authorized representative of the other party has been obtained.

IN WITNESS WHEREOF, the parties have signed this Agreement as of the date first above written.

ADVANCED MICRO DEVICES, INC.

By: /s/ Richard Previte

Name: Richard Previte
Title: President and Co-Chief Operating Officer

VANTIS CORPORATION

By: /S/ Frank Barone

Name: Frank Barone
Title: Acting President and Chief Operating Officer

EXHIBIT A

[CONTENTS OF TABLE REDACTED]

EXHIBIT B

MINIMUM [*] PURCHASED CAPACITY AMOUNT
SHORT-TERM COMMITTED CAPACITY AMOUNT
MINIMUM ANNUAL PURCHASED CAPACITY AMOUNT
LONG-TERM COMMITTED CAPACITY AMOUNT

1) NOTE. For capacity planning purposes, Vantis' die demand will be converted to equivalent Wafer demand using the current AMD NDW planning yields by Product.

2) [*] TAKE OR PAY/SHORT-TERM COMMITTED CAPACITY AMOUNT. In accordance with the terms of the Agreement, Vantis must purchase the following amount of each Rolling [*] Forecast, and AMD must reserve the following amount of capacity at the Facilities for each [*] in such forecast.

MONTHLY

MONTH IN FORECAST	TAKE OR PAY PURCHASE OBLIGATION [*] MINIMUM (SHOWN AS A % OF [*] ROLLING FORECAST)	SHORT-TERM COMMITTED CAPACITY AMOUNT (SHOWN AS A % OF [*]MINIMUM)
M1		
M2		
M3	[CONTENTS OF TABLE REDACTED]	
M4		
M5		
M6		

[REMAINDER OF PAGE INTENTIONALLY LEFT BLANK]

EXHIBIT B (CONTINUED)

3) ANNUAL TAKE OR PAY/LONG-TERM COMMITTED CAPACITY AMOUNT. In accordance with the terms of the Agreement, Vantis must purchase the following amount of each Annual Forecast, and AMD must reserve the following amount of capacity at the Facilities for each year in such forecast:

ANNUAL

TAKE OR PAY PURCHASE OBLIGATION

Operative Period	Year in Forecast	Minimum Annual Purchased Capacity Amount (shown as a % of Annual Forecast)	LONG-TERM COMMITTED CAPACITY AMOUNT NOTE: ONLY OPERATIVE [*]
		(1)	
		[CONTENTS OF TABLE REDACTED]	

- ---

(1) Because of the anticipated time of effectiveness of the Agreement, this percentage, instead of being a percentage of the total [*] Forecast for [*], shall be a percentage of the aggregate amount of the Rolling [*] Forecast for the period [*]. The Rolling [*] Forecast for the period [*] is attached to the Agreement as Schedule 9.1.2.

EXHIBIT C
MANUFACTURING PERFORMANCE METRICS
[*]

PROCESS YIELD (%)

[*]	[*]	[*]

[CONTENTS OF TABLE REDACTED]

CYCLE TIME (DAYS)

[*]	[*]	[*]

[CONTENTS OF TABLE REDACTED]

PERFORMANCE TO MIX*

[*]	[*]	[*]

[CONTENTS OF TABLE REDACTED]

* Based on current Perf-to-Mix methodology, TOM will have different baselines.

SORT EQUIPMENT AVAILABILITY

[CONTENTS OF TABLE REDACTED]

THEORETICAL CYCLE TIME (DAYS)

[CONTENTS OF TABLE REDACTED]

[Confidential Treatment Request]

SCHEDULE 7.8.1(a)
VANTIS WAFER SORT EQUIPMENT

ASSET #	DESCRIPTION	INSTALL DT	CAP BASE	BOOK VALUE	SERIAL #

[CONTENTS OF TABLE REDACTED]

EXHIBIT E

BASE WAFER PRICE TABLE

[CONTENTS OF TABLE REDACTED]

WAFER SORT PRICE TABLE

[CONTENTS OF TABLE REDACTED]

SCHEDULE 2.29

Maximum Committed Capacity Amount
[*]

WAFER OUTS (K)	[*]	[*]	[*]

[CONTENTS OF TABLE REDACTED]

* Estimated by Vantis as of April 19, 1999

SCHEDULE 9.1.1

Existing Annual Forecast
[*]

WAFER OUTS (K)	[*]	[*]	[*]

[CONTENTS OF TABLE REDACTED]

(1)

- ---
(1): The Die Outs and Wafer Outs shown for [*] will be fabricated in [*] until completion of all [*] Process and Product Qualifications in the SDC. Thereafter, the Die Outs and Wafer Outs shown for [*] will be fabricated in the [*].

[Confidential Treatment Request]

SCHEDULE 9.1.2

Rolling [*] Forecast*
([*])

DIE OUTS (K)	[*]	[*]	[*]	[*]	[*]	[*]

[CONTENTS OF TABLE REDACTED]

(1)

WAFER OUTS	[*]	[*]	[*]	[*]	[*]	[*]

[CONTENTS OF TABLE REDACTED]

(1)

- ---------------------------
(1): The Die Outs and Wafer Outs shown for [*] will be fabricated in [*] until completion of all [*] Process and Product Qualifications in the SDC. Thereafter, the Die Outs and Wafer Outs shown for [*] will be fabricated in the [*].

[Confidential Treatment Request]

SCHEDULE 9.2.1

Existing Long-Term Committed Capacity Amount)
[*]

WAFER OUTS (K)	[*]	[*]	[*]

[CONTENTS OF TABLE REDACTED]

(1)

- ---------------------------
(1): The Die Outs and Wafer Outs shown for [*] will be fabricated in [*] until completion of all [*] Process and Product Qualifications in the SDC. Thereafter, the Die Outs and Wafer Outs shown for [*] will be fabricated in the [*].

FIRST AMENDMENT TO

AMENDED AND RESTATED WAFER FABRICATION AGREEMENT

This FIRST AMENDMENT TO AMENDED AND RESTATED WAFER FABRICATION AGREEMENT ("Amendment") is entered into as of the 24th day of September, 1999, by and between ADVANCED MICRO DEVICES, INC., a Delaware corporation having its principal place of business at One AMD Place, Sunnyvale, California 94088 ("AMD"), and VANTIS CORPORATION, a Delaware corporation having its principal place of business at 995 Stewart Drive, Sunnyvale, California 94088 ("Vantis"). Unless otherwise defined herein, capitalized terms used herein shall have the respective meanings assigned to them in the Amended and Restated Wafer Fabrication Agreement, dated as of April 21, 1999, by and between AMD and Vantis (the "Wafer Fab Agreement").

RECITALS

A. AMD and Vantis entered into the Wafer Fab Agreement, whereby AMD agreed to fabricate certain semiconductor devices for Vantis.

B. AMD and Vantis desire to amend certain terms of the Wafer Fab Agreement.

AGREEMENT

Now, therefore, in consideration of the premises and for other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the parties agree as follows:

1. AMENDMENT

a. EXPECTED NET DIE PER WAFER. The Expected Net Die Per Wafer set forth on Exhibit A - Expected Net Die Per Wafer for the following devices: [*], in the third and fourth fiscal quarters of 1999, shall be deleted in their entirety and replaced with the Net Die Per Wafer set forth in the table below.

TECHNOLOGY	DEVICE	NET DIE PER WAFER
[*]	[*]	[*]
	[*]	[*]
	[*]	[*]
[*]	[*]	[*]
	[*]	[*]
[*]	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]

[Confidential Treatment Request]

B. BASE DIE PRICE TABLE. The Base Die Price set forth on Exhibit F - Base Die Price Table for the following devices: [*], in the third and fourth fiscal quarters of 1999, shall be deleted in their entirety and replaced with the Base Die Price set forth in the table below.

TECHNOLOGY	DEVICE	BASE DIE PRICE ($)
[*]	[*]	[*]
	[*]	[*]
	[*]	[*]
[*]	[*]	[*]
	[*]	[*]
[*]	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]

c. REFERENCES WITHIN THE WAFER FAB AGREEMENT. Each reference in the Wafer Fab Agreement to "this Agreement" and the words "hereof," "herein" and "hereunder," or words of like import, shall mean and be a reference to the Wafer Fab Agreement as amended by this Amendment.

2. MISCELLANEOUS

a. WAFER FAB AGREEMENT OTHERWISE NOT AFFECTED. Except as expressly amended pursuant hereto, the Wafer Fab Agreement shall remain unchanged and in full force and effect and is hereby ratified and confirmed in all respects.

b. AMENDMENT AND WAIVERS. The provisions of this Amendment may only be amended or waived in accordance with the terms of the Wafer Fab Agreement.

c. SUCCESSORS AND ASSIGNS. The provisions of this Amendment shall be binding upon and inure to the benefit of the parties hereto and their respective successors and assigns.

d. COUNTERPARTS. This Amendment may be executed in any number of counterparts, each of which shall be an original, with the same effect as if the signatures thereto and to this Amendment were upon the same instrument.

e. SEVERABILITY. In the event that any provision of this Amendment shall be unlawful or otherwise unenforceable, such provision shall be severed, and the entire agreement shall not fail on account thereof, the balance continuing in full force and effect, and the parties shall endeavor to replace the severed provision with a similar provision that is not unlawful or otherwise unenforceable.

f. NO THIRD-PARTY BENEFICIARIES. No person not a party to this Amendment shall have any rights under this Amendment as a third-party beneficiary or otherwise other than persons or entities entitled to indemnification as expressly set forth herein.

g. GOVERNING LAW. This Amendment shall be governed by and construed in accordance with the laws of the State of California, without reference to conflicts of law principles.

h. INTEGRATION. This Amendment sets forth the entire agreement and understanding between the parties as to its subject matter and supersedes all prior agreements, understandings and memoranda between the parties. No amendments or supplements to this Amendment shall be effective for any purpose except by a written agreement signed by the parties.

[THIS SPACE INTENTIONALLY LEFT BLANK]

IN WITNESS WHEREOF, the parties have executed this Amendment as of the date first above written.

ADVANCED MICRO DEVICES, INC.

By: /s/ Donald L. Bolin

Name: Donald L. Bolin

Title: Director Planning

VANTIS CORPORATION

By: /s/ Ronald F. Brandt

Name: Ronald F. Brandt

Title: Vice President Engineering and Manufacturing

SECOND AMENDMENT TO

AMENDED AND RESTATED WAFER FABRICATION AGREEMENT

This SECOND AMENDMENT TO AMENDED AND RESTATED WAFER FABRICATION AGREEMENT ("Amendment") is entered into as of the 18th day of February, 2000, by and between ADVANCED MICRO DEVICES, INC., a Delaware corporation having its principal place of business at One AMD Place, Sunnyvale, California 94088 ("AMD"), and VANTIS CORPORATION, a Delaware corporation having its principal place of business at 995 Stewart Drive, Sunnyvale, California 94088 ("Vantis"). Unless otherwise defined herein, capitalized terms used herein shall have the respective meanings assigned to them in the Amended and Restated Wafer Fabrication Agreement, dated as of April 21, 1999, as amended by the First Amendment to Amended and Restated Wafer Fabrication Agreement dated as of September 24, 1999, by and between AMD and Vantis (the "Wafer Fab Agreement").

RECITALS

A. AMD and Vantis entered into the Wafer Fab Agreement, whereby AMD agreed to fabricate certain semiconductor devices for Vantis.

B. AMD and Vantis desire to amend certain terms of the Wafer Fab Agreement.

AGREEMENT

Now, therefore, in consideration of the premises and for other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the parties agree as follows:

1. AMENDMENT

a. EXPECTED NET DIE PER WAFER. The Expected Net Die Per Wafer set forth on Exhibit A - Expected Net Die Per Wafer for the first and second fiscal quarters of 2000 shall be deleted in their entirety and replaced with the Net Die Per Wafer set forth in the table below.

TECHNOLOGY	DEVICE	NET DIE PER WAFER
[*]	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]

TECHNOLOGY	DEVICE	NET DIE PER WAFER
[*]	[*]	[*]

[Confidential Treatment Request]

TECHNOLOGY	DEVICE	NET DIE PER WAFER
[*]	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
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TECHNOLOGY	DEVICE	NET DIE PER WAFER
[*]	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]

TECHNOLOGY	DEVICE	NET DIE PER WAFER
E[*]	[*]	[*]
	[*]	[*]
	[*]	[*]
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	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]

[Confidential Treatment Request]

TECHNOLOGY	DEVICE	NET DIE PER WAFER
[*]	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
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	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]

b. BASE DIE PRICE TABLE. The Base Die Prices set forth on Exhibit F - Base Die Price Table for 2000 shall be deleted in their entirety and replaced with the Base Die Prices set forth in the table below.

TECHNOLOGY	DEVICE	BASE DIE PRICE
[*]	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]

TECHNOLOGY	DEVICE	BASE DIE PRICE
[*]	[*]	[*]

[Confidential Treatment Request]

TECHNOLOGY	DEVICE	BASE DIE PRICE
[*]	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
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	[*]	[*]
	[*]	[*]
	[*]	[*]

TECHNOLOGY	DEVICE	BASE DIE PRICE
[*]	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]

TECHNOLOGY	DEVICE	BASE DIE PRICE
[*]	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]

[Confidential Treatment Request]

TECHNOLOGY	DEVICE	BASE DIE PRICE
[*]	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]
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	[*]	[*]
	[*]	[*]
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	[*]	[*]
	[*]	[*]
	[*]	[*]
	[*]	[*]

c. REFERENCES WITHIN THE WAFER FAB AGREEMENT. Each reference in the Wafer Fab Agreement to "this Agreement" and the words "hereof," "herein" and "hereunder," or words of like import, shall mean and be a reference to the Wafer Fab Agreement as amended by this Amendment.

2. MISCELLANEOUS

a. WAFER FAB AGREEMENT OTHERWISE NOT AFFECTED. Except as expressly amended pursuant hereto, the Wafer Fab Agreement shall remain unchanged and in full force and effect and is hereby ratified and confirmed in all respects.

b. AMENDMENT AND WAIVERS. The provisions of this Amendment may only be amended or waived in accordance with the terms of the Wafer Fab Agreement.

c. SUCCESSORS AND ASSIGNS. The provisions of this Amendment shall be binding upon and inure to the benefit of the parties hereto and their respective successors and assigns.

d. COUNTERPARTS. This Amendment may be executed in any number of counterparts, each of which shall be an original, with the same effect as if the signatures thereto and to this Amendment were upon the same instrument.

e. SEVERABILITY. In the event that any provision of this Amendment shall be unlawful or otherwise unenforceable, such provision shall be severed, and the entire agreement shall not fail on account thereof, the balance continuing in full force and effect, and the parties shall endeavor to replace the severed provision with a similar provision that is not unlawful or otherwise unenforceable.

f. NO THIRD-PARTY BENEFICIARIES. No person not a party to this Amendment shall have any rights under this Amendment as a third-party beneficiary or otherwise other than persons or entities entitled to indemnification as expressly set forth herein.

[Confidential Treatment Request]

g. GOVERNING LAW. This Amendment shall be governed by and construed in accordance with the laws of the State of California, without reference to conflicts of law principles.

h. INTEGRATION. This Amendment sets forth the entire agreement and understanding between the parties as to its subject matter and supersedes all prior agreements, understandings and memoranda between the parties. No amendments or supplements to this Amendment shall be effective for any purpose except by a written agreement signed by the parties.

[THIS SPACE INTENTIONALLY LEFT BLANK]

IN WITNESS WHEREOF, the parties have executed this Amendment as of the date first above written.

ADVANCED MICRO DEVICES, INC.

By: /s/ Thomas E. Bumch
Name: Thomas E. Bunch
Title: Director, Strategic Planning

VANTIS CORPORATION

By: /s/ Frank Barone
Name: Frank J. Barone
Title: Chief Operating Officer

AGREED TO AND ACCEPTED:

LATTICE SEMICONDUCTOR CORPORATION

By: /s/ Randy D. Baker
Name: Randy D. Baker
Title: Vice President, Manufacturing

EXHIBIT 21.1

LATTICE SEMICONDUCTOR CORPORATION

SUBSIDIARIES OF THE REGISTRANT

	NAME	JURISDICTION OF INCORPORATION
1.	Lattice GmbH	Germany
2.	Lattice Semiconducteurs SARL	France
3.	Lattice Semiconductor AB	Sweden
4.	Lattice Semiconductor Asia Limited	Hong Kong
5.	Lattice Semiconductor KK	Japan
6.	Lattice Semiconductor (Shanghai) Co. Ltd	China
7.	Lattice UK Limited	United Kingdom
8.	Vantis Corporation	Delaware, USA
9.	Vantis International Limited	Delaware, USA
10.	Vantis SAS	France
11.	Vantis GmbH	Germany
12.	Vantis (UK) Limited	United Kingdom
13.	Vantis II (UK) Limited	United Kingdom
14.	Vantis SRL	Italy

EXHIBIT 23.1

CONSENT OF INDEPENDENT ACCOUNTANTS

We hereby consent to the incorporation by reference in the Registration Statements on Form S-8 (No. 33-33933, No. 33-35259, No. 33-38521, No. 33-76358, No. 33-51232, No. 33-69496, No. 333-15737, No. 333-40031, No. 333-69467, and No. 333-81035) and the Registration Statements on Form S-3 (No. 33-57512, No. 333-15741, No. 333-40043, No. 333-69469 and No. 333-93285) of Lattice Semiconductor Corporation and subsidiaries of our report dated January 19, 2000 relating to the consolidated financial statements, which appears in the Transition Report to Stockholders, which is incorporated in this Transition Report on Form 10-K. We also consent to the incorporation by reference of our report dated January 19, 2000 relating to the financial statement schedule, which appears in this Form 10-K.

/s/ PRICEWATERHOUSECOOPERS LLP

Portland, Oregon
March 28, 2000

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9-MOS
JAN-01-2000
APR-04-1999
JAN-01-2000
113,824
100,316
33,676
(1,583)
26,036
313,986
126,294
(66,605)
916,155
161,228
260,000
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483
482,290
916,155
269,699
269,699
108,687
340,049
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75
9,732
(74,470)
(27,989)
(46,481)
0
(1,665)
0
(48,146)
(1.01)
(1.01)