Exhibit 99.1

Safe Harbor

Forward Looking Statements

We may make projections or other forward-looking statements regarding future events during our presentation today. We caution you that such statements are predictions based on information that is currently available and that actual results may differ materially. We refer you to the documents that the company has filed with the SEC, including our 10-K, 10-Qs and 8-Ks. These documents identify important risk factors that could cause actual results to differ materially from those contained in our projections or forward-looking statements.

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Spartan is a registered trademark of Xilinx, Inc. and Cyclone is a registered trademark of Intel Corporation in the United States and/or other countries.

Solid Progress Over the Past Year

FOCUSED STRATEGY

100% Focus on FPGA

RE-ENERGIZED TEAM

New Leadership Team; Revitalized Culture

SOLUTION INNOVATION

Application Focused Innovation

PROFIT EXPANSION

2x Growth in Profit
5x Growth in Cash Flow

INCREASED INVESTMENT

Increasing Investment in New Devices and Solutions

STRONGER ROADMAP

Faster Cadence; High Fidelity Execution

Note: Net profit and cash flow expansion based on non-GAAP results from Q1 thru Q3 2019 compared to Q1 thru Q3 2018

LATTICE
SEMICONDUCTOR.

New Products Over the Next 12 Months

sensAI 2.0

New AI Capabilities

LAUNCH DATE
MAY 20, 2019

MachXO3D

Robust Platform Security
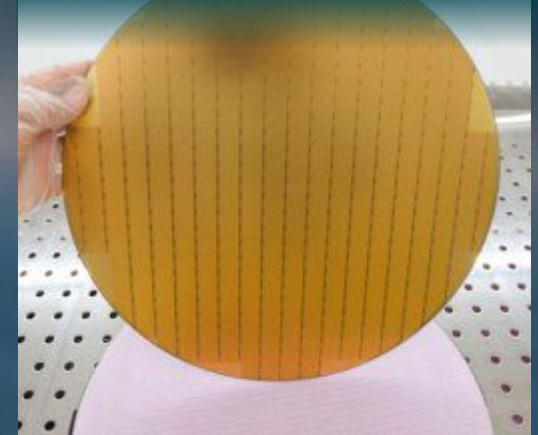
LAUNCH DATE
MAY 20, 2019

CrossLinkPlus

Enhanced Video Bridging

Sampling in ~~H2 2019~~

Q3 2019

Next Generation

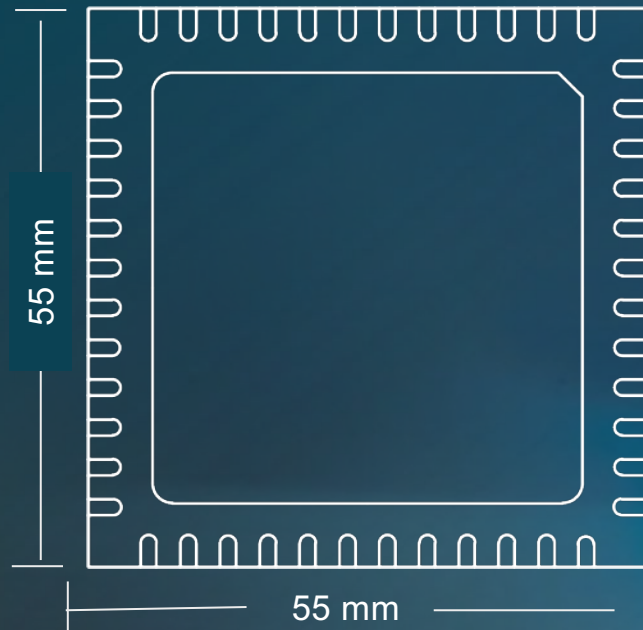Next Generation FPGA Platform

Sampling ~~early 2020~~

Today

Our Mission

The Low Power Programmable Leader

LATTICE
SEMICONDUCTOR.

Lattice's Focus: Low Power, Small Size

OTHER FPGA COMPANIES

Focused on Large, High Power Devices
for Data Center Compute

55 mm

55 mm

~200 W With Heat Sink

LATTICE
SEMICONDUCTOR®

Focused on Low Power,
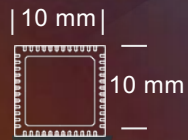Smaller Form Factors

10 mm

10 mm

~1 W
(Small)

1.40 mm

1.45 mm
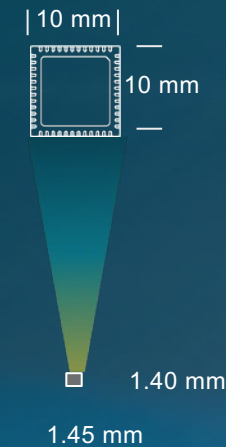
~1 mW
(Smallest)

Addressing Applications Where
Power Efficiency & Small Size are Important

Solving Problems at the Edge

| 10 mm |

10 mm

~1 W
(Small)

1.40 mm

1.45 mm

~1 mW
(Smallest)

AI & IoT

AI Inferencing at the Edge

VIDEO

Embedded Vision

SECURITY

Hardware Platform Security
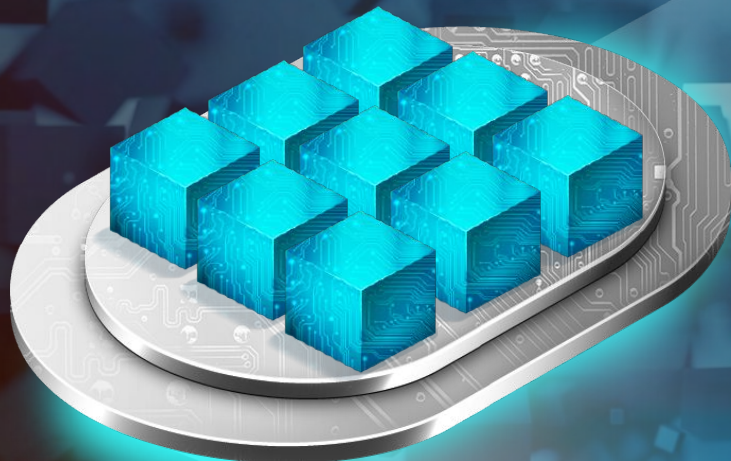
5G INFRASTRUCTURE

Control & Management

AUTOMATION

Precision Robotic Motor Control

LATTICE
SEMICONDUCTOR

Introducing Our New Low Power FPGA Platform

LATTICE NEXUS

LATTICE
SEMICONDUCTOR

Introducing Our New Low Power FPGA Platform

LATTICE INNOVATION

SOLUTIONS

ARCHITECTURE

Hardened D-PHY		Fast Programmable I/O
Industry Leading SER	Logic Cells Embedded Memory DSP Blocks	Ultra Fast Boot
Enhanced PLLs		Hardened PCIe

CIRCUIT

LATTICE NEXUS

LATTICE SEMICONDUCTOR.
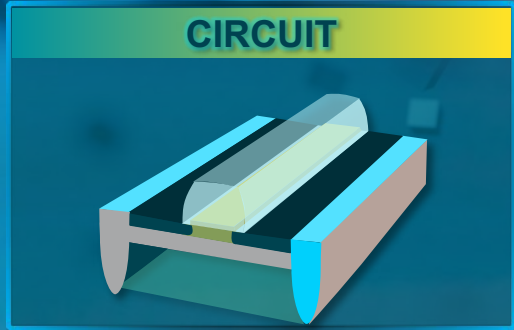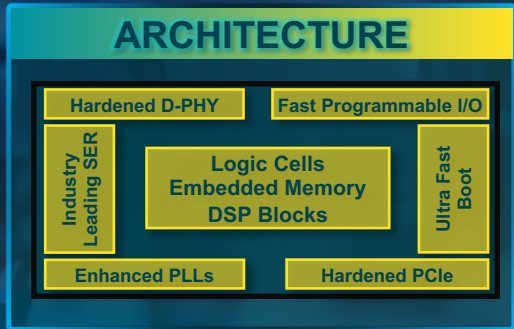
Lattice Nexus is Changing the Landscape

POWER

Operating Power Consumption

Competition | Lattice

Up to 75% Lower power
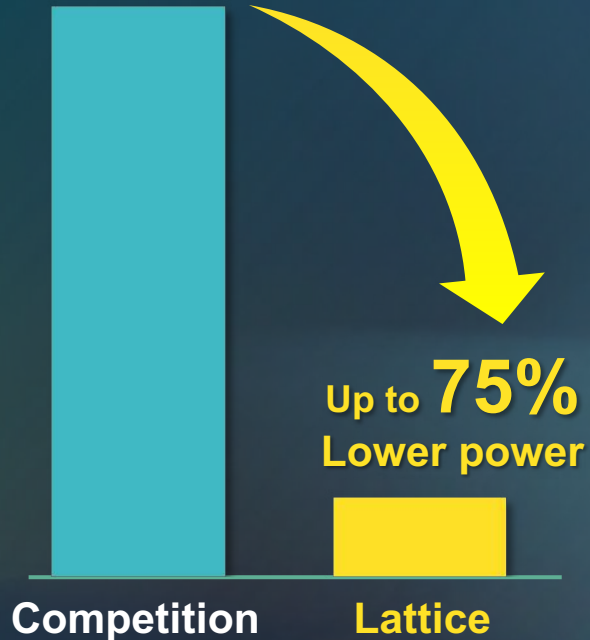
PERFORMANCE

Video Connectivity

Up to 2x Faster speed

Competition | Lattice

RELIABILITY

Soft Error Rates

Up to 100x Lower SER

Competition | Lattice

Note: comparing similar class competitive devices

LATTICE SEMICONDUCTOR
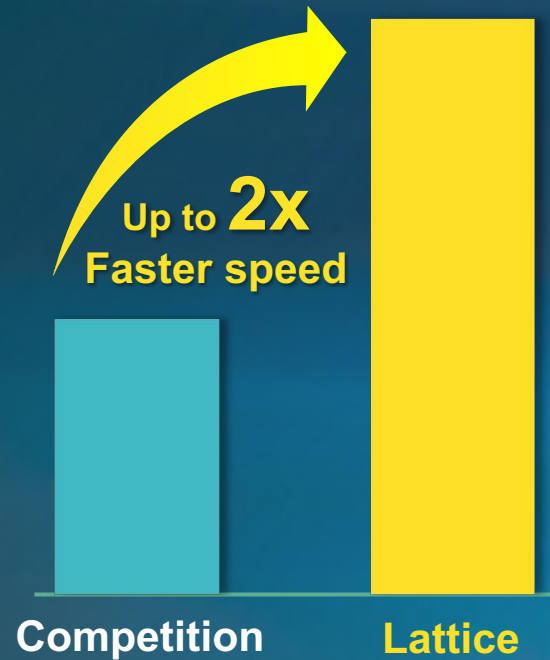
Bringing Lattice Nexus Across All our Key End Markets

COMMUNICATIONS	COMPUTE	INDUSTRIAL	AUTOMOTIVE	CONSUMER

5G Wireless	Servers	Industrial IoT	ADAS	Smart Home
Switches/Routers	Client	Factory Automation	Infotainment	Wearables

$3B Lattice Market Opportunity

LATTICE
SEMICONDUCTOR,

LATTICE NEXUS

- Low power leadership

- Edge computing ready

- Robust and reliable
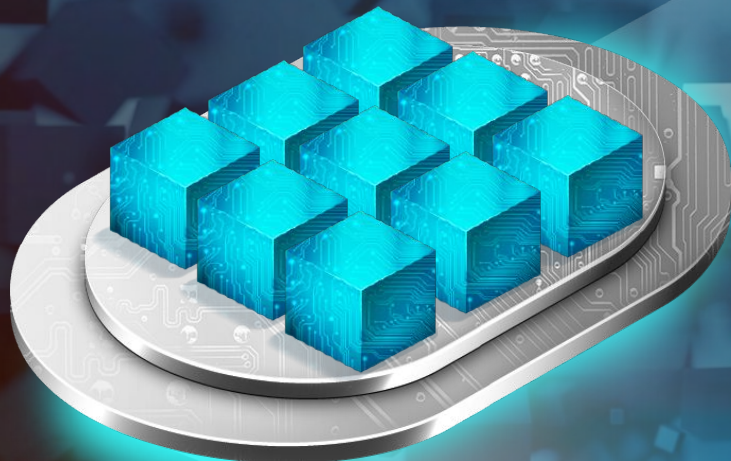
- Smallest form factor

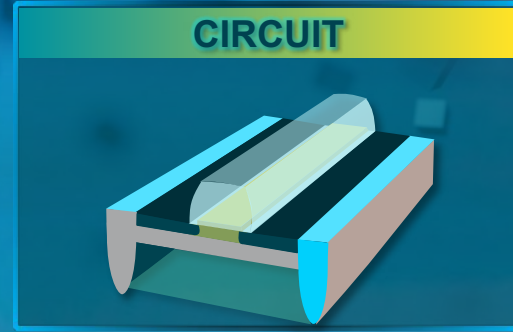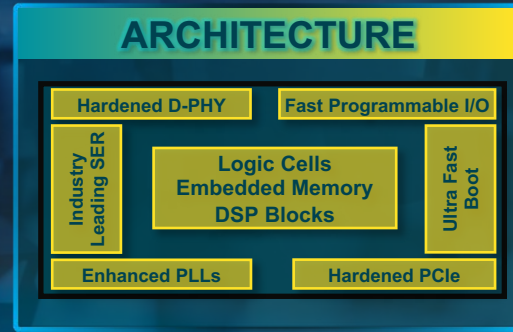- Faster innovation cadence

Steve Douglass

Corporate Vice President,
R&D

Introducing Our New Low Power FPGA Platform

LATTICE INNOVATION

SOLUTIONS

ARCHITECTURE

Hardened D-PHY		Fast Programmable I/O
Industry Leading SER	Logic Cells Embedded Memory DSP Blocks	Ultra Fast Boot
Enhanced PLLs		Hardened PCIe

CIRCUIT

LATTICE NEXUS

Circuit Innovation

SOLUTIONS

ARCHITECTURE

Hardened D-PHY	Fast Programmable I/O

Industry Leading SER	Logic Cells Embedded Memory DSP Blocks	Ultra Fast Boot

Enhanced PLLs	Hardened PCIe
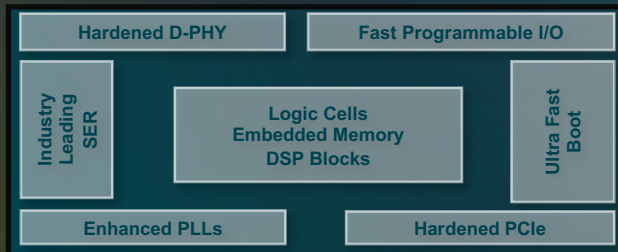
CIRCUIT

LATTICE NEXUS ON FDSOI

GATE

SOURCE   DRAIN

ULTRA-THIN BURIED OXIDE
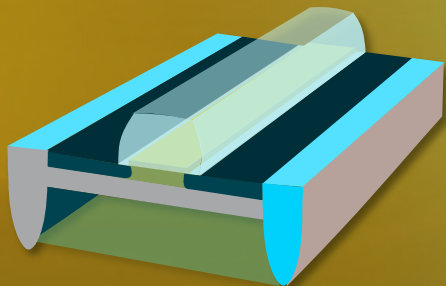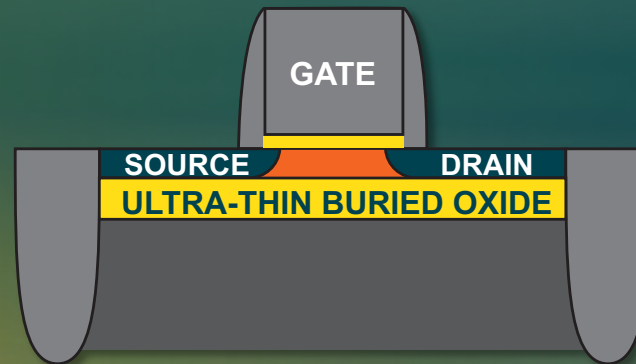
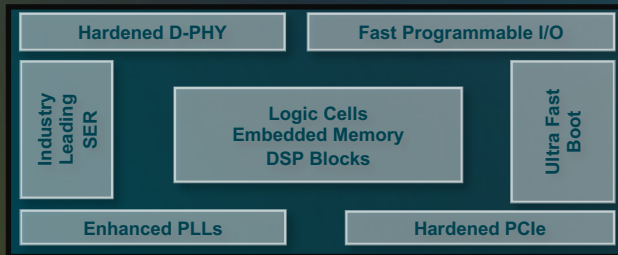## TRADITIONAL FPGA ON BULK

GATE

SOURCE   DRAIN
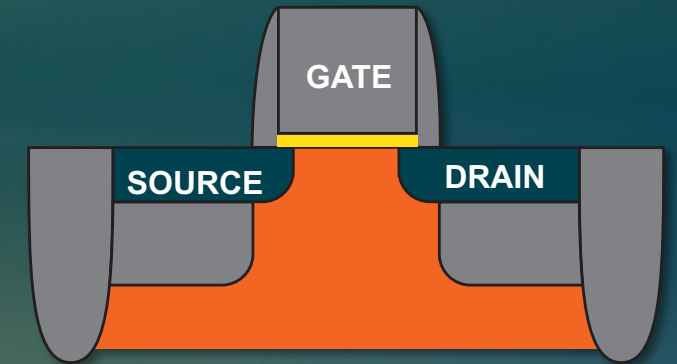
- Greatly reduces transistor leakage and susceptibility to soft errors
- FDSOI leverages bulk CMOS process and has fewer processing steps
- In high volume production today

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SEMICONDUCTOR.

Circuit Innovation

SOLUTIONS

ARCHITECTURE

- Hardened D-PHY
- Fast Programmable I/O
- Industry Leading SER
- Logic Cells Embedded Memory DSP Blocks
- Ultra Fast Boot
- Enhanced PLLs
- Hardened PCIe
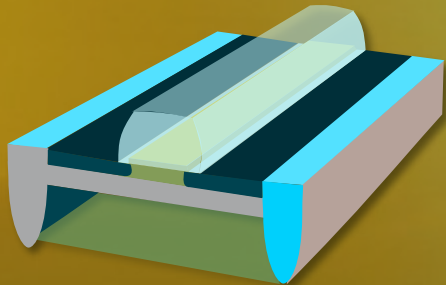
CIRCUIT

POWER

Static Power
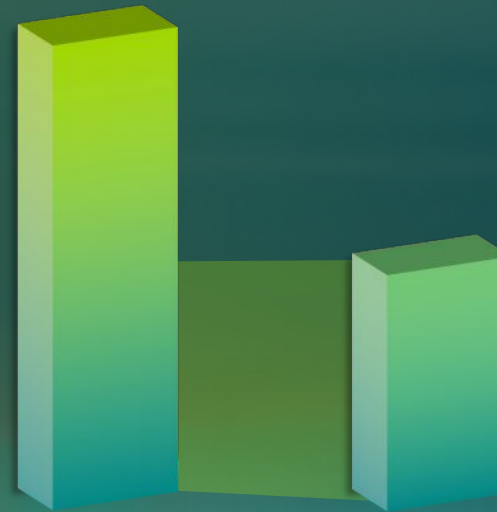
Bulk   FDSOI

Half
The Power

RELIABILITY

Soft Error Rate
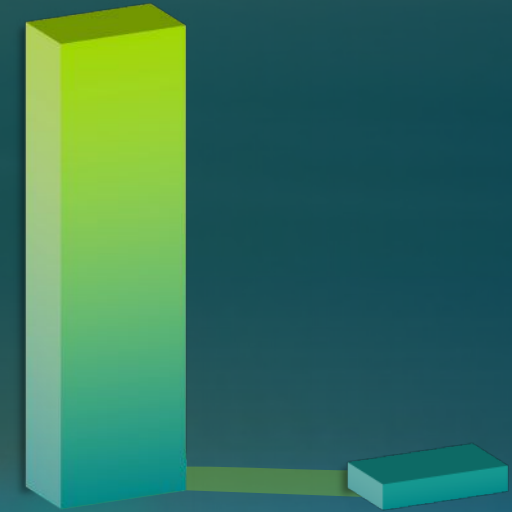
Bulk   FDSOI

100x
Lower SER

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SEMICONDUCTOR.

Circuit Innovation

SOLUTIONS

ARCHITECTURE

Hardened D-PHY	Fast Programmable I/O

Industry Leading SER	Logic Cells Embedded Memory DSP Blocks	Ultra Fast Boot

Enhanced PLLs	Hardened PCIe
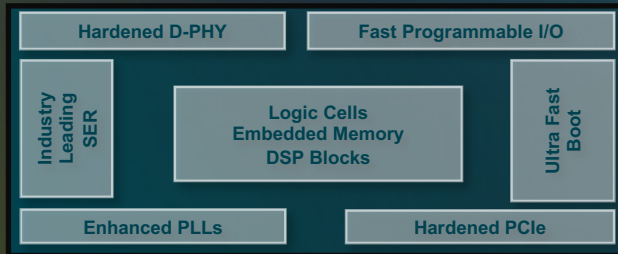
CIRCUIT

PROGRAMMABLE BODY BIAS

GATE

SOURCE — DRAIN

ULTRA-THIN BURIED OXIDE
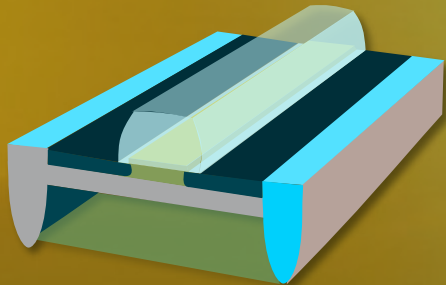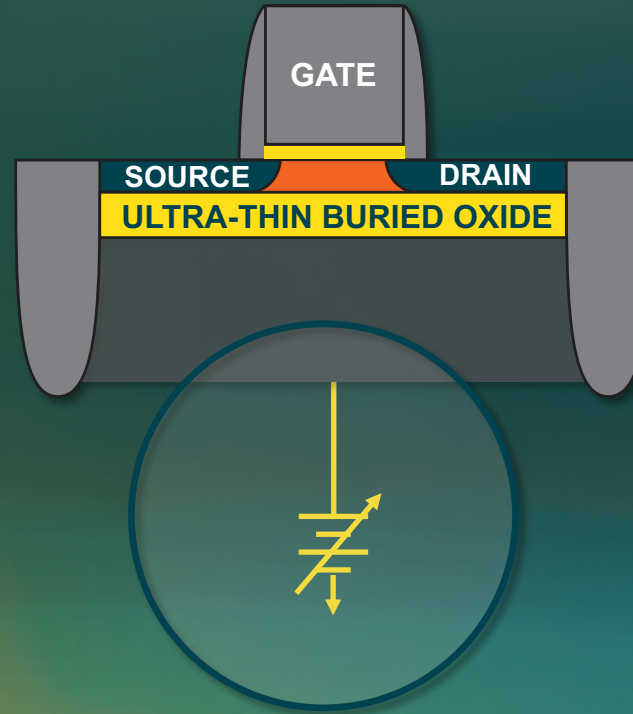
Allows customers to optimize for both:

HIGHER PERFORMANCE

LOWER POWER
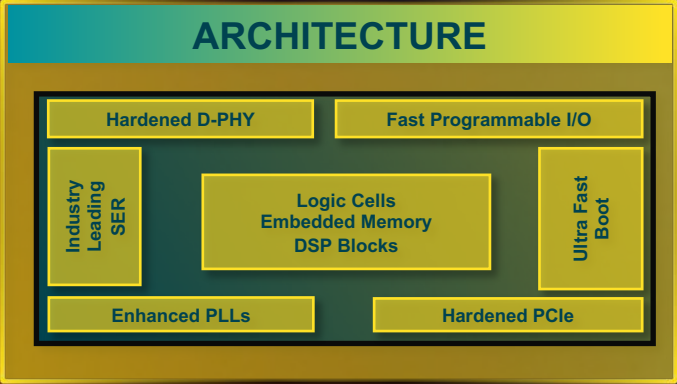
LATTICE SEMICONDUCTOR.

Architecture Innovation

SOLUTIONS

ARCHITECTURE

Hardened D-PHY | Fast Programmable I/O

Industry Leading SER

Logic Cells
Embedded Memory
DSP Blocks

Ultra Fast Boot

Enhanced PLLs | Hardened PCIe

CIRCUIT

OPTIMIZED FOR POWER EFFICIENT COMPUTING

DSP → EBR → DDR

FABRIC

LATTICE
SEMICONDUCTOR,

Architecture Innovation

SOLUTIONS

ARCHITECTURE

Hardened D-PHY	Fast Programmable I/O

Industry Leading SER

Logic Cells
Embedded Memory
DSP Blocks

Ultra Fast Boot

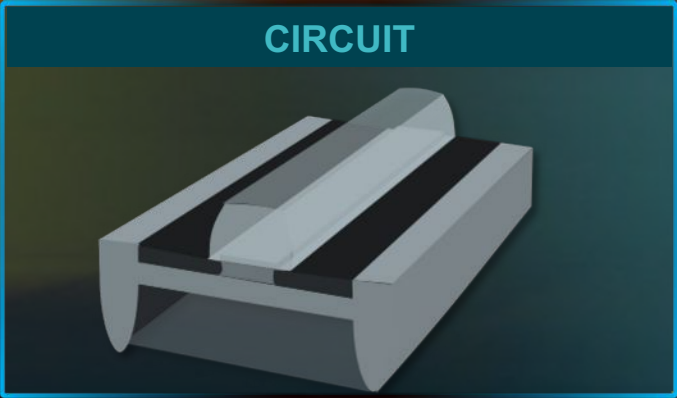|	
Enhanced PLLs	Hardened PCIe

CIRCUIT

OPTIMIZED FOR POWER EFFICIENT COMPUTING

FPGA / DSP

EBR

LARGE RAM
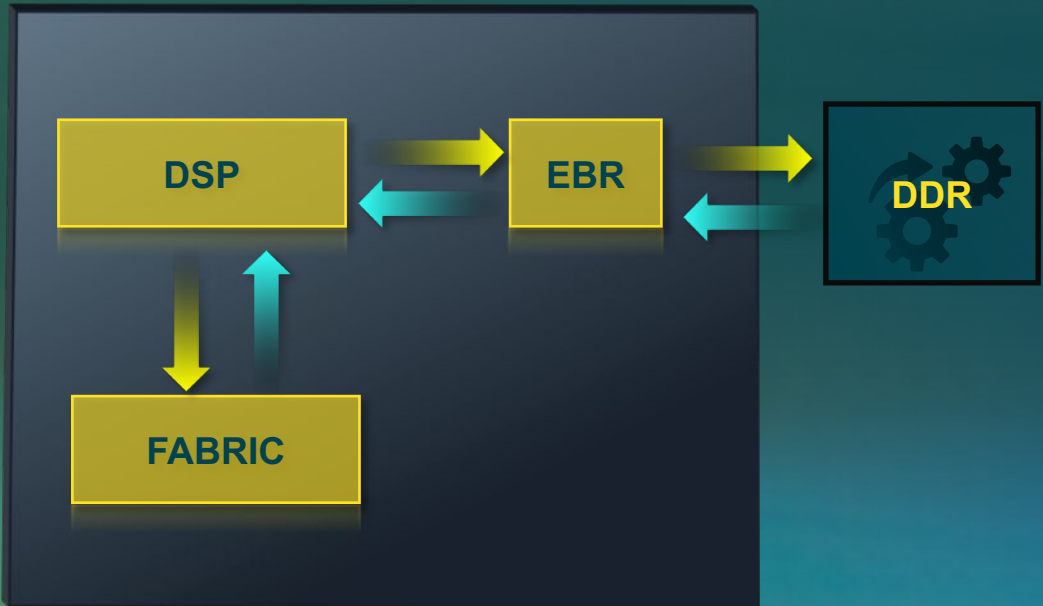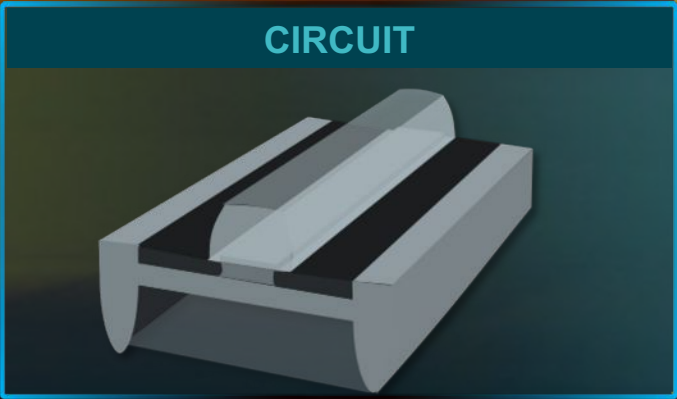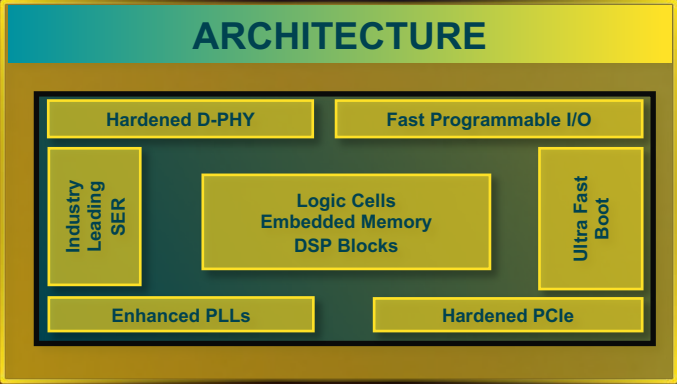
2x
Faster Performance

Half
The Power

Note: Performance and power relative to Lattice prior generation devices

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Human Presence Detection Demo

KEY APPLICATIONS

Industrial safety **Security cameras** **Client compute** **Smart doorbells**

OVERVIEW

What You Are Seeing
Human presence detection with bounding box around upper body implemented with our first Lattice Nexus based device.

Why It Matters
Human presence detection is a common AI use case in many Edge applications including security cameras, client compute, factory automation, and automotive.

LATTICE SEMICONDUCTOR.
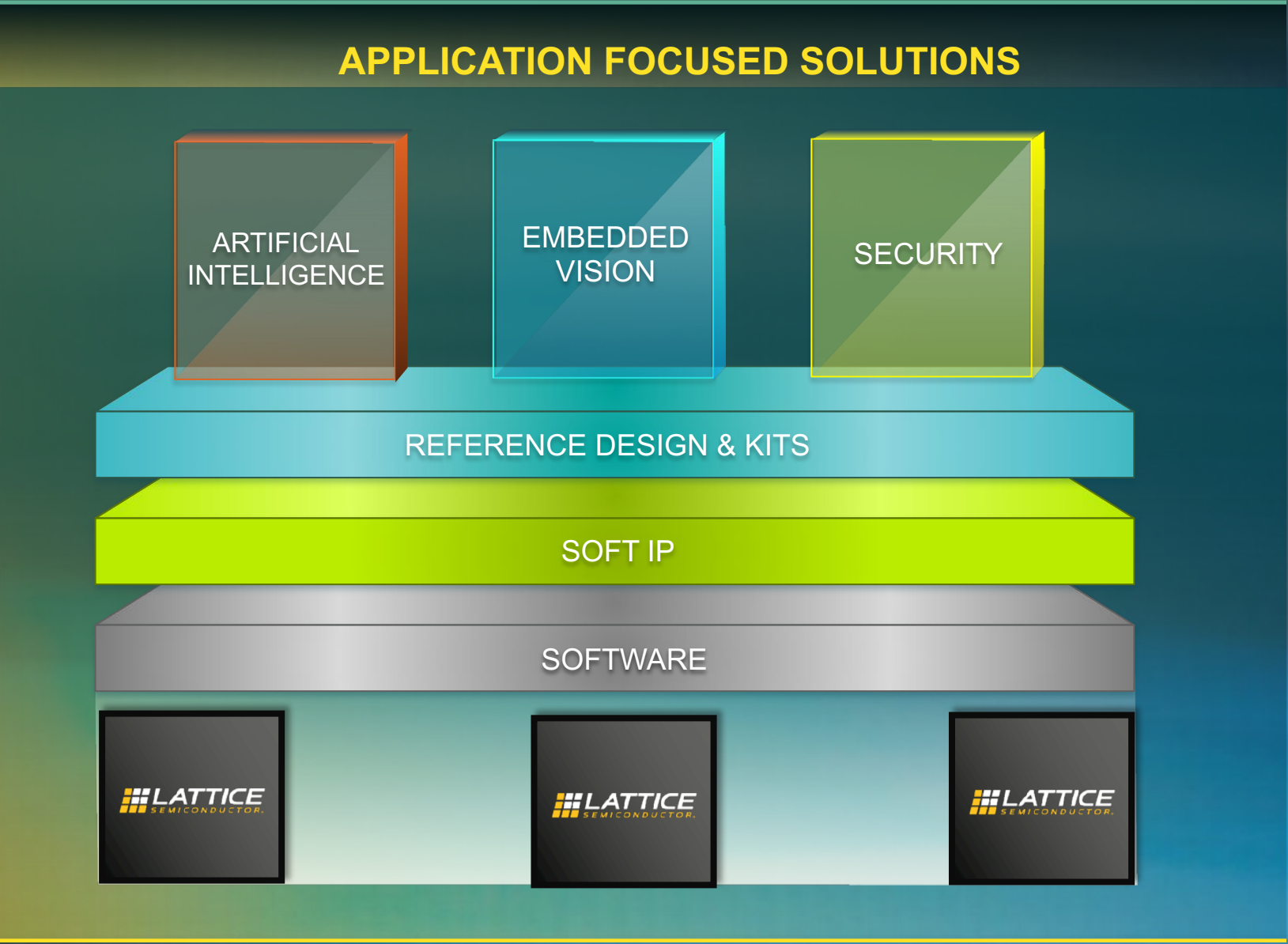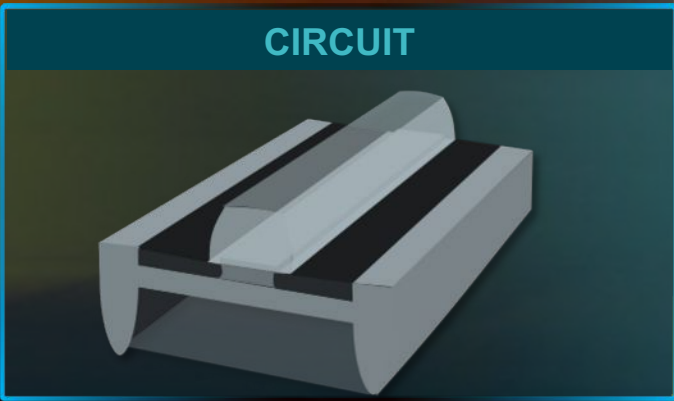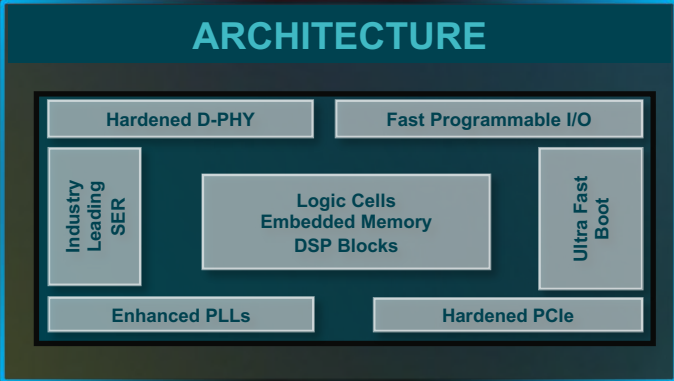
Solutions Innovation

SOLUTIONS

ARCHITECTURE

Hardened D-PHY | Fast Programmable I/O

Industry Leading SER

Logic Cells
Embedded Memory
DSP Blocks

Ultra Fast Boot
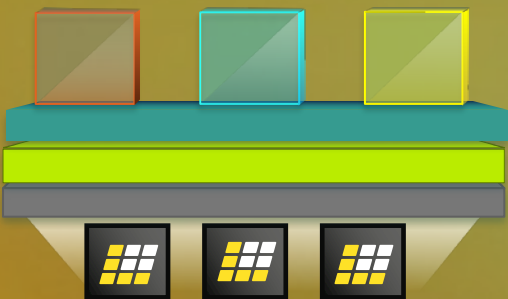
Enhanced PLLs | Hardened PCIe
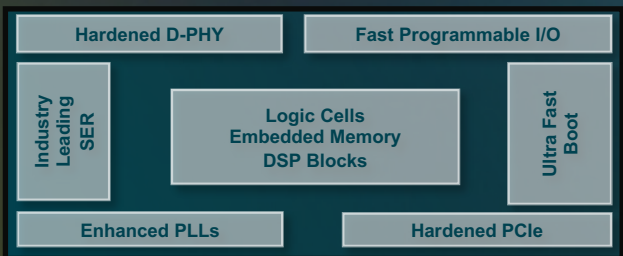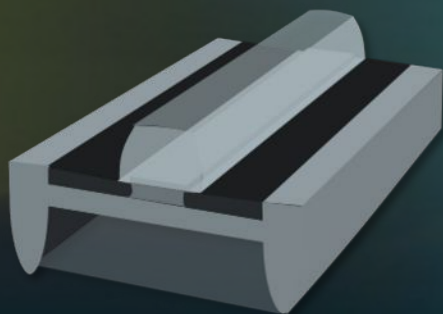
CIRCUIT

APPLICATION FOCUSED SOLUTIONS

ARTIFICIAL INTELLIGENCE

EMBEDDED VISION

SECURITY

REFERENCE DESIGN & KITS

SOFT IP

SOFTWARE

LATTICE SEMICONDUCTOR

Solutions Innovation

Camera Aggregation Demo

What You Are Seeing

MIPI CSI-2 data streams from 4 cameras are aggregated into a single data stream, bridged to parallel data and displayed in a single HDMI output.

Why It Matters

Number of sensors are increasing, and the application processors have limited MIPI inputs.

Number of screen sizes and resolutions are increasing.

Need solution that can aggregate data streams for multiple image sensors in applications such as ADAS, drones, AR/VR, robots etc.

KEY APPLICATIONS

AR / VR   **Drones**   **ADAS**   **Robotics**

LATTICE SEMICONDUCTOR.

Introducing Our New Low Power FPGA Platform

LATTICE **NEXUS**

Product 1

Product 2

Product 3

...

Product N

LATTICE
SEMICONDUCTOR.

Introducing Lattice CrossLink-NX

Introducing Lattice CrossLink-NX

Hardened MIPI D-PHY

Fast Programmable I/O

Industry Leading SER

Programmable Logic
Embedded Memory
DSP Blocks

Ultra Fast Boot

Enhanced PLLs

Hardened PCIe

LATTICE
SEMICONDUCTOR
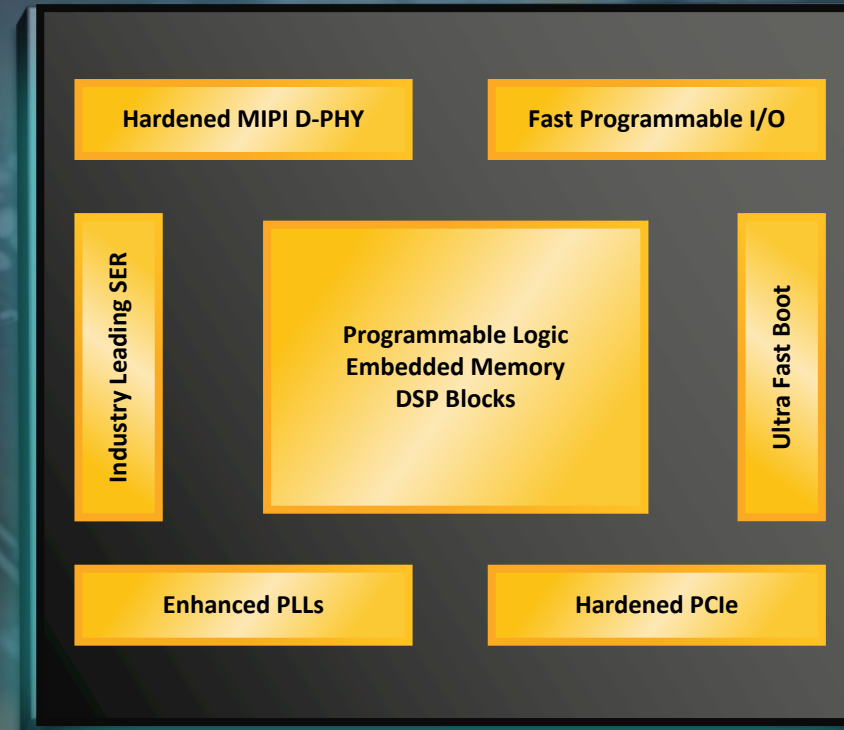
A Closer Look at CrossLink-NX

PROGRAMMABLE LOGIC CORE

- Low power mode
- High performance mode
- High embedded memory count
- Optimized DSP blocks

DEDICATED INTERFACES

- 8 D-PHY lanes @ 2.5 Gbps
- One lane PCIe @ 5 Gbps

Hardened MIPI D-PHY

Fast Programmable I/O

Industry Leading SER

Programmable Logic
Embedded Memory
DSP Blocks

Ultra Fast Boot

Enhanced PLLs

Hardened PCIe
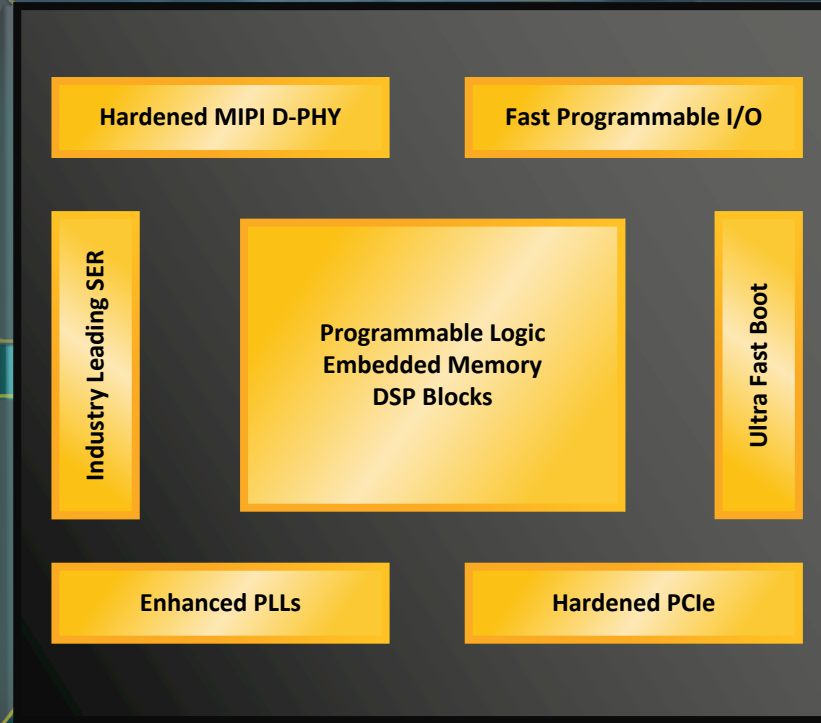
FAST PROGRAMMABLE I/O

- Up to 12 MIPI D-PHY interfaces @ 1.5 Gbps
- LVDS, subLVDS, SGMII
- DDR3 @ 1066 Mbps
- Up to 192 total I/O

INSTANT-ON

- 3 ms I/O configuration
- 14 ms device configuration

Enhanced for Customer Needs: Power Efficiency, Performance, Reliability

LATTICE SEMICONDUCTOR

Esam Elashmawi

Chief Marketing &
Strategy Officer

Customer Engagement

LOW POWER

PERFORMANCE

HIGH RELIABILITY

Solving the Power Challenge

LOW POWER

PERFORMANCE

HIGH RELIABILITY

POWER IS KEY TO SOLVE

PORTABLE & AUTONOMOUS CHALLENGES

SYSTEM & OPERATING COSTS

LOWEST POWER FPGA …

Up to **75%** lower power compared to competition

Operating Power Consumption

Xilinx Spartan 7	
Intel Cyclone 10	
Lattice CrossLink-NX	

Note: comparing similar class competitive devices

LATTICE SEMICONDUCTOR

CrossLink-NX Low Power Demo
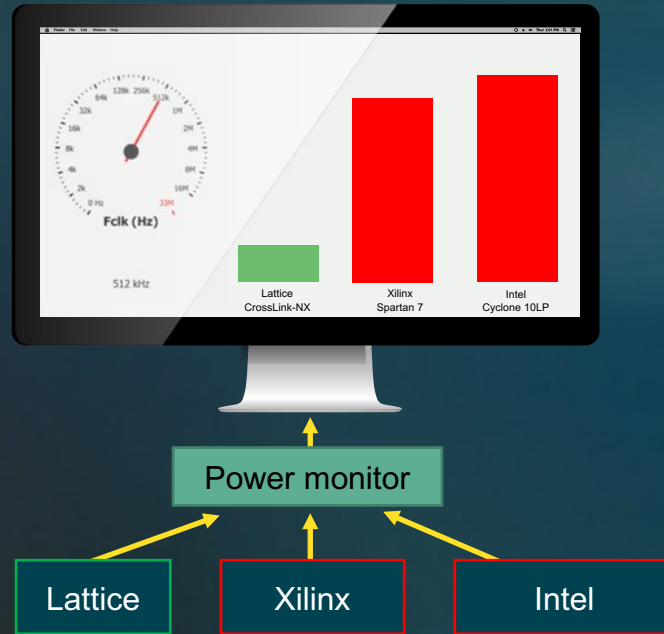
Power monitor

Lattice | Xilinx | Intel

KEY APPLICATIONS

Industrial Robots   **Drones**   **Medical**   **Factory Automation**   **Servers**   **5G**

OVERVIEW

What You Are Seeing

Power consumption for Lattice CrossLink-NX-40 running a typical design compared with Xilinx Spartan 7 (XC7S50) and Intel Cyclone 10LP (10CL025).

Why It Matters

- Simplifies thermal management
- Improves operating costs
- Extends battery life

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Solving the Performance Challenge

LOW POWER

PERFORMANCE

HIGH RELIABILITY

PERFORMANCE IS KEY TO SOLVE

USER EXPERIENCE

PERFORMANCE FOR AI

ENHANCED PERFORMANCE FEATURES

Fastest display connection

Chart: MIPI D-PHY Speed (Mbps)
- Lattice CrossLink-NX: ~2500
- Xilinx Spartan 7: ~1200
- Intel Cyclone 10LP: ~800

Optimized for power efficient computing

Chart: Memory per Logic Cell (bits)
- Lattice CrossLink-NX: ~65
- Xilinx Spartan 7: ~52
- Intel Cyclone 10LP: ~29

Note: comparing similar class competitive devices

LATTICE SEMICONDUCTOR.
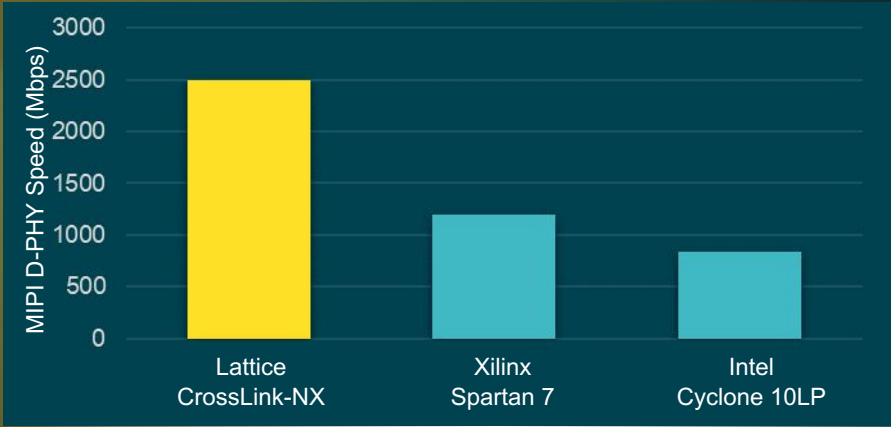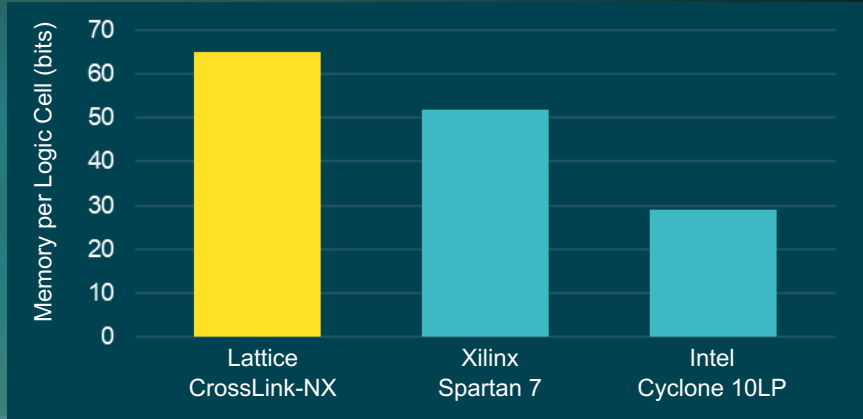
sensAI Application Example: Retail Security Camera

ALWAYS-ON HUMAN COUNTING

Lattice CrossLink-NX

- SRAM (weights / activations)
- Sensor Interface
- Neural Network Accelerators

Data → Sensors

Results → MCU

PERFORMANCE

10 fps — CrossLink- NX-40K

10x FASTER

1 fps — MCU

POWER

600 mW — MCU

3x LOWER

200 mW — CrossLink- NX-40K
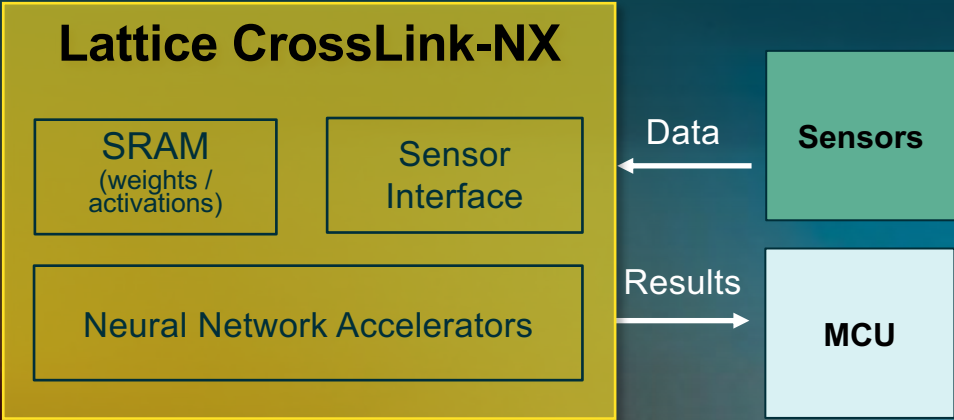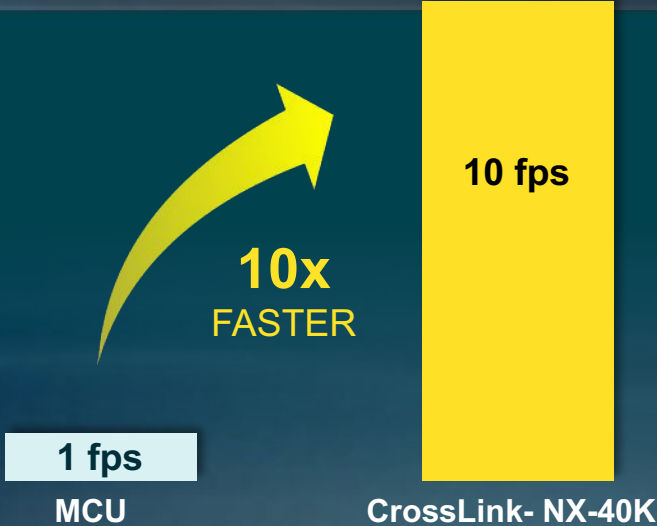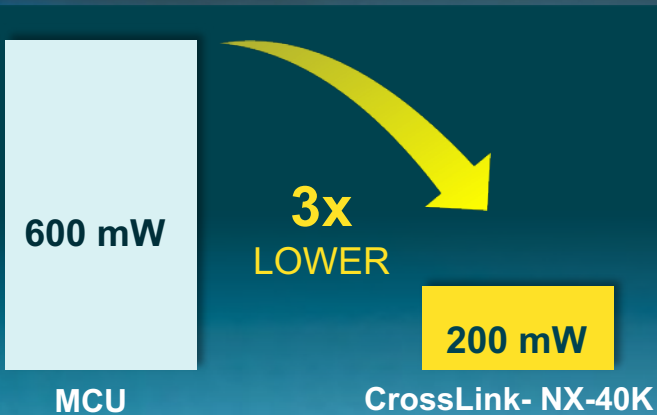
Instant-on

LOW POWER

PERFORMANCE

HIGH RELIABILITY

PERFORMANCE IS KEY TO SOLVE

INCREASED DEMAND FOR INSTANT-ON APPLICATIONS

UP TO 50X FASTER

I/O wake up time

Intel
Cyclone 10LP

Xilinx
Spartan 7

Lattice
CrossLink-NX

Instant-on Range

Note: comparing similar class competitive devices

LATTICE
SEMICONDUCTOR

CrossLink-NX Instant-on Demo

Lattice → VCC RAMP / I/O DEFINED → Monitor → `003`

Xilinx → VCC RAMP / I/O DEFINED → Monitor → `150`

Intel → VCC RAMP / I/O DEFINED → Monitor → `168`

KEY APPLICATIONS

Motor Control

Human Machine Interfaces

ADAS
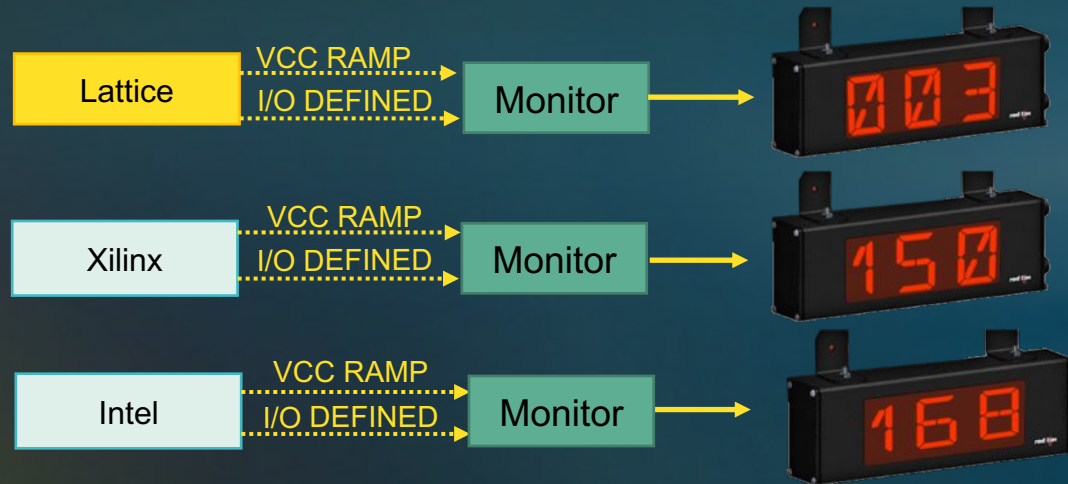
OVERVIEW

What You Are Seeing

Time for device to self configure I/O to a user defined state for Lattice CrossLink-NX-40 compared with Xilinx Spartan 7 (XCS7-50) and Intel Cyclone 10LP (10LP025).

Why It Matters

"Instant-on" I/O configuration is important for applications such as LED drivers, motor control and board housekeeping.

Reduces complexity, cost, and power dissipation of customer systems.

Note: based on competition's evaluation boards running at similar frequencies

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Solving the Reliability Challenge

LOW POWER

PERFORMANCE

HIGH RELIABILITY

RELIABILITY IS KEY TO SOLVE

CRITICAL SAFETY & RUGGEDIZED

SYSTEM UP TIME

MOST RELIABLE FPGA FOR RUGGEDIZED APPS

Temperature Ranges

- 40˚C   125˚C

Suitable for:

OUTDOOR | AUTOMOTIVE | INDUSTRIAL | AVIONICS

Soft Error Rates (FIT)

Xilinx*
Spartan 7

Lattice
CrossLink-NX

Up to **100x**
Lower SER
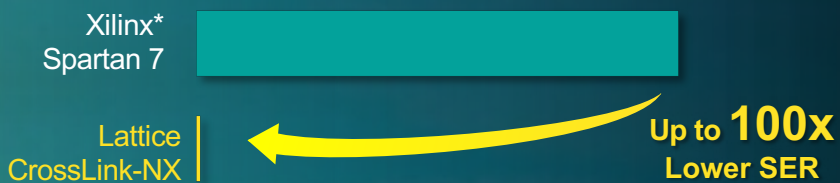
FIT (Failure In Time) (1B device hours)
* Based on Xilinx published data

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SEMICONDUCTOR

Small Size Matters

	CrossLink-NX LIFCL-40-7MG121C	Xilinx Spartan 7 XC7S50-1GCSGA324C	Intel Cyclone 10LP 10CL040YU484C6
Logic Cells	40K	50K	40K

Engaged with > 65 customers

Early Access Program with 30+ customers

Solutions available today

Jim Anderson

President, Chief Executive Officer

The Lowest Power FPGA Platform
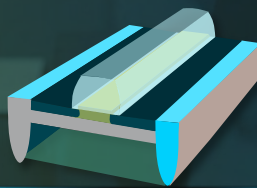
SOLUTIONS

ARCHITECTURE

- Hardened D-PHY
- Fast Programmable I/O
- Industry Leading SER
- Logic Cells Embedded Memory DSP Blocks
- Ultra Fast Boot
- Enhanced PLLs
- Hardened PCIe

CIRCUIT

LATTICE NEXUS

LOW POWER

PERFORMANCE

HIGH RELIABILITY

CrossLink-NX

LATTICE SEMICONDUCTOR.
CrossLink-NX

Product 2

Product 3

Product N

LATTICE SEMICONDUCTOR.

Faster Cadence of New Devices and Solutions

	H1 2019	H2 2019	H1 2020	H2 2020
Solutions	Lattice sensAI 2.0	Lattice Radiant 2.0	Embedded Vision Stack	Security Stack
Devices	MachXO3D	CrossLinkPlus	CrossLink-NX	Nexus Product #2	Nexus Product #3
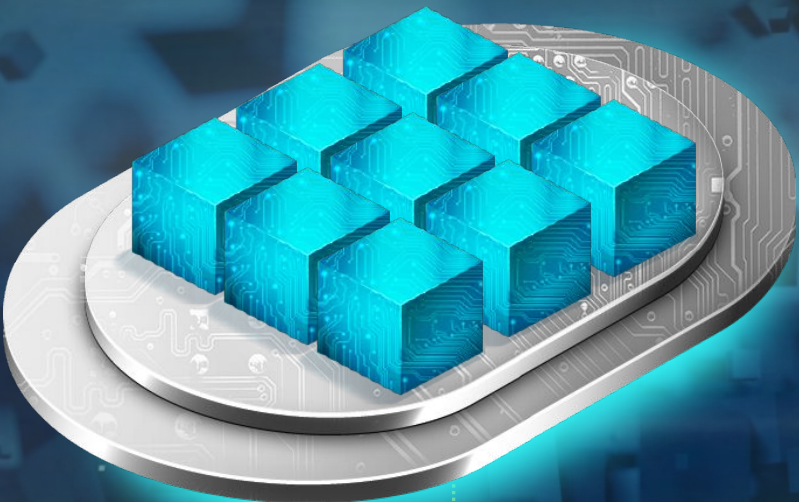
LATTICE **NEXUS**

CrossLink-**NX**

DEMO SIGNAGE

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SEMICONDUCTOR.

Human Presence Detection & Counting

BLOCK DIAGRAM

CrossLink-NX

| MIPI CSI-2 Sensor |

- Byte to Pixel
- Raw2RGB
- CSI-2/DSI D-PHY Rx
- SRAM (Weights/Activations)
- Neural Network Accelerators

SII1136

HDMI Output

KEY APPLICATIONS

Security cameras

Client compute

Smart doorbells

Smart appliances
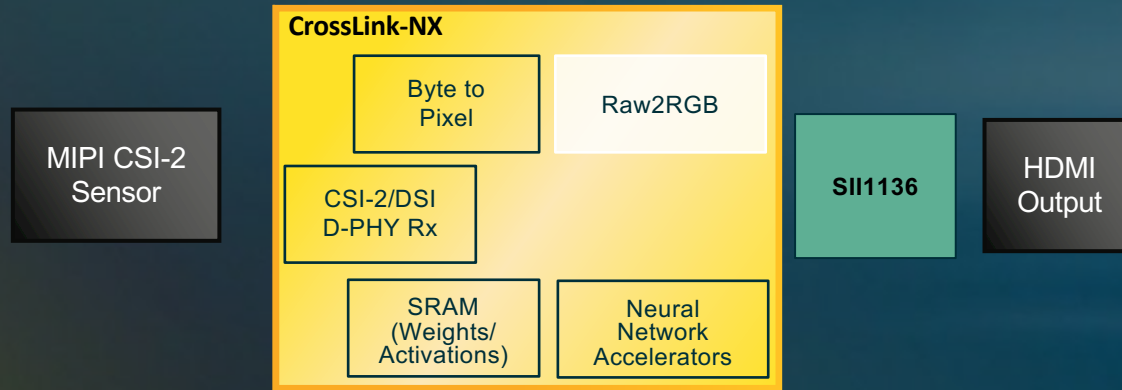
OVERVIEW

What You Are Seeing
Human presence detection and counting with bounding box around upper body implemented with Lattice CrossLink-NX

Why It Matters
Human presence detection is a common AI use case in many Edge applications including security cameras, client compute, factory automation, and automotive.

The Lattice Advantage
Lattice CrossLink-NX supports detection at 2x frame rate and 0.5x the power of prior generation

Lattice CrossLink-NX supports detection at 10x higher frame rate and 0.3x power compared to MCUs

Integrated D-PHY to reduce power and BOM cost

FPGA flexibility for additional pre/post processing compared to fixed function ASICs

LATTICE SEMICONDUCTOR

Camera Aggregation

BLOCK DIAGRAM

CrossLink-NX

MIPI CSI-2 Sensor	CSI-2/DSI D-PHY Rx	Byte to Pixel	Raw2RGB			
MIPI CSI-2 Sensor	CSI-2/DSI D-PHY Rx	Byte to Pixel	Raw2RGB	4:1 Aggregation	SII1136	HDMI Output
MIPI CSI-2 Sensor	CSI-2/DSI D-PHY Rx	Byte to Pixel	Raw2RGB			
MIPI CSI-2 Sensor	CSI-2/DSI D-PHY Rx	Byte to Pixel	Raw2RGB			
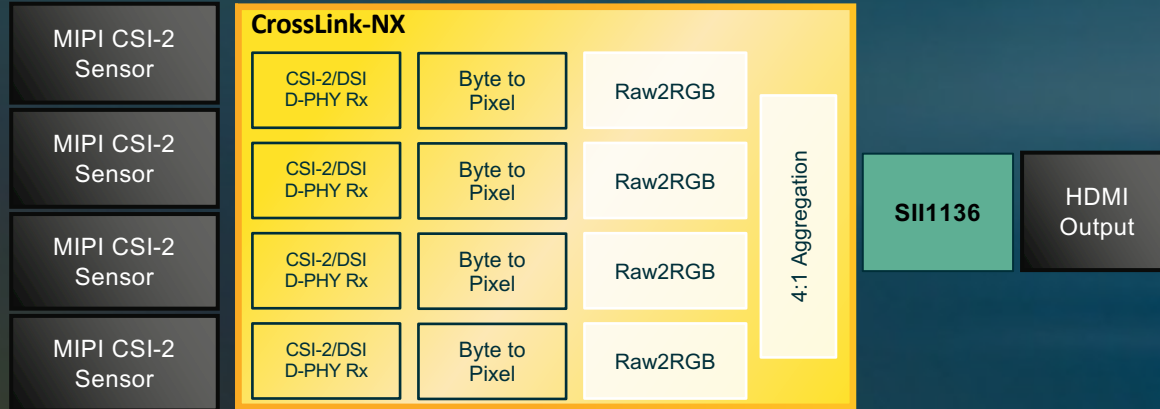
KEY APPLICATIONS

AR / VR **Drones** **ADAS** **Robotics**

OVERVIEW

What You Are Seeing

4 cameras, each providing a separate MIPI CSI-2 data stream aggregated into a single data stream, bridged to parallel data and displayed in a single HDMI output.

Why It Matters

Application processors with limited MIPI D-PHY inputs cannot interface to multiple image sensors in applications such as ADAS, drones, AR/VR, robots etc.

The Lattice Advantage
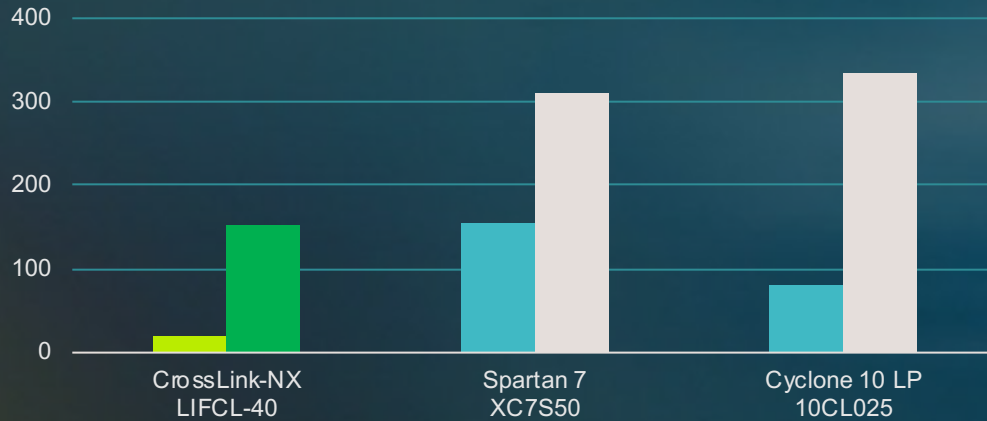
Only FPGA with up to 8 hard D-PHY lanes @ 2.5 Gbps

Scalable to support up to 14 MIPI D-PHY interfaces

Low power consumption ~300 mW

Up to 40K LUTs for customization and additional image processing

LATTICE SEMICONDUCTOR

CrossLink-NX Delivering Up to 75% Lower Power

OPERATING POWER (mW) @ 2 MHz and 200 MHz

Bar chart with y-axis from 0 to 400:
- CrossLink-NX LIFCL-40
- Spartan 7 XC7S50
- Cyclone 10 LP 10CL025

KEY APPLICATIONS

Industrial Robots | Drones | Medical | Factory Automation | Servers | 5G

OVERVIEW

What You Are Seeing
Power consumption for Lattice CrossLink-NX-40 running a typical design compared with Xilinx Spartan 7 (XC7S50) and Intel Cyclone 10LP (10CL025) running at a variety of frequencies

Why It Matters
Low power consumption simplifies thermal management, improves operating costs and where applicable extends battery life

The Lattice Advantage
Up to 75% lower power than Xilinx Spartan 7 and Intel Cyclone 10LP

Programmable back bias for per device performance / static power optimization

28 nm FD-SOI technology provides best in class dynamic power

HP and LP user modes

LATTICE SEMICONDUCTOR

CrossLink-NX Enabling Up to 50x Faster I/O Wake Up Time

I/O Self Configuration Time (mS)

200

100

3mS

0

CrossLink-NX
LIFCL-40

Spartan 7
XC7S50

Cyclone 10 LP
10CL025

KEY APPLICATIONS

Motor Control

Human Machine Interfaces

ADAS
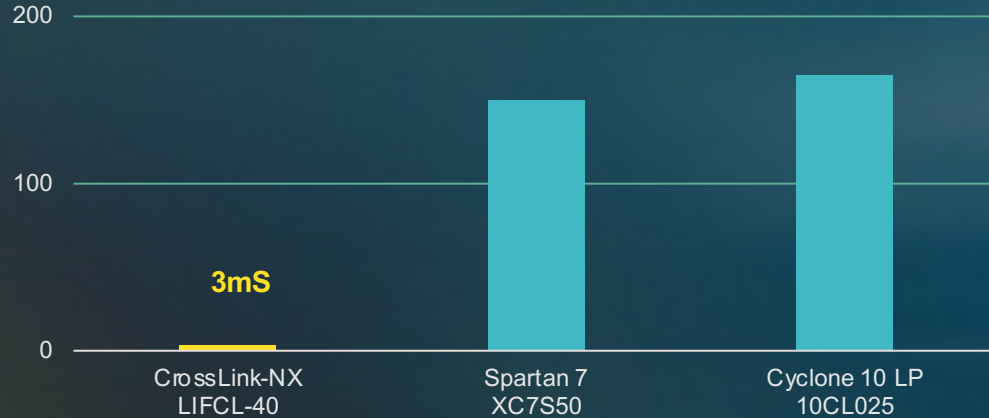
OVERVIEW

What You Are Seeing
The I/O self configuration time of the Lattice CrossLink-NX-40 running on the Lattice development board compared with Xilinx Spartan 7 (XCS7-50) and Intel Cyclone 10LP (10LP025) configured for the fastest possible configuration times on their associated development boards.

Why It Matters
"Instant-on" I/O configuration is important for applications such as LED drivers, motor control and board housekeeping.

Reduces complexity, cost, and power dissipation of customer systems

The Lattice Advantage
Smart monitor of SPI configuration memory avoids delay timers

150 MHz Quad SPI configuration interface for high speed configuration data transfer

Early I/O configuration ensures outputs stable as soon as possible

LATTICE SEMICONDUCTOR