SECURITIES AND EXCHANGE COMMISSION
WASHINGTON, D.C 20549
FORM 10-K

COMMISSION FILE NUMBER: 0-18032

/ X / Annual report pursuant to Section 13 or 15(d) of the Securities Exchange Act of 1934 for the fiscal year ended March 29, 1997 or

/ / Transition report pursuant to Section 13 or 15(d) of the Securities Exchange Act of 1934 For the transition period from to

LATTICE SEMICONDUCTOR CORPORATION

(Exact name of Registrant as specified in its Charter)

DELAWARE	93-0835214
(State of Incorporation)	(I.R.S Employer Identification No.)
5555 NE MOORE COURT, HILLSBORO, OREGON	97124-6421
(Address of principal executive offices)	(Zip Code)

Registrant's telephone number, including area code: (503) 681-0118

SECURITIES REGISTERED PURSUANT TO SECTION 12(b) OF THE ACT: NONE
SECURITIES REGISTERED PURSUANT TO SECTION 12(g) OF THE ACT:

Title of Class	Name of Exchange
Common Stock, $.01 par value	NASDAQ
Preferred Share Purchase Rights	None

Indicate by check mark whether the Registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the Registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days.

Yes X No
----- -----

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of the Registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K.

Yes No X
----- -----

As of June 12, 1997, the aggregate market value of the shares of voting stock of the Registrant held by non-affiliates was approximately $785 million. Shares of Common Stock held by each officer and director and by each person who owns 5% or more of the outstanding Common Stock have been excluded in that such persons may be deemed affiliates. This determination of affiliate status is not necessarily a conclusive determination for other purposes.

As of June 12, 1997, 23,066,825 shares of the Registrant's common stock were outstanding.

DOCUMENTS INCORPORATED BY REFERENCE

1. Portions of the Annual Report to Stockholders for the fiscal year ended March 29, 1997 are incorporated by reference in Part II hereof.

2. Portions of the definitive proxy statement of the Registrant to be filed pursuant to Regulation 14A for the 1997 Annual Meeting of Stockholders to be held on August 11, 1997 are incorporated by reference in Part III hereof.

LATTICE SEMICONDUCTOR CORPORATION
FORM 10-K
ANNUAL REPORT
TABLE OF CONTENTS

BUSINESS

This Report contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933, as amended, and Section 21E of the Securities Exchange Act of 1934, as amended. Actual results could differ materially from those projected in the forward-looking statements as a result of the factors set forth in "Factors Affecting Future Results" and elsewhere in this Report.

GENERAL

Lattice Semiconductor Corporation (the "Company") designs, develops and markets high performance programmable logic devices ("PLDs") and related development system software. The Company is the inventor and world's leading supplier of in-system programmable ("ISP-TM-") PLDs. PLDs are standard semiconductor components that can be configured by the end customer as specific logic functions, enabling shorter design cycle times and reduced development costs. Lattice was founded in 1983 and is based in Hillsboro, Oregon.

PLD MARKET BACKGROUND

Three principal types of digital integrated circuits are used in most electronic systems: microprocessors, memory and logic. Microprocessors are used for control and computing tasks, memory is used to store programming instructions and data, and logic is employed to manage the interchange and manipulation of digital signals within a system. Logic contains interconnected groupings of simple logical "AND" and logical "OR" functions, commonly described as "gates". Typically, complex combinations of individual gates are required to implement the specialized logic functions required for systems applications. While system designers use a relatively small number of standard architectures to meet their microprocessor and memory needs, they require a wide variety of logic circuits in order to achieve end product differentiation.

Logic circuits are found in a wide range of today's electronic systems including communications equipment, computers, peripherals, instrumentation, industrial controls and military systems. According to Dataquest Incorporated, a semiconductor market research firm, logic accounted for approximately 31% of the estimated $103 billion worldwide digital integrated circuit market in 1996. The logic market encompasses, among other segments, standard logic, custom-designed application specific integrated circuits ("ASICs", which include conventional gate-arrays, standard cells and full custom logic circuits), and PLDs. Logic is often classified by the number of gates per chip, with PLDs offering up to 50,000 gates, and conventional gate arrays and custom logic circuits reaching up to several hundred thousand gates.

Manufacturers of electronic systems are increasingly challenged to bring differentiated products to market quickly. These competitive pressures often preclude the use of custom-designed ASICs, which generally entail significant design risks and time delay. Standard logic products, an alternative to custom-designed ASICs, limit a manufacturer's flexibility to adequately customize an end system. Programmable logic addresses this inherent dilemma. PLDs are standard products, purchased by systems manufacturers in a "blank" state, that can be

custom configured into a virtually unlimited number of specific logic functions by programming the device with electrical signals. PLDs give system designers the ability to quickly create their own custom logic functions to provide product differentiation without sacraficing rapid time to market. Certain PLD products, including the Company's, are reprogrammable, meaning that the logic configuration can be modified, if needed, after the initial programming. A recent development pioneered by the Company, in-system programmable PLDs, extends the flexibility of standard reprogrammable PLDs by allowing the system designer to configure and reconfigure the logic functions of the PLD with standard 5-volt or 3.3-volt power supplies without removing the PLD from the system board.

Several common types of PLDs currently coexist in the marketplace, each offering customers a particular set of benefits. These include low-density PLDs (less than 1,000 gates) and high-density PLDs (greater than 1,000 gates). High-density PLDs include both complex PLDs ("CPLDs," up to 25,000 gates) and field programmable gate arrays ("FPGAs," up to 50,000 gates).

Low-density devices are typically based on industry standard architectures and include the GAL-Registered Trademark- ("Generic Array Logic") product family developed by the Company. These architectures are familiar to most system designers and are supported by standard widely available development tools. Offering the highest absolute performance and lowest cost per device, these products are the most effective PLD solution to support simple logic functions.

High-density devices are typically based on proprietary architectures and require support from sophisticated computer aided engineering ("CAE") development tools. Due to higher levels of logic integration, absolute performance typically lags that of state-of-the-art low-density PLDs by one or more technology generations. However, in situations requiring complex logic functions, high-density PLDs can provide important advantages over a large cluster of low-density devices. These advantages include system performance enhancement and power and cost savings.

CPLDs and FPGAs are the two primary types of high-density PLD architectures. Each architecture is generally optimal for different types of logic functions, although many logic functions can be implemented with either architecture. CPLDs are characterized by a regular building block structure of wide-input logic cells, termed macrocells, and use of a centralized logic interconnect scheme. CPLDs are optimal for control logic applications, such as state machines, bus arbitration, encoders, decoders and sequencers. FPGAs are characterized by a narrow-input logic cell and use a distributed interconnect scheme. FPGAs are optimal for register intensive and data path logic applications such as interface logic and arithmetic functions. The Company believes that a substantial portion of high-density PLD customers utilize both CPLD and FPGA architectures within a single system design, partitioning logic functions across multiple devices to optimize overall system performance and cost.

TECHNOLOGY

The Company believes that electrically erasable CMOS ("E(2)CMOS-Registered Trademark-") is the preferred process technology for both high-density CPLDs and low-density PLDs due to its inherent performance, reprogrammability and testability benefits. E(2)CMOS, through its fundamental ability to be programmed and erased electronically, serves as the foundation for the Company's ISP products.

IN-SYSTEM PROGRAMMABLE (ISP) PRODUCTS AND TECHNOLOGY

The Company has pioneered the development of ISP products, based on a proprietary technology, which affords it a competitive advantage in the high-density CPLD market. In contrast to standard PLDs, ISP devices can be configured and reconfigured by the system designer without being removed from the printed circuit board. Standard E(2)CMOS programmable logic devices require 12-volt electrical signals and therefore must be removed from the printed circuit board and programmed using stand alone, specialized hardware, while ISP devices can be programmed with standard 5-volt or 3.3-volt electrical signals. ISP devices offer enhanced flexibility versus standard PLDs, providing a number of important benefits to a system manufacturer across the full spectrum of an electronic system product cycle. ISP devices can allow customers to reduce design cycle times, accelerate time to market, reduce prototyping costs, reduce manufacturing costs and lower inventory requirements. ISP devices can also provide customers the opportunity to perform simplified and cost-effective field reconfiguration through a data file transferred by computer disk or serial data signal. All of the Company's high-density CPLDs are available with ISP. The Company also offers its most popular low-density architecture, the GAL22V10, with ISP.

E(2)CMOS PROCESS TECHNOLOGY

The Company's current high- and low-density PLD offerings are based on the Company's proprietary E(2)CMOS manufacturing process technology, termed UltraMOS-Registered Trademark-. The Company's current production processes, UltraMOS IV, UltraMOS V and UltraMOS VI are sub-micron CMOS technologies.

In comparison to bipolar technology, at one time the dominant technology for low-density PLDs, E(2)CMOS technology consumes less power and generates less heat while operating at comparable speed. Additionally, in contrast to one-time-programmable bipolar PLDs, E(2)CMOS PLDs are fully erasable and reprogrammable, providing greater end customer design flexibility and allowing the PLD manufacturer to fully test all programmable elements in a device prior to shipment. An alternative CMOS technology, Erasable Programmable Read Only Memory ("EPROM"), provides the same low power consumption benefits as E(2)CMOS, but requires ultraviolet light exposure for erasure, necessitating expensive quartz windowed packages and limiting testability. Antifuse and Static Random Access Memory ("SRAM") technologies, used primarily in the manufacture of high-density FPGAs, offer certain advantages for very dense logic devices, but also have significant drawbacks when compared with E(2)CMOS. Antifuse technology is non-erasable, non-reprogrammable and subject to lengthy initial programming times that can hinder usage in volume production applications. SRAM technology is volatile (erases when electrical power is removed), and as such programmable SRAM FPGAs require additional non-volatile memory, typically on a separate device, to store programming code. This adds cost and printed circuit board area to a design, and results in the devices not being completely functional at initial system power-up.

PRODUCTS

HIGH-DENSITY CPLDS

SILICON. The Company first entered the high-density market in fiscal 1993 and currently offers four distinct families of ispLSI-Registered Trademark-products, each consisting of multiple devices. All devices are offered with ISP. The Company is currently shipping over 125 speed, package and temperature range combinations of high-density CPLDs.

ISPLSI 1000/E: The Company's original high-density family utilizes an innovative, proprietary architecture incorporating familiar GAL-like logic building blocks. This family offers performance of up to 125 MHz, with propagation delays as low as 7.5 nanoseconds, densities of 2,000 to 8,000 gates, and is available in surface mount packages ranging from 44- to 128-pins.

ISPLSI 2000/V: The ispLSI 2000 family utilizes an architecture designed for input/output ("I/O") intensive applications and offers industry leading CPLD performance. This family provides performance of up to 180 MHz, with propagation delays as low as 5 nanoseconds, densities of 1,000 to 6,000 gates, and 44- to 176-pin standard surface mount packages. The ispLSI 2000LV family, an extension of the ispLSI 2000 family, operates using the emerging 3.3-volt power supply standard. Offered with a range of density, performance and package specifications, the ispLSI 2000LV family is targeted towards emerging high-growth, low-voltage system applications in the computing and communication markets.

ISPLSI 3000: The ispLSI 3000 family incorporates an enhanced logic architecture to target higher density applications while retaining high performance. It offers densities of 7,000 to 14,000 gates, and performance of up to 125 MHz, with propagation delays as low as 7.5 nanoseconds. Available in 160- to 304-pin surface mount packages, the 3000 family also incorporates boundary scan test, an attractive feature that provides enhanced testing capabilities important for complex systems.

ISPLSI 6000: The ispLSI 6000 family extends the Company's high-density CPLD density range to 25,000 gates. This family utilizes an innovative cell-based architecture that combines a general purpose high-density CPLD with memory and other function specific circuit blocks. Offered with performance of up to 77 MHz, with propagation delays as low as 15 nanoseconds, the ispLSI 6000 family allows integration of complete logic subsystems in the communications, computing and multimedia markets.

The Company plans to continue to introduce new families of high-density products, as well as improve the performance of existing product families, to meet market needs.

SOFTWARE DEVELOPMENT TOOLS. All of the Company's high-density products are supported by the Company's ispDS-TM- software development tools and ispDS+-TM- software development tools (referred to as "fitters"). Designed to be a low cost, fully integrated development tool, ispDS runs under the Microsoft Windows operating system on a personal computer. ispDS software allows a customer to enter and verify a logic design, perform logic minimization, assign I/O pins and critical speed paths, simulate timing, execute automatic place and route tasks and download a program to an ISP device. Designed to provide a seamless integration of the Company's development tools with standard design environments, ispDS+ software leverages customers' existing investments in third-party CAE tools. Optimized for HDL synthesis, ispDS+ software supports all

popular third party CAE development tool environments running on IBM compatible personal computers as well as workstations from Sun Microsystems and Hewlett-Packard. The Company offers ispDS+ products supporting common third party CAE design tool environments, including Cadence, Data I/O ABEL, Data I/O Synario, Exemplar, Isdata, Logical Devices, Mentor Graphics, OrCAD, Synopsys, Synplicity and ViewLogic. ispDS+ software allows a customer to compile a design developed in a third party environment, assign I/O pins and critical speed paths, simulate and analyze timing, execute automatic place and route tasks and download a program to an ISP device. In fiscal 1997, the Company released new versions of its existing ispDS and ispDS+ software development tools to enhance performance, functionality and ease of use.

The Company also provides several software algorithms that support in-system programming of the Company's ISP devices. These software products include ispCODE-TM-, ispDOWNLOAD-TM-, ispREMOTE-TM- and ispATE-TM-. ispATE enables ISP product programming to be integrated into automatic test equipment ("ATE") on the manufacturing floor.

During fiscal 1997, the number of installed seats of the Company's software development tools, as measured by the Company, grew from over 10,000 to over 17,000. The Company plans to continue to enhance and expand its development tool offerings.

LOW-DENSITY PLDS

The Company offers the industry's broadest line of low-density CMOS PLDs based on its 16 families of GAL products offered in over 200 speed, power, package and temperature range combinations. GAL devices range in complexity from approximately 200 to 1,000 logic gates and are typically assembled in 20-, 24-and 28-pin standard dual in-line packages and in 20- and 28-pin standard plastic leaded chip carrier packages. The Company offers the industry standard GAL16V8, GAL20V8, GAL22V10, GAL20RA10 and GAL20XV10 architectures in a variety of speed grades, with propagation delays as low as 3.5 nanoseconds, the highest performance in the industry. The Company also offers several innovative proprietary extension architectures, the ispGAL-Registered Trademark-22V10, GAL26CV12, GAL18V10, GAL16VP8, GAL20VP8, GAL6001/2, GAL16V8Z and GAL20V8Z, each of which is optimized for specific applications. These product families offer industry leading performance levels, typically with propagation delays as low as 7.5 nanoseconds. The Company extended its GAL line by introducing a family of 3.3-volt industry standard architectures, the GAL16LV8, GAL20LV8, GAL22LV10 and GAL26CLV12 in a variety of speed grades, with propagation delays as low as 3.5 nanoseconds, the highest performance in the industry. Offered with a range of power consumption specifications, these devices are targeted towards emerging high-growth, low-voltage system applications in the communication and computing markets. The Company is currently selling the GAL16LV8D-3.5, the world's fastest PLD available in any technology or operating voltage.

The Company plans to continue to maintain a broad offering of performance leadership, standard and proprietary architecture low-density CMOS PLDs.

The Company's GAL products are supported by industry standard software and hardware development tools marketed by independent manufacturers specifically for PLD applications.

PRODUCT DEVELOPMENT

The Company places great emphasis on product development and believes that continued investment in the development of new products that exploit market trends is required to maintain its competitive position. The Company's product development activities emphasize new high-density PLDs, improvements of its proprietary ISP products and E(2)CMOS processes technologies, performance enhancement and cost reduction of existing products, and extension and enhancement of its software development tools. Product development activities occur in the Company's Hillsboro, Oregon headquarters, its Milpitas, California product development center, and its Shanghai, China design center.

Research and development expenses were $22.9 million, $26.8 million and $27.8 million in fiscal years 1995, 1996 and 1997, respectively. The Company expects to continue to make significant investments in research and development in the future.

OPERATIONS

The Company does not manufacture its silicon wafers. The Company has historically maintained strategic relationships with large semiconductor manufacturers in order to source its finished silicon wafers, allowing the Company to focus its internal resources on product, process and market development. In addition, assembly is performed for the Company by outside suppliers. The Company performs most test operations and reliability and quality assurance processes internally, as the Company believes it can add significant customer value in these areas. The Company has achieved ISO 9001 quality certification, an indication of the Company's high internal operational standards.

WAFER FABRICATION

The majority of the Company's silicon wafer requirements are currently supplied by Seiko Epson Corporation ("Seiko Epson") in Japan pursuant to an agreement with S MOS Systems, Inc. ("S MOS"), an affiliated U.S. distributor of Seiko Epson. See "Licenses and Agreements - Seiko Epson/S MOS." The Company negotiates wafer volumes, prices and terms with Seiko Epson and S MOS on a periodic basis. In addition, the Company receives silicon wafers from United Microelectronics Corporation ("UMC") in Taiwan pursuant to an agreement entered into in 1995. Wafer prices and other purchase terms related to this commitment are subject to periodic adjustment. See " Licenses and Agreements - UMC." A significant interruption in supply from Seiko Epson through S MOS or from UMC would have a material adverse effect on the Company's business. See "Factors Affecting Future Results."

ASSEMBLY

After wafer fabrication and initial testing, the Company ships wafers to independent subcontractors for assembly. During assembly, wafers are separated into individual die and encapsulated in plastic or ceramic packages. Presently, the Company has qualified long-term assembly partners in Hong Kong, Malaysia, the Philippines, South Korea and the United States.

TESTING

The Company electrically tests the die on each wafer prior to shipment for assembly. Following assembly, prior to customer shipment, each product undergoes final testing using test equipment, techniques and quality assurance procedures. Final testing on certain products is performed at independent contractors in Malaysia, the Philippines, South Korea and the United States.

MARKETING, SALES AND CUSTOMERS

The Company sells its products directly to end customers through a network of independent sales representatives and indirectly through a network of distributors. The Company utilizes a direct sales management and field applications engineering organization in combination with manufacturers' representatives and distributors to reach a broad base of potential end customers. The Company's end customers are primarily original equipment manufacturers in the fields of communications, computing, peripherals, instrumentation, industrial controls and military systems. The Company believes its distribution channel is a cost-effective means of reaching end customers.

At March 29, 1997, the Company had 19 sales representatives and five distributors in the United States and Canada. In North America, Arrow Electronics, Inc., Hamilton Hallmark, Insight Electronics, Inc. and Marshall Industries provide nationwide distribution, while Future Electronics provides regional distribution coverage in Canada. The Company has established sales channels in over 30 foreign countries through a network of over 30 sales representatives and distributors. Approximately one-half of the Company's North American sales and most of its foreign sales are made through distributors.

The Company protects each of its North American distributors and some of its foreign distributors against reductions in published prices, and expects to continue this policy in the foreseeable future. The Company also allows returns from these distributors of unsold products under certain conditions. For these reasons, the Company does not recognize revenue until products are resold by these distributors.

The Company provides technical and marketing assistance to its end customers and sales force with engineering staff based in the Company's headquarters, design centers and selected field sales offices. The Company maintains 21 domestic and international sales offices where the Company's field sales managers and applications engineers are based. These offices are located in the metropolitan areas of Atlanta, Austin, Boston, Chicago, Dallas, Denver, Los Angeles, Minneapolis, Orlando, Portland, Raleigh, San Diego, San Jose, Hong Kong, London, Munich, Paris, Seoul, Stockholm, Taipei and Tokyo.

International revenues, including those from Canada, accounted for 47%, 48% and 49% of the Company's revenues in fiscal 1995, 1996 and 1997, respectively. Revenues from Europe were $24.5 million, $37.9 million

and $ 39.9 million, and from Asia were $40.6 million, $52.4 million and $ 52.6 million, in fiscal 1995, 1996 and 1997, respectively. Both international and domestic revenues are generally invoiced in U.S. dollars with the exception of sales in Japan which are invoiced in yen.

The Company's products are sold to a large and diverse group of customers. No individual end customer accounted for more than 5% of revenue in either fiscal 1995, 1996 or 1997. Two distributors accounted for approximately 12% and 11% of revenue in fiscal 1995. One distributor accounted for approximately 11% of revenue in fiscal 1996. No distributor accounted for more than 10% of revenue in fiscal 1997.

The Company's sales are primarily executed against purchase orders for standard products. Customers frequently revise quantities and delivery schedules, without penalty. The Company therefore does not believe that backlog as of any given date is indicative of future revenue.

COMPETITION

The semiconductor industry overall is intensely competitive and is characterized by rapid technological change, rapid rates of product obsolescence and price erosion. The Company's current and potential competitors include a broad range of semiconductor companies, ranging from very large, established companies to emerging companies, many of which have greater financial, technical, manufacturing, marketing and sales resources than the Company.

The principal competitive factors in the CMOS PLD market include product features, price, customer support, and sales, marketing and distribution strength. In the high-density segment, the availability of competitive software development tools is also critical. In addition to product features such as speed, power consumption, reprogrammability, design flexibility and reliability, competition in the PLD market occurs on the basis of price and market acceptance of specific products and technology. The Company believes that it competes favorably with respect to each of these factors. The Company intends to continue to address these competitive factors by working to continually introduce product enhancements and new products, by seeking to establish its products as industry standards in their respective markets, and by working to reduce the manufacturing cost of its products over their life cycle.

In the high-density PLD market, the Company primarily competes directly with Advanced Micro Devices ("AMD") and Altera, both of which offer competing CPLD products. The Company also competes indirectly with manufacturers of FPGA devices such as Actel, Lucent, and Xilinx as well as other semiconductor companies providing non-PLD based logic solutions. As the Company and these other companies seek to expand their markets, competition may increase.

In the low-density PLD market, the Company competes primarily with AMD, a licensee of the Company's GAL patents, which offers a full line of E(2)CMOS GAL-compatible PLDs. Altera, Atmel and Cypress Semiconductor offer products based on similar and competing CMOS technologies and architectures, however, these companies do not offer full product lines.

Although to date the Company has not experienced significant competition from companies located outside the United States, such companies may become a more significant competitive factor in the future. As the

Company and its current competitors seek to expand their markets, competition may increase. Any such increases in competition could have a material adverse effect on the Company's operating results.

PATENTS

The Company seeks to protect its products and wafer fabrication process technology primarily through patents, trade secrecy measures, copyrights, mask work protection, trademark registrations, licensing restrictions, confidentiality agreements and other approaches designed to protect proprietary information. There can be no assurance that others may not independently develop competitive technology not covered by the Company's patents or that measures taken by the Company to protect its technology will be effective.

The Company holds domestic, European and Japanese patents on its PLD products and has patent applications pending in the United States, Japan and under the European Patent Convention. There can be no assurance that pending patent applications or other applications that may be filed will result in issued patents, or that any issued patents will survive challenges to their validity. Although the Company believes that its patents have value, there can be no assurance that the Company's patents, or any additional patents that may be issued in the future, will provide meaningful protection from competition. The Company believes its success will depend primarily upon the technical expertise, experience, creativity and the sales and marketing abilities of its personnel.

Patent and other proprietary rights infringement claims are common in the semiconductor industry. The Company has received a letter from a semiconductor manufacturer stating that it believes a number of its patents, related to product packaging, cover certain products sold by the Company. While the manufacturer has offered to license certain of such patents to the Company, there can be no assurance, on this or any other claim which may be made against the Company, that the Company could obtain a license on terms or under conditions that would be favorable to the Company.

LICENSES AND AGREEMENTS

SEIKO EPSON/S MOS

S MOS, an affiliated U.S. distributor of Seiko Epson, has agreed to provide manufactured wafers to the Company in quantities based on six-month rolling forecasts provided by the Company. The Company has committed to buy certain minimum quantities of wafers per month. The Company's products are manufactured in Japan at Seiko Epson's wafer fabrication facilities and delivered to the Company by S MOS. Prices for the wafers obtained from S MOS are reviewed and adjusted periodically and may be adjusted to reflect prevailing currency exchange rates. See "Factors Affecting Future Results." Daniel S. Hauer, a member of the Company's Board of Directors, is Chairman of the Board of Directors of S MOS.

In July 1994, the Company entered into an advance production payment agreement with Seiko Epson and S MOS, under which it advanced to Seiko Epson $42 million during fiscal 1995 to be used by Seiko Epson to finance additional sub-micron semiconductor wafer manufacturing capacity. Under the terms of the agreement, the advance is to be repaid in the form of advanced technology sub-micron semiconductor wafers. Subject to certain conditions set forth in the agreement, Seiko Epson has agreed to supply, and the Company has agreed to receive, such wafers at a price (in Japanese yen) and volume expected to achieve full repayment of the advance

over a three- to four-year period. In conjunction with the advance production payment agreement, the Company also paid $2 million during fiscal 1995 for the development of sub-micron process technology and the fabrication of engineering wafers to be delivered over the same period. The agreement calls for wafers to be supplied by Seiko Epson through S MOS pursuant to a purchase agreement concluded with S MOS. Total wafer receipts under these agreements aggregated approximately $30.2 million as of March 29, 1997.

In March 1997, the Company entered into a second advance production payment agreement with Seiko Epson and SMOS under which it agreed to advance approximately $90 million, payable over two years, to Seiko Epson to finance construction of an eight-inch sub-micron semiconductor wafer manufacturing facility. The timing of the payments is related to certain milestones in the development of the facility. Under the terms of the agreement, the advance is to be repaid with semiconductor wafers over a multi-year period. The agreement calls for wafers to be supplied by Seiko Epson through S MOS pursuant to purchase agreements concluded with S MOS. The Company also has an option under the agreement to advance Seiko Epson an additional $60 million for additonal wafer supply under similar terms. The first payment pursuant to this agreement, approximately $17.0 million, was made during March 1997.

UMC

The Company entered into a series of agreements with UMC in September 1995 pursuant to which the Company agreed to join UMC and several other companies to form a separate Taiwanese company, UICC, for the purpose of building and operating an advanced semiconductor manufacturing facility in Taiwan, Republic of China. Under the terms of the agreement, the Company will invest approximately $53 million, payable in three installments, for a 10% equity interest in UICC and the right to receive a percentage of the facility's wafer production at market prices. The timing of the payments is related to certain milestones in the development of the advanced semiconductor manufacturing facility. The first payment, in the amount of $13.7 million, was paid in January 1996, the second payment, in the amount of approximately $25.8 million, was paid during January 1997, and the final payment is anticipated to be required within the six-month period ending December 1997.

AMD

In November 1987, as part of the settlement of a patent infringement suit against the Company, the Company and Monolithic Memories, Inc. ("MMI", subsequently merged with AMD) entered into an agreement cross-licensing each other's patents covering programmable and reprogrammable logic devices based on patent applications having a first filing date prior to November 1989. The agreement was subsequently amended in May 1989 by the Company and AMD, the successor to the rights and obligations of MMI in the original agreement. The amendment covers those patents relating to PLD products which are based on patent applications originally filed by the Company, MMI and AMD prior to December 31, 1991. The license terminates, with respect to certain patents asserted by AMD, to cover the Company's current principal products if the Company is acquired by a semiconductor manufacturer with sales in excess of a stated amount or by certain types of companies headquartered in designated Asian countries. No license has been granted to either party for any copyright work, trademark or process technology and, therefore, AMD has not been licensed to use the GAL trademark on its products.

FACTORS AFFECTING FUTURE RESULTS

The Company believes that its future operating results will be subject to quarterly variations based upon a wide variety of factors, including the cyclical nature of both the semiconductor industry and the end markets addressed by the Company's products, the timing of new product introductions, price erosion, product obsolescence, substantial adverse currency exchange rate movements, variations in product mix, scheduling, rescheduling and cancellation of large orders, competitive factors, the availability of manufacturing capacity and wafer supply, the ability to achieve volume production at Seiko Epson's new eight-inch facility or UICC, the ability to develop and implement new process technologies, fluctuations in manufacturing yields, changes in effective tax rates and litigation expenses. Due to these and other factors, the Company's past results are a less useful predictor of future results than is the case in more mature and stable industries. The Company has increased its level of operating expenses and investment in manufacturing capacity in anticipation of future growth in revenues, primarily from increased sales of its high-density products. To the extent that this revenue growth does not materialize, the Company's operating results would be adversely affected.

The semiconductor industry is highly cyclical and has been subject to significant downturns at various times that have been characterized by diminished product demand, production overcapacity and accelerated erosion of average selling prices. The Company's rate of growth in recent periods has been positively and negatively impacted by trends in the semiconductor industry. Any material imbalance in industry-wide production capacity relative to demand, shift in industry capacity toward products competitive with the Company's products, reduced demand or reduced growth in demand or other factors could result in a decline in the demand for or the prices of the Company's products and could have a material adverse effect on the Company's operating results.

The market price of the Company's common stock could be subject to significant fluctuations in response to variations in quarterly operating results, shortfalls in revenues or earnings from levels expected by securities analysts and other factors such as announcements of technological innovations or new products by the Company or by the Company's competitors, government regulations, developments in patent or other proprietary rights, and developments in the Company's relationships with parties to collaborative agreements. In addition, the stock market can experience significant price fluctuations. These fluctuations often are unrelated to the operating performance of the specific companies whose stocks are traded. Broad market fluctuations, as well as economic conditions generally and in the semiconductor industry specifically, could adversely affect the market price of the Company's common stock.

The Company does not manufacture finished silicon wafers. Its products, however, require wafers manufactured with state-of-the-art fabrication equipment and techniques. Accordingly, the Company's strategy has been to maintain relationships with large semiconductor manufacturers for the production of its wafers. Currently all of its silicon wafers are manufactured by either Seiko Epson in Japan or UMC in Taiwan. A significant interruption in supply from Seiko Epson, through S MOS, Seiko Epson's affiliated U.S. distributor, or from UMC would have a material adverse effect on the Company's business.

Worldwide manufacturing capacity for silicon wafers is limited and inelastic. Therefore, significant increases in demand or interruptions in supply could adversely affect the Company. Through fiscal 1997, the Company was successful in obtaining adequate wafer capacity commitments; however, it has in the past experienced delays in obtaining wafers. Although current commitments are anticipated to be adequate through fiscal 1998, there can be

no assurance that existing capacity commitments will be sufficient to permit the Company to satisfy all of its customers' demand in future periods. The Company negotiates wafer prices and certain wafer supply commitments with Seiko Epson, S MOS and UMC on an annual basis, and, in some cases, as frequently as semiannually. Moreover, wafer prices and commitments are subject to continuing review and revision by the parties. There can be no assurance that Seiko Epson, S MOS or UMC will not reduce their allocations of wafers or increase prices to the Company in future periods or that any such reduction in supply could be offset pursuant to arrangements with alternate sources of supply. If any substantial reduction of supply or substantial price increase were to occur, the Company's operating results could be materially adversely affected.

The Company's wafer purchases from Seiko Epson are denominated in Japanese yen. In the past, the dollar has lost substantial value with respect to the yen. There is no assurance that the value of the dollar with respect to the yen will not again experience substantial deterioration. Any substantial continued deterioration of dollar-yen exchange rates could have a material adverse effect on the Company's results of operations.

The Company depends upon wafer suppliers to produce wafers with acceptable yields and to deliver them to the Company in a timely manner. Substantially all of the Company's revenues are derived from products based on E(2)CMOS process technology. Successful implementation of the Company's proprietary E(2)CMOS process technology, UltraMOS, requires a high degree of coordination between the Company and its wafer supplier. Therefore, significant lead time is required to reach volume production at a new wafer supply location such as Seiko Epson's new eight-inch facility or UICC. Accordingly, there can be no assurance that volume production at Seiko Epson's new eight-inch facility or UICC will be achieved in the near term or at all. The manufacture of high performance E(2)CMOS semiconductor wafers is a complex process that requires a high degree of technical skill, state-of-the-art equipment and effective cooperation between the wafer supplier and the circuit designer to produce acceptable yields. Minute impurities, errors in any step of the fabrication process, defects in the masks used to print circuits on a wafer and other factors can cause a substantial percentage of wafers to be rejected or numerous die on each wafer to be non-functional. As is common in the semiconductor industry, the Company has from time to time experienced in the past, and expects that it will experience in the future, production yield problems and delivery delays. Any prolonged inability to obtain adequate yields or deliveries could adversely affect the Company's operating results.

The Company expects that, as is customary in the semiconductor business, it will in the future seek to convert its fabrication process technology to larger wafer sizes, to smaller device geometries or to new or additional suppliers in order to maintain or enhance its competitive position. Such conversions entail inherent technological risks that could adversely affect yields and delivery times and could have a material adverse impact on the Company's operating results. To a considerable extent, the Company's ability to execute its strategies will depend upon its ability to maintain and enhance its advanced process technologies. As the Company does not presently operate its own wafer fabrication or process development facility, the Company depends upon silicon wafer manufacturers to provide the facilities and support for its process development. In light of this dependency and the intensely competitive nature of the semiconductor industry, there is no assurance that either process technology development or timely product introduction can be sustained in the future.

In addition, other unanticipated changes in or disruptions of the Company's wafer supply arrangements could reduce product availability, increase cost or impair product quality and reliability. Many of the factors that could result in such changes are beyond the Company's control. For example, a disruption of operations at Seiko

Epson's or UMC's manufacturing facilities as a result of a work stoppage, fire, earthquake or other natural disaster, would cause delays in shipments of the Company's products and would have a material adverse effect on the Company's operating results.

The Company's finished silicon wafers are assembled and packaged by independent subcontractors located in the Philippines, South Korea and Malaysia, Hong Kong and the United States. Although the Company has not yet experienced significant problems or interruptions in supply from its assembly contractors, any prolonged work stoppages or other failure of these contractors to supply finished products could have a material adverse effect on the Company's operating results.

Because of the rapid rate of technological change in the semiconductor industry, the Company's success will ultimately depend in large part on its ability to introduce new products on a timely basis that meet a market need at a competitive price and with acceptable margins as well as enhancing the performance of its existing products. The success of new products, including the Company's high-density product families, depends on a variety of factors, including product selection, timely and efficient completion of product design, timely and efficient implementation of manufacturing and assembly processes, product performance, quality and reliability in the field and effective sales and marketing. Because new product development commitments must be made well in advance of sales, new product decisions must anticipate both future demand and the technology that will be available to supply that demand. New and enhanced products are continually being introduced into the Company's markets by others, and these products can be expected to affect the competitive environment in the markets in which they are introduced. There is no assurance that the Company will be successful in enhancing its existing products or in selecting, developing, manufacturing, marketing and selling new products.

Future revenue growth will be largely dependent on market acceptance of the Company's new and proprietary products, including its high-density product families, and market acceptance of the Company's proprietary software development tools. There can be no assurance that the Company's product and process development efforts will be successful or that new products, including the Company's high-density products, will continue to achieve market acceptance. If the Company were unable to successfully define, develop and introduce competitive new products in a timely manner, its future operating results would be adversely affected.

The semiconductor industry is intensely competitive and is characterized by rapid technological change, sudden price fluctuations, general price erosion, rapid rates of product obsolescence, periodic shortages of materials and manufacturing capacity and variations in manufacturing costs and yields. The Company's competitive position is affected by all of these factors and by industry competition for effective sales and distribution channels. The Company's existing and potential competitors range from established major domestic and international semiconductor companies to emerging companies. Many of the Company's competitors have substantially greater financial, technological, manufacturing, marketing and sales resources than the Company. The Company faces direct competition from companies that have developed or licensed similar technology and from licensees of the Company's products and technology. The Company also faces indirect competition from a wide variety of semiconductor companies offering products and solutions based on alternative technologies. Although to date the Company has not experienced significant competition from companies located outside the United States, such companies may become a more significant competitive factor in the future. As the Company and its current competitors seek to expand their markets, competition may increase, which could have an adverse effect on the Company's operating results. Competitors' development of new technologies that have price/performance

characteristics superior to the Company's technologies could adversely affect the Company's results of operations. There can be no assurance that the Company will be able to develop and market new products successfully or that the products introduced by others will not render the Company's products or technologies non-competitive or obsolete. The Company expects that its markets will become more competitive in the future.

In an effort to secure additional wafer supply, the Company may from time to time consider various arrangements, including joint ventures with, minority investments in, advanced purchase payments to, loans to or similar arrangements with independent wafer manufacturers in exchange for committed production capacity. Such arrangements are becoming common within the industry as independent wafer manufacturers increasingly seek to require their customers to share a portion of the cost of capital intensive wafer fabrication facilities. In 1994, the Company entered into an advanced production payment agreement with Seiko Epson pursuant to which it advanced a total of $42 million to Seiko Epson. In September 1995, the Company entered into an agreement with UMC under which it will invest a total of approximately $53 million for a 10% equity interest in a separate Taiwanese company (UICC) providing for the formation of a joint venture with UMC and several other companies for the purpose of building and operating an advanced semiconductor manufacturing facility. In March 1997, the Company entered into a second advanced production payment agreement with Seiko Epson pursuant to which it plans to advance up to $150 million to Seiko Epson. To the extent the Company pursues any other such transactions with Seiko Epson, UMC or any other wafer manufacturers, such transactions could entail even greater levels of investment requiring the Company to seek additional equity or debt financing to fund such activities. There can be no assurance that any such additional funding could be obtained when needed or, if available, on terms acceptable to the Company.

The Company's success depends in part on its proprietary technology. While the Company attempts to protect its proprietary technology through patents, copyrights and trade secrets, it believes that its success will depend more upon technological expertise, continued development of new products, and successful market penetration of its silicon and software products. There can be no assurance that the Company will be able to protect its technology or that competitors will not be able to develop similar technology independently. The Company currently has a number of United States and foreign patents and patent applications. There can be no assurance that the claims allowed on any patents held by the Company will be sufficiently broad to protect the Company's technology, or that any patents will issue from any application pending or filed by the Company. In addition, there can be no assurance that any patents issued to the Company will not be challenged, invalidated or circumvented or that the rights granted thereunder will provide competitive advantages to the Company.

The semiconductor industry is generally characterized by vigorous protection and pursuit of intellectual property rights and positions, which have on occasion resulted in protracted litigation that utilizes cash and management resources, which can have a significant adverse effect on operating results. The Company has received a letter from a semiconductor manufacturer stating that it believes a number of its patents related to product packaging cover certain products sold by the Company. While the manufacturer has offered to license certain of such patents to the Company, there can be no assurance, on this or any other claim which may be made against the Company, that the Company could obtain a license on terms or under conditions that would be favorable to the Company. In addition, there can be no assurance that other intellectual property claims will not be made against the Company in the future or that the Company will not be prohibited from using the technologies subject to such claims or be required to obtain licenses and make corresponding royalty payments for past or future use.

International revenues accounted for 47%, 48% and 49% of the Company's revenues for fiscal 1995, 1996 and 1997, respectively. The Company believes that international revenues will continue to represent a significant percentage of revenues. International revenues and operations may be adversely affected by the imposition of governmental controls, export license requirements, restrictions on the export of technology, political instability, trade restrictions, changes in tariffs and difficulties in staffing and managing international operations.

The future success of the Company is dependent, in part, on its ability to attract and retain highly qualified technical and management personnel, particularly highly skilled engineers involved in new product, both silicon and software, and process technology development. Competition for such personnel is intense. There can be no assurance that the Company will be able to retain its existing key technical and management personnel or attract additional qualified employees in the future. The loss of key technical or management personnel could delay product development cycles or otherwise have a material adverse effect on the Company's business.

The Company currently depends on foreign manufacturers -- Seiko Epson, a Japanese company, and UMC, a Taiwanese company -- for the manufacture of all of its finished silicon wafers, and anticipates depending on UICC, a Taiwanese company, for the manufacture of a portion of its finished silicon wafers. In addition, after wafer manufacturing is completed and each wafer is tested, products are assembled by subcontractors in South Korea, the Philippines, Hong Kong, and Malaysia. Although the Company has not experienced any interruption in supply from its subcontractors, the social and political situations in these countries can be volatile, and any prolonged work stoppages or other disruptions in the Company's ability to manufacture and assemble its products would have a material adverse effect on the Company's results of operations. Furthermore, economic risks, such as changes in currency exchange rates, tax laws, tariffs, or freight rates, or interruptions in air transportation, could have a material adverse effect on the Company's results of operations.

EMPLOYEES

As of March 29, 1997, the Company had 531 full-time employees. The Company believes that its future success will depend, in part, on its ability to continue to attract and retain highly skilled technical, marketing and management personnel.

None of the Company's employees is subject to a collective bargaining agreement. The Company has never experienced a work stoppage and considers its employee relations good.

ITEM 2. PROPERTIES

The Company's corporate offices, testing and principal research and design facilities are located in two adjacent buildings owned by the Company in Hillsboro, Oregon comprising a total of 90,000 square feet. The Company's executive, administrative, marketing and production activities are also located at these facilities. The Company leases a 41,000 square foot research and design facility in Milpitas, California under a five-year term which expires in August 1998.

The Company leases space in various locations in the United States for its domestic sales offices, and also leases space in Hong Kong, London, Munich, Paris, Seoul, Stockholm, Taipei and Tokyo for its international sales offices. The Company owns a 13,000 square foot research and development facility and approximately 6,000 square feet of dormitory facilities in Shanghai.

ITEM 3. LEGAL PROCEEDINGS.

There are no material pending legal proceedings to which the Company is a party or to which any of its property is subject.

ITEM 4. SUBMISSION OF MATTERS TO A VOTE OF SECURITY HOLDERS.

Not applicable.

ITEM 4(a). EXECUTIVE OFFICERS OF THE REGISTRANT.

As of June 12, 1997, the executive officers of the Company are as set forth below.

Name	Age	Position
Cyrus Y. Tsui	51	President, Chief Executive Officer and Chairman of the Board
Steven A. Laub	38	Senior Vice President and Chief Operating Officer
Stephen A. Skaggs	34	Senior Vice President, Chief Financial Officer and Secretary
Jonathan K. Yu	56	Corporate Vice President, Business Development
Martin R. Baker	41	Vice President and General Counsel
Randy D. Baker	38	Vice President, Manufacturing
Albert L. Chan	47	Vice President, California Product Development
Stephen M. Donovan	46	Vice President, International Sales
Paul T. Kollar	51	Vice President, Sales
Rodney F. Sloss	53	Vice President, Finance
Kenneth K. Yu	49	Vice President and Managing Director, Lattice Asia

Executive officers of the Company are appointed by the Board of Directors to serve at the discretion of the Board and hold office until the officers' successors are appointed.

Cyrus Y. Tsui joined the Company in September 1988 as President, Chief Executive Officer and Director, and in March 1991 was named Chairman of the Board. From 1987 until he joined the Company, Mr. Tsui was Corporate Vice President and General Manager of the Programmable Logic Division of AMD. He was Vice President and General Manager of the Commercial Products Division of Monolithic Memories Incorporated from 1983 until the merger with AMD in 1987. Mr. Tsui has held technical and managerial positions in the semiconductor industry for over 25 years. He has worked in the programmable logic industry since its inception.

Steven A. Laub joined the Company in June 1990 as Vice President and General Manager. He was elected Senior Vice President and Chief Operating Officer in August 1996.

Stephen A. Skaggs joined the Company in December 1992 as Director, Corporate Development. He was elected Senior Vice President, Chief Financial Officer and Secretary in August 1996. From 1984 until he joined the Company, Mr. Skaggs was with Bain & Company, Inc., an international management consulting firm.

Jonathan K. Yu joined the Company in February 1992 as Vice President, Operations. He was elected Corporate Vice President, Business Development in August 1996. Mr. Yu has held technical and managerial positions in the semiconductor industry for over 30 years.

Martin R. Baker joined the Company in January 1997 as Vice President and General Counsel. From 1991 until he joined the Company, Mr. Baker held legal positions with Altera Corporation.

Randy D. Baker joined the Company in April 1985 as Manager, Manufacturing and was promoted in 1988 to Director, Manufacturing. He was elected Vice President, Manufacturing in August 1996. Mr. Baker has worked in the semiconductor industry for over 15 years.

Albert L. Chan joined the Company in May 1989 as California Design Center Manager and was promoted in 1991 to Director, California Product Development Center. He was elected Vice President, California Product Development in August 1993. Mr. Chan has worked in the programmable logic industry since 1983.

Stephen M. Donovan joined the Company in October 1989 and has served as Director of Marketing and Director of International Sales. He was elected Vice President, International Sales in August 1993. Mr. Donovan has worked in the programmable logic industry since 1982.

Paul T. Kollar joined the Company in November 1985 and since that time has served as Vice President, Sales and Vice President, Sales and Marketing. Mr. Kollar has worked in the semiconductor industry for over 25 years.

Rodney F. Sloss joined the Company in May 1994 as Vice President, Finance. From 1992 to 1994, Mr. Sloss served as Chief Financial Officer of The Alexander Haagen Company, a real estate developer.

Kenneth K. Yu joined the Company in January 1991 as Director of Process Technology. He has served as Managing Director, Lattice Asia since November 1992 and was elected Vice President, Lattice Asia in August 1993. Mr. Yu has held technical and managerial positions in the semicondutor industry for over 20 years.

PART II

ITEM 5. MARKET FOR THE REGISTRANT'S COMMON STOCK AND RELATED STOCKHOLDER MATTERS.

The Company's common stock is traded on the over-the-counter market and prices are quoted on the Nasdaq National Market under the symbol "LSCC". The following table sets forth the high and low sale prices for the common stock for the last two fiscal years and for the period since March 29, 1997. On June 12, 1997, the last reported sale price of the common stock was $55 3/8. All share prices have been adjusted for the three-for-two stock split effected in the form of a stock dividend which was paid on July 6, 1993. As of June 12, 1997, the Company had approximately 290 beneficial owners of its common stock.

	High	Low
Fiscal 1996:		
First Quarter	$37 1/8	$23
Second Quarter	43	28 7/8
Third Quarter	42 1/8	27 5/8
Fourth Quarter	37 3/8	26 3/8
Fiscal 1997:		
First Quarter	$36 1/4	$21 5/8
Second Quarter	31 1/2	19 3/4
Third Quarter	47	27 1/2
Fourth Quarter	54 7/8	39 3/4
Fiscal 1998:		
First Quarter (through June 12, 1997)	$62 5/8	$43 1/4

The payment of dividends on the common stock is within the discretion of the Company's Board of Directors. The Company intends to retain earnings to finance the growth of its business. The Company has not paid cash dividends on its common stock and the Board of Directors does not expect to declare cash dividends on the common stock in the near future.

ITEM 6. SELECTED FINANCIAL DATA.

The information required by this Item is set forth in the Company's 1997 Annual Report to Stockholders at page 17 under the caption "Selected Financial Data", which information is incorporated herein by reference.

ITEM 7. MANAGEMENT'S DISCUSSION AND ANALYSIS OF FINANCIAL CONDITION AND RESULTS OF OPERATIONS.

The information required by this Item is set forth in the Company's 1997 Annual Report to Stockholders at pages 14 through 16 under the caption "Management's Discussion and Analysis of Financial Condition and Results of Operations", which information is incorporated herein by reference.

ITEM 8. FINANCIAL STATEMENTS AND SUPPLEMENTARY DATA.

FINANCIAL STATEMENTS

The information required by this Item is set forth in the Company's 1997 Annual Report to Stockholders, at pages 18 through 28, which information is incorporated herein by reference.

No other schedules are included because the required information is inapplicable, not required or is presented in the financial statements or related notes thereto.

ITEM 9. CHANGES IN AND DISAGREEMENTS WITH ACCOUNTANTS ON ACCOUNTING AND FINANCIAL DISCLOSURE.

Not applicable.

With the exception of the information expressly incorporated by reference from the Annual Report to Stockholders into Parts II and IV of this Form 10-K, the Company's Annual Report to Stockholders is not to be deemed filed as part of this Report.

PART III

Certain information required by Part III is omitted from this Report in that the Company will file its definitive proxy statement for the Annual Meeting of Stockholders to be held on August 11, 1997, pursuant to Regulation 14A of the Securities Exchange Act of 1934 (the "Proxy Statement"), not later than 120 days after the end of the fiscal year covered by this Report, and certain information included in the Proxy Statement is incorporated herein by reference.

ITEM 10. DIRECTORS AND EXECUTIVE OFFICERS OF THE REGISTRANT.

The information required by this item with respect to directors of the Company is included under "Proposal 1: Election of Directors" in the Company's Proxy Statement and is incorporated herein by reference. Information with respect to executive officers of the Company is included under Item 4(a) of Part I of this Report and is incorporated herein by reference.

ITEM 11. EXECUTIVE COMPENSATION.

The information required by this item with respect to executive compensation is included under "Proposal 1: Election of Directors," "Executive Compensation" and "Comparison of Total Cumulative Stockholder Return" in the Company's Proxy Statement and is incorporated herein by reference.

ITEM 12. SECURITY OWNERSHIP OF CERTAIN BENEFICIAL OWNERS AND MANAGEMENT.

The information required by this Item is included in the Company's Proxy Statement under the caption "Security Ownership of Certain Beneficial Owners and Management" and is incorporated herein by reference.

ITEM 13. CERTAIN RELATIONSHIPS AND RELATED TRANSACTIONS.

The information required by this Item is included under "Proposal 1: Election of Directors - Transactions with Management" in the Company's Proxy Statement and is incorporated herein by reference.

PART IV

ITEM 14. EXHIBITS, FINANCIAL STATEMENT SCHEDULES AND REPORTS ON FORM 8-K.

(a)(1) and (2) FINANCIAL STATEMENTS AND FINANCIAL STATEMENT SCHEDULES.

The information required by this item is included under Item 8 of this Report.

(a)(3) EXHIBITS.

3.1 Certificate of Incorporation, as amended (Incorporated by reference to Exhibit 3.1 filed with the Company's Annual Report on Form 10-K for the fiscal year ended March 31, 1990).

3.2 Bylaws, as amended (Incorporated by reference to Exhibit 3.2 filed with the Company's Annual Report on Form 10-K for the fiscal year ended March 30, 1991).

4.1 Preferred Shares Rights Agreement dated as of September 11, 1991 between Lattice Semiconductor Corporation and First Interstate Bank of Oregon, N.A., as Rights Agent (Incorporated by reference to Exhibit 1 filed with the Company's Registration Statement on Form 8-A on September 13, 1991).

10.3 Patent License Agreement dated November 10, 1989 between Monolithic Memories, Inc. and Lattice Semiconductor Corporation, as amended (Incorporated by reference to Exhibit 10.3, File No. 33-31231).(1)

10.4 Production and Non-exclusive License Agreement dated January 19, 1987 between Lattice Semiconductor Corporation and SGS Semiconductor Corporation (Incorporated by reference to Exhibit 10.4, File No. 33-31231).(1)

10.5 Manufacturing Agreement dated February 18, 1988 between Lattice Semiconductor Corporation and S MOS Systems, Inc. (Incorporated by reference to Exhibit 10.5, File No. 33-35427).(1)

10.6 Extension effective December 31, 1990 to Manufacturing Agreement dated February 18, 1988 between Lattice Semiconductor Corporation and S MOS Systems, Inc. (Incorporated by reference to Exhibit 10.6 filed with the Company's Annual Report on Form 10-K for the fiscal year ended March 30, 1991).

10.7 Form of Distributor Agreement (Incorporated by reference to Exhibit 10.6, File No. 33-31231).

10.8 Form of Representative Agreement (Incorporated by reference to Exhibit 10.7, File No. 33-31231).

10.9 * Lattice Semiconductor Corporation 1988 Stock Incentive Plan, as amended (Incorporated by reference to Exhibit 10.9 filed with the Company's Annual Report on Form 10-K for the fiscal year ended March 28, 1992).

10.10 * Form of Stock Option Agreement (Incorporated by reference to Exhibit 10.9, File No. 33-31231).

10.11 * Employment Letter dated September 2, 1988 from Lattice Semiconductor Corporation to Cyrus Y. Tsui (Incorporated by reference to Exhibit 10.10, File No. 33-31231).

10.12 Form of Proprietary Rights Agreement (Incorporated by reference Exhibit 10.11, File No. 33-31231).

10.13 * Outside Directors Compensation Plan (Incorporated by reference to Exhibit 10.12, File No. 33-31231).

10.14 * Amended Outside Directors Stock Option Plan (Incorporated by reference to Exhibit 10.13, File No. 33-35427).

10.15 * 1993 Outside Directors Stock Option Plan (Incorporated by reference to Exhibit 10.15 filed with the Company's Annual Report on Form 10-K for the fiscal year ended April 3, 1993).

10.16 * Employee Stock Purchase Plan, as amended (Incorporated by reference to Exhibit 10.16 filed with the Company's Annual Report on Form 10-K for the fiscal year ended April 3, 1993).

10.17 Advance Production Payment Agreement dated July 5, 1994 among Lattice Semiconductor Corporation and Seiko Epson Corporation and S-MOS Systems, Inc. (Incorporated by reference to Exhibit 10.17 filed with the Company's Annual Report on Form 10-K for the fiscal year ended April 1, 1995). (1)

10.18 Engineering Payment Agreement dated July 5, 1994 among Lattice Semiconductor Corporation and Seiko Epson Corporation and S-MOS Systems, Inc. (Incorporated by reference to Exhibit 10.18 filed with the Company's Annual Report on Form 10-K for the fiscal year ended April 1, 1995). (1)

10.19 Bridge Capacity Letter dated September 12, 1995 between Lattice Semiconductor Corporation and United Microelectronics Corporation. (Incorporated by reference to Exhibit 10.1 filed with the Company's Current Report on Form 8-K dated September 28, 1995)(1).

10.20 Foundry Venture Side Letter dated September 13, 1995 among Lattice Semiconductor Corporation, United Microelectronics Corporation and FabVen (Incorporated by reference to Exhibit 10.2 filed with the Company's Current Report on Form 8-K dated September 28, 1995)(1).

10.21 FabVen Foundry Capacity Agreement dated as of August ___, 1995 among FabVen, United Microelectronics Corporation and Lattice Semiconductor Corporation (Incorporated by reference to Exhibit 10.3 filed with the Company's Current Report on Form 8-K dated September 28, 1995)(1).

10.22 Foundry Venture Agreement dated as of August ___, 1995, between Lattice Semiconductor Corporation and United Microelectronics Corporation (Incorporated by reference to Exhibit 10.4 filed with the Company's Current Report on Form 8-K dated September 28, 1995)(1).

10.23 Advance Production Payment Agreement dated March 17, 1997 among Lattice Semiconductor Corporation and Seiko Epson Corporation and S MOS Systems, Inc. (2)

10.24 Lattice Semiconductor Corporation 1996 Stock Incentive Plan (Incorporated by reference to Exhibit 4.1 filed on Form S-8 dated November 7, 1996).

11.1 Computation of Net Income Per Share.

13.1 1997 Annual Report to Stockholders

21.1 Subsidiaries of the Registrant.

23.1 Consent of Independent Accountants.

24.1 Power of Attorney (see pages 27-28).

27 Financial Data Schedule for Twelve Months Ended March 29, 1997.

_____

(1) Pursuant to Rule 24b-2 under the Securities Exchange Act of 1934, confidential treatment has been granted to portions of this exhibit, which portions have been deleted and filed separately with the Securities and Exchange Commission.

(2) Pursuant to Rule 24b-2 under the Securities Exchange Act of 1934, confidential treatment has been requested for portions of this exhibit, which portions have been deleted and filed separately with the Securities and Exchange Commission.

* Management contract or compensatory plan or arrangement required to be filed as an Exhibit to this Annual Report on Form 10-K pursuant to Item 14(c) thereof.

(b) No reports on Form 8-K were filed during the last quarter of fiscal 1997.

(c) See (a)(3) above.

(d) See (a)(1) and (2) above.

SIGNATURES

Pursuant to the requirements of Section 13 or 15(d) of the Securities Exchange Act of 1934, the Registrant has duly caused this Report to be signed on its behalf by the undersigned, thereunto duly authorized, in the City of Hillsboro, State of Oregon, on the 26th of June, 1997.

LATTICE SEMICONDUCTOR CORPORATION

By: /s/Stephen A. Skaggs

Stephen A. Skaggs, Senior Vice President, Chief Financial Officer and Secretary

POWER OF ATTORNEY

KNOW ALL PERSONS BY THESE PRESENTS, that each person whose signature appears below constitutes and appoints Cyrus Y. Tsui and Stephen A. Skaggs, jointly and severally, his attorneys-in-fact, each with the power of substitution, for him in any and all capacities, to sign any amendments to this Report on Form 10-K, and to file the same, with exhibits thereto and other documents in connection therewith, with the Securities and Exchange Commission, hereby ratifying and confirming all that each of said attorneys-in-fact, or his substitute or substitutes, may do or cause to be done by virtue hereof.

Pursuant to the requirements of the Securities Exchange Act of 1934, this Report has been signed below by the following persons on the 26th day of June, 1997 on behalf of the Registrant and in the capacities indicated:

Signature	Title
/s/Cyrus Y. Tsui Cyrus Y. Tsui	President, Chief Executive Officer and Chairman of the Board (Principal Executive Officer)
/s/Stephen A. Skaggs Stephen A. Skaggs	Senior Vice President, Chief Financial Officer and Secretary (Principal Financial Officer)
/s/Mark O. Hatfield Mark O. Hatfield	Director
/s/Daniel S. Hauer Daniel S. Hauer	Director

Signature	Title
/s/Harry A. Merlo Harry A. Merlo	Director
/s/Larry W. Sonsini Larry W. Sonsini	Director
/s/Douglas C. Strain Douglas C. Strain	Director

REPORT OF INDEPENDENT ACCOUNTANTS
ON FINANCIAL STATEMENT SCHEDULE

To the Board of Directors
of Lattice Semiconductor Corporation

Our audits of the consolidated financial statements referred to in our report dated April 16, 1997 appearing in the 1997 Annual Report to Stockholders of Lattice Semiconductor Corporation (which report and consolidated financial statements are incorporated by reference in this Annual Report on Form 10-K) also included an audit of the Financial Statement Schedule listed in Item 14(a)(2) of this Form 10-K. In our opinion, this Financial Statement Schedule presents fairly, in all material respects, the information set forth therein when read in conjunction with the related consolidated financial statements.

/s/ Price Waterhouse LLP

PRICE WATERHOUSE LLP

Portland, Oregon
April 16, 1997

SCHEDULE VIII

LATTICE SEMICONDUCTOR CORPORATION

VALUATION AND QUALIFYING ACCOUNTS

(IN THOUSANDS)

COLUMN A CLASSIFICATION	COLUMN B BALANCE AT BEGINNING OF PERIOD	COLUMN C CHARGED TO COSTS AND EXPENSES	COLUMN D CHARGED TO OTHER ACCOUNTS (DESCRIBE)	COLUMN E WRITE-OFFS NET OF RECOVERIES	COLUMN F BALANCE AT END OF PERIOD
Year ended April 1, 1995:					
Allowance for deferred tax asset	$2,420	$ 399	--	--	$2,819
Allowance for doubtful accounts	697	75	--	(29)	743
	$3,117	$ 474	$ --	$ (29)	$3,562
Year ended March 30, 1996:					
Allowance for deferred tax asset	$2,819	$(483)	--	--	$2,336
Allowance for doubtful accounts	743	70	--	(13)	800
	$3,562	$ (413)	$ --	$ (13)	$3,136
Year ended March 29, 1997:					
Allowance for deferred tax asset	$2,336	$(340)	--	--	$1,996
Allowance for doubtful accounts	800	70	--	4	874
	$3,136	$ (270)	$ --	$ 4	$2,870

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

ADVANCE PRODUCTION PAYMENT AGREEMENT

THIS ADVANCE PAYMENT AGREEMENT ("this Agreement"), is entered into this March 17, 1997, by and among SEIKO EPSON CORPORATION, a Japanese corporation having its principal place of business at 3-5, Owa 3-chome, Suwa-shi, Nagano-ken 392, Japan ("Epson"), S MOS Systems Inc., a California corporation, having a place of business at 150 River Oaks Parkway, San Jose, California 95134-1951, U.S.A. ("SMOS") and Lattice Semiconductor Corporation, a Delaware corporation, having a place of business at 5555 N.E. Moore Ct., Hillsboro, Oregon 97124-6421, U.S.A. ("Lattice").

1 BACKGROUND

1.1 EPSON

Epson is in the business of designing, manufacturing, testing and selling semiconductor devices, among other products. Epson manufactures such semiconductor devices at its plant located at 281 Fujimi, Fujimi-machi, Suwa-gun, Nagano-ken 399-02, Japan (the "Fujimi Facility") and its plant located at 166-3 Jurizuka, Sakata-shi, Yamagata-ken 998-01, Japan (the "Sakata Facility").

1.2 SMOS

SMOS is an affiliate of Epson and is Epson's authorized distributor in the United States for semiconductor devices. SMOS is in the business of designing, testing and selling semiconductor devices. SMOS conducts its business at its office located at 150 River Oaks Parkway, San Jose, CA 95134-1951, U.S.A.

1.3 LATTICE

Lattice is in the business of designing, developing, manufacturing and marketing and selling both high- and low-density E(2)-CMOS-Registered Trademark- programmable logic devices and related development system software.

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

1.4 SCOPE OF AGREEMENT

Epson and SMOS have an ongoing business relationship with Lattice whereby Epson fabricates semiconductor devices for Lattice. The parties entered into an advance production payment agreement dated July 5, 1994 for development and manufacture of 0.8-0.5 micron, 2-3 metal layer, 6 inch CMOS semiconductor wafers. The parties desire to expand their relationship. Specifically, Lattice desires to develop and sell high performance, advanced architecture semiconductor devices, and Epson desires to construct (*) CMOS process line installed in the Site (as hereafter defined) in order to fabricate such semiconductor wafers and distribute them to Lattice through SMOS. Accordingly, the parties agree that Lattice will pay to Epson an advance production payment ("APP") only to be used as a credit to purchase the Products from Epson through SMOS over a specified period of time in accordance with this Agreement. The Products shall be first sold to SMOS from Epson, and then be sold to Lattice from SMOS under the terms and conditions of the Purchase Agreement (as hereafter defined). (In the event that SMOS has fallen into a situation where it is unable to play the role required under this Agreement for any reason specifically prescribed in this Agreement or any other reason, Epson and Lattice will mutually consult about the substitute form of the transaction contemplated herein.)

1.5 POSITION OF SMOS

Notwithstanding any provision herein to the contrary, Lattice, Epson and SMOS acknowledges that although this Agreement is executed by each of such three (3) parties, SMOS is a party hereto solely for the purpose to evidencing its role, as the intermediary through which, under the terms of the Purchase Agreement, the Products to be sold to Lattice by Epson will be sold, and to evidence SMOS'S agreement to such an arrangement. SMOS shall under no circumstances have any rights under this Agreement (it being understood, however, that this Article 1.5 shall not in any way affect the rights of SMOS under the Purchase Agreement). In particular, and without limiting the generality of the foregoing, SMOS shall have no rights under Article 14 of this Agreement (i.e., any reference to party or parties to this Agreement shall be deemed to be only to Epson and Lattice unless

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

specifically prescribed therein), and Epson and Lattice may amend this Agreement in any respect. Epson agrees to cause SMOS to comply with all of the terms of this Agreement and the Purchase Agreement. Any material breach of the Purchase Agreement shall constitute a material breach to this Agreement for the purpose of Article 14.4 of this Agreement.

2 DEFINITIONS

2.1 "APP" will mean the advance production payment of Ten Billion Four Hundred and Sixty Nine Million and Seven Hundred Thousand Japanese Yen (JPY10,469,700,000) to be made by Lattice to Epson in the manner described in Article 4. If the parties agree, in accordance with Article 4.4, on additional APP, the definition of "APP" hereof shall be interpreted to include such additional APP.

2.2 "EQUIPMENT" will mean the semiconductor fabrication equipment that Epson will install in the New Facility for purposes of fabricating New Facility Wafers.

2.3 "EXISTING AGREEMENTS" will mean those contracts for the development, fabrication, testing and/or sale of semiconductor devices between Epson and Lattice in effect as of the date of this Agreement.

2.4 "FREE WAFERS" will have the meaning ascribed to it in Article 8.

2.5 "FUJIMI FACILITY" will have the meaning ascribed to it in Article 1.1.

2.6 "NEW FACILITY" will mean the (*) CMOS process line constructed at the Site using the Equipment.

2.7 "NEW FACILITY WAFERS" will mean the semiconductor wafers to be fabricated by Epson for Lattice at the New Facility.

2.8 "PRICE" will have the meaning ascribed to it in Article 10.1.

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

2.9 "PRODUCTS" will mean those specific types of New Facility Wafers fabricated using the same masks and the same process flow and identified by the same series or product name or number. The Products will be ordered, fabricated, delivered and sold pursuant to the terms and conditions of Purchase Agreement(s). The Products which the parties desire to fabricate at the New Facility will be agreed by and between Epson and Lattice, referring to the Process Road Map for Lattice attached hereto as Exhibit B, which may be reviewed and amended from time to time by mutual agreement of the parties. The parties acknowledge however, that the final determination of what Products will be fabricated may depend on the results of joint development and product qualification.

2.10 "PURCHASE AGREEMENT(S)" will mean the agreements by and between SMOS and Lattice pursuant to which SMOS agrees to sell and Lattice agrees to purchase the Products. It is the intention of the parties to execute the Purchase Agreement, the terms of which shall be negotiated and agreed between SMOS and Lattice, after the execution of this Agreement.

2.11 "PROJECTED COMPLETION SCHEDULE" will have the meaning ascribed to it in Article 3.1.2.

2.12 "PURCHASE COMMITMENT" will have the meaning ascribed to it in Article 7.1 and Exhibit D attached hereto.

2.13 "SAKATA FACILITY" will have the meaning ascribed to it in Article 1.1.

2.14 "SITE" will mean that portion of the Sakata Facility where the New Facility will be constructed.

2.15 "SUPPLY COMMITMENT" will have the meaning ascribed to it in Article 6.1 and Exhibit D.

2.16 (*) Process will mean the (*), CMOS process owned, licensed or developed by Epson which will be used at the New Facility. The (*) Process will include (a) all process flow, process steps, process conditions, and modifications thereto, used to

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

manufacture semiconductor wafers at the New Facility as well as (b) all methods, formulae, procedures, technology and know-how associated with such process steps and process conditions. The (*) Process will not include any methods, formulae, procedures, technology or know-how licensed or received from Lattice under this Agreement, the Existing Agreements or other agreements executed between the parties in the future unless otherwise agreed in writing. If the parties find it necessary or convenient to document process flow for any Product, such documentation will be signed by the parties and attached to the appropriate Purchase Agreement as an exhibit.

2.17 "SUBSIDIARY" will mean any corporation, partnership, joint venture or other legal entity which agrees in writing to be bound by the terms and conditions of this Agreement and more than fifty percent (50%) of whose ownership rights are controlled directly or indirectly by Epson or Lattice, as the case may be, but only so long as such control exists.

3 CONSTRUCTION AND REPRESENTATION

3.1 CONSTRUCTION OF THE NEW FACILITY

3.1.1 LOCATION AND COSTS

Epson hereby agrees, subject to its receipt of the full amount of the APP as provided in Article 4.1 to construct the New Facility at the Site and to install the Equipment therein.

3.1.2 COMPLETION SCHEDULE

The projected completion schedule for the construction of the New Facility (the "Projected Completion Schedule") is set forth in Exhibit A attached hereto. In the event Epson has reason to believe that any item in the Projected Completion Schedule designated as a "Construction Milestone" will be delayed by more than thirty (30) calendar days, Epson will promptly notify Lattice in writing and (a) explain the reason for the delay, (b) describe the estimated amount of time that construction will be delayed and (c)

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

describe the action that Epson will take to minimize the delay.

3.1.3 BUSINESS INTERRUPTION INSURANCE

Epson will use its best efforts to obtain business interruption insurance coverage for the New Facility once the construction of the New Facility is complete. The insurance will cover at least such risks as are usually insured against by companies engaged in the manufacture of semiconductor devices in Japan. Epson will maintain such business interruption insurance coverage during the term of this Agreement. Epson will furnish to Lattice, upon written request, full information concerning the business interruption insurance coverage.

3.1.4 FIRST SHIPMENT DELAY

In the event that the first mass production of the first Product is expected to be delayed beyond the process road map described in the latest version of Exhibit B, firstly, the shipment of such Product shall be made by utilizing existing facilities in the Sakata Facility subject to successful completion of the relevant process at such existing facility. Such alternative shipment shall not be applied for off-setting the APP. Epson shall provide regular action plans for the cure of the delay, and make monthly progress reports to Lattice. If no cure is achievable by the beginning of (*), and if the delay is not caused by Lattice, then Epson shall, in addition to the Free Wafers as prescribed in Article 8 hereof, provide additional free wafers (*).

3.1.5 DESIGN REQUIREMENTS

Epson acknowledges that Lattice may require certain safety and security requirements for semiconductor fabrication facilities, and Epson agrees to work with Lattice to incorporate such requirements into the design of the New Facility to the extent reasonably requested by Lattice and commercially feasible.

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

3.2 REPRESENTATIONS OF EPSON

In order to induce Lattice to enter into this Agreement and to make the APP hereunder, Epson hereby represents and warrants that:

3.2.1 CORPORATE STATUS

Epson (a) is duly organized, validly existing and in good standing under the laws of the jurisdiction of its incorporation, (b) has the corporate power to own or lease its assets and to transact the business in which it is currently engaged and (c) is in compliance with all requirements of law except to the extent that the failure to comply therewith will not materially affect the ability of Epson to perform its obligations under this Agreement.

3.2.2 CORPORATE AUTHORITY

(a) Epson has the corporate power, authority and legal right to execute, deliver and perform this Agreement and has taken as of the date hereof all necessary corporate action to execute this Agreement, (b) the person executing this Agreement has actual authority to do so on behalf of Epson and (c) there are no outstanding assignments, grants, licenses, encumbrances, obligations or agreements, either written, oral or implied, that prohibit execution of this Agreement.

3.2.3 OWNERSHIP OF THE SITE

Epson has such right, title and interest in and to the Site and the structures located thereon as is required to permit the operation of the Site as currently conducted and contemplated to be conducted under this Agreement.

3.2.4 NO MATERIAL LITIGATION

No litigation, investigation or administrative proceeding is presently pending, or to the knowledge of Epson, threatened against Epson which, if adversely determined, would materially affect Epson's ability to carry out the terms and conditions of this Agreement. If such material litigation, investigation or administrative proceeding is commenced against Epson, Epson shall notify Lattice thereof within

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

thirty (30) days of the commencement.

3.3 REPRESENTATION OF SMOS

In order to induce Lattice to enter into this Agreement and to make the APP hereunder, SMOS hereby represents and warrants that:

3.3.1 CORPORATE STATUS

SMOS (a) is duly organized, validly existing and in good standing under the laws of the jurisdiction of its incorporation, (b) has the corporate power to own or lease its assets and to transact the business in which it is currently engaged and (c) is in compliance with all requirements of law except to the extent that the failure to comply therewith will not materially affect the ability of SMOS to perform its obligations under this Agreement.

3.3.2 CORPORATE AUTHORITY

(a) SMOS has the corporate power, authority and legal right to execute, deliver and perform this Agreement and has taken as of the date hereof all necessary corporate action to execute this Agreement, (b) the person executing this Agreement has actual authority to do so on behalf of SMOS and (c) there are no outstanding assignments, grants, licenses, encumbrances, obligations or agreements, either written, oral or implied, that prohibit execution of this Agreement.

3.3.3 NO MATERIAL LITIGATION

No litigation, investigation or administrative proceeding is presently pending, or to the knowledge of SMOS, threatened against SMOS which, if adversely determined, would materially affect SMOS's ability to carry out the terms and conditions of this Agreement. If such material litigation, investigation or administrative proceeding is commenced against SMOS, SMOS shall notify Lattice thereof within thirty (30) days of the commencement.

3.4 REPRESENTATIONS OF LATTICE

In order to induce Epson to enter into this Agreement and to make the Supply Commitment, Lattice hereby represents and warrants

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

that:

3.4.1 CORPORATE STATUS
Lattice is duly organized, validly existing and in good standing under the laws of the jurisdiction of its incorporation, (b) has the corporate power to own or lease its assets and to transact the business in which it is currently engaged and (c) is in compliance with all requirements of law except to the extent that the failure to comply therewith will not materially affect the ability of Lattice to perform its obligations under this Agreement.

3.4.2 CORPORATE AUTHORITY
(a) Lattice has the corporate power, authority and legal right to execute, deliver and perform this Agreement and has taken as of the date hereof all necessary corporate action to execute this Agreement, (b) the person executing this Agreement has actual authority to do so on behalf of Lattice and (c) there are no outstanding assignments, grants, licenses, encumbrances, obligations or agreements, either written, oral or implied, that prohibit execution of this Agreement.

3.4.3 NO MATERIAL LITIGATION
No litigation, investigation or administrative proceeding is presently pending, or to the knowledge of Lattice, threatened against Lattice which, if adversely determined, would materially affect Lattice's ability to carry out the terms and conditions of this Agreement. If such material litigation, investigation or administrative proceeding is commenced against Lattice, Lattice shall notify Epson thereof within thirty (30) days of the commencement.

4 APP

4.1 APP
Lattice shall pay to Epson an amount equal to Ten Billion, Four Hundred sixty nine Million and Seven Hundred Thousand Japanese Yen (JPY10,469,700,000) ("APP"), which APP will be credited against certain future purchases by Lattice of New Facility

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

Wafers as provided in Article 5. Lattice will pay the whole amount of APP in accordance with the payment schedule described in Exhibit C hereof.

4.2 PAYMENT METHOD
All payments made by Lattice to Epson will be in immediately available funds and will be made by wire transfer in Japanese Yen to the following bank account of Epson at:

(*)
(*)
For the Account of Seiko Epson Corporation.

4.3 NON-REFUND OF APP
The APP will not be refundable except as provided in Articles 6.4.1 or 14.8.

4.4 ADDITIONAL APP
Epson acknowledges that Lattice may wish to pay to Epson additional APP of Sixty Million U.S. Dollars (US$60,000,000), to be converted to, and paid in Japanese Yen using U.S. dollar/Japanese Yen exchange rate prevailing in Tokyo, as published in Nihon Keizai Shinbun (Nikkei Newspaper), as at the end of a month immediately preceding the month during which the parties execute an amendment to this Agreement to effectuate such additional APP. Lattice will notify Epson by (*), whether or not it wishes to pay such additional APP. If Lattice so wishes to pay to Epson additional APP, Lattice's additional APP shall be deemed to be a part of the APP for all purposes hereunder, including but not limited to the same Price, procedure to offset from the additional APP, and Free Wafers. The specific terms for such additional APP, including payment terms, term of this Agreement and the additional Supply/Purchase Commitment shall be determined and added as an addendum to this Agreement within ninety (90) days of Lattice's first notification stated above.

5 CREDIT OF APP

5.1 CREDIT OF APP
The Purchase price of all New Facility Wafers purchased by

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

Lattice under the Purchase Agreement will be credited against the amount of the APP until the aggregate Japanese Yen value of all New Facility Wafers (excluding the Free Wafers) purchased and received by Lattice, calculated pursuant to Article 5.2, equals or exceeds the amount of the APP. The criteria and time required for wafer acceptance by Lattice will be described in the Purchase Agreement.

5.2 CALCULATION OF AGGREGATE CREDIT VALUE

The amount of APP will be offset and reduced on Japanese Yen to Japanese Yen basis, at the end of each calendar month of this Agreement, by an amount equal to the Price for the New Facility Wafers multiplied by the total number of New Facility Wafers (excluding the Free Wafers) shipped to Lattice pursuant to the Purchase Agreement during the calendar month, with adjustment of the increase pursuant to the methods provided in the Purchase Agreement, however under no circumstances shall the APP balance be increased, except as provided for in Article 14.8 of this Agreement. Further, any wafer provided to Lattice under Article 6.4.1 from alternative facility, besides the New Facility, shall not be used to offset the APP.

5.3 INVOICES

Epson will cause SMOS to provide Lattice with invoices under the Purchase Agreement which, for the purpose of APP application, specify the purchase price of the New Facility Wafers. Also, SMOS shall provide Lattice and Epson with the monthly report describing, among others, the outstanding balance of the APP (after the application of all prior offsets, reductions and credits) as of the commencement of the month subject to the invoices, the number of New Facility Wafers shipped to Lattice during that calendar month and the applied Price, and the outstanding balance of the APP as of the end of such calendar month. Such report shall be signed by the respective responsible person at Epson, SMOS and Lattice, provided that Lattice shall not be required to sign any such report unless it is satisfied with the accuracy and completeness thereof. Lattice may, for its signature, review all invoices and reports for inaccuracies and if any such inaccuracies are found and confirmed by Epson and

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

SMOS, Lattice may request to make corrections to these invoices and reports.

5.4 OBLIGATION AFTER COMPLETION OF OFF-SETTING THE APP

Lattice will be required to pay for all New Facility Wafers in accordance with the Purchase Agreements once the Advance Payment has been fully offset and reduced. Lattice will make the payments to Epson in Japanese Yen based on the Price. Further, Epson will be required to fulfill the Supply Commitment and Lattice will be required to fulfill the Purchase Commitment until Lattice has purchased (*) New Facility Wafers. After Lattice has purchased this fixed volume of the New Facility Wafers, during the effective period of this Agreement, Epson and Lattice will continue to make efforts to supply and purchase at the rate to be mutually agreed under fair and competitive prices to be determined between the parties.

6 SUPPLY COMMITMENT

6.1 CONTENTS OF SUPPLY COMMITMENT

It is the intent of Lattice to purchase and Epson to supply New Facility Wafers until a total (*) New Facility Wafers have been supplied to Lattice by Epson through SMOS and received and accepted by Lattice ("Supply Commitment"). The Supply Commitment and the supply schedule thereof are set forth in Exhibit D. The Supply Commitment herein shall remain in effect until Lattice has received and accepted a total of (*) New Facility Wafers (exclusive of the Free Wafers) through SMOS from Epson under this Agreement. Dealing of New Facility Wafers rejected by Lattice for any reason shall be as described in the Purchase Agreement. The Supply Commitment for a particular month may be modified as specifically set forth in this Agreement, but under no circumstances shall the aggregate Supply Commitment of (*) New Facility Wafers be reduced.

6.2 PURCHASE AGREEMENTS

The Supply Commitment will apply to Products covered by the Purchase Agreements. The parties anticipate that such Purchase Agreements will apply to Products distributed by Lattice which require fabrication using the (*) Process.

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

6.3 EXCESS CAPACITY

Epson will use its best efforts to provide Lattice, through SMOS, with excess capacity of the New Facility if Lattice requires so in the manner specified below. In this case, APP shall be applied to Lattice's orders of New Facility Wafers in excess of the Supply Commitment of the month. Also, the Free Wafers prescribed in Article 8 shall be provided for such excess volume of the New Facility Wafers. First, in the event that Lattice desires to purchase New Facility Wafers in excess of the Purchase Commitment, Lattice will specify in writing the amount of capacity required, the Product(s) it desires to purchase and the date from which such capacity is required, and notify Epson of it through SMOS.

Second, Epson will then determine how much capacity is available and notify Lattice of its determination through SMOS. Epson will give Lattice priority over third parties for excess capacity of the New Facility except to the extent that Epson is already obligated to provide such third parties with capacity.

Third, the parties will then mutually agree upon a preliminary excess capacity allocation. Any excess capacity allocated under this Article 6.3 will be applied to the Supply Commitment and to the Purchase Commitment.

In order to provide Lattice with first priority for unused capacity using the specific process for Lattice, Epson agrees to give Lattice monthly written notice of any unused capacity using the specific process for Lattice for the next (*), and to provide Lattice with the first right to reserve such unused capacity for any New Facility Wafers which Lattice desires to purchase in excess of the Purchase Commitment. Lattice will have a reasonable time to elect to reserve such excess capacity. The parties acknowledge that "specific process for Lattice" above refers to Lattice's (*) process, and that Epson's capacity plan at the time of executing this Agreement shows that approximately (*) of total production capacity of the New Facility will be for (*) process, subject to change by then-current production plan of Epson. Epson will notify Lattice if the capacity set aside for (*) process will change by (*) of the total

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

capacity.

6.4 FAILURE TO MEET SUPPLY COMMITMENT

6.4.1 FAILURE DUE TO EPSON

In the event that (a) Epson fails to fulfill the Supply Commitment by the end of any month during the term of this Agreement or (b) Epson has reason to believe that it will be unable to fabricate the Supply Commitment by the end of such month, then Epson will take the following measures:

First, Epson will promptly notify Lattice in writing and describe the nature of the difficulty.

Second, Epson will use its best efforts to remedy the difficulty in an expeditious manner by the end of the second full month following the month in which Epson is unable to meet the Supply Commitment (in other words, the third month including the month in which the difficulty occurs).

Third, Epson will use its best efforts to make available during the above referenced three (3) month period sufficient capacity at the Sakata Facility, the Fujimi Facility or Epson's other qualified facility to cover the deficiency between the Supply Commitment and the actual capacity subject to completion of product qualification. The parties acknowledge, however, that Epson cannot guarantee the use of such alternative capacity.

Fourth, if Epson's inability to fulfill the Supply Commitment is due to force majeure prescribed in Article 15.14, Epson will use its best efforts to make available alternative capacity at the Sakata Facility and/or Fujimi Facility. The parties acknowledge, however, that Epson cannot guarantee the use of existing capacity at the Sakata Facility or Fujimi Facility.

Notwithstanding any provision of this Agreement to the contrary, in the event that Epson fails to fulfill the Supply Commitment (including any failure by virtue of the

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

action or inaction of SMOS or any of the deficiency within the three (3) month period referenced above), such failure shall constitute a material breach of this Agreement and Epson, SMOS and Lattice shall discuss the relief of such breach prior to Lattice's termination of this Agreement based on the right permitted in Article 14.4 (which termination may be made without the notice and cure period contemplated by Article 14.4).

6.4.2 FAILURE DUE TO LATTICE

Notwithstanding anything contained in Article 6.4.1 to the contrary, in the event that Epson fails to fulfill the Supply Commitment in any month due to (a) design defects in Products caused by Lattice, (b) design changes requested by Lattice, (c) process flow changes requested by Lattice or (d) any other reason caused by Lattice, Epson will only be required to make reasonable efforts to fulfill the Supply Commitment in such month. Provisions concerning Lattice's failure to fulfill its Purchase Commitment are set forth in Article 7.2.

6.4.3 FAILURE DUE TO BOTH PARTIES

Notwithstanding anything contained in Article 6.4.1, 6.4.2 or 7.1 to the contrary, in the event that Epson fails to fulfill the Supply Commitment and Lattice fails to fulfill the Purchase Commitment due to difficulties caused jointly by Lattice and Epson, the parties will mutually agree in writing upon a fair and equitable solution.

6.4.4 FAILURE DUE TO CATASTROPHE

In the event that any fire, flood, earthquake, explosion or any other catastrophe prevents Epson from fabricating New Facility Wafers for Lattice, (a) Epson will immediately implement the measures required by Article 6.4.1, (b) Epson

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

will permit Lattice to inspect the New Facility, and (c) the parties will begin good faith negotiations to agree on a corrective action plan.

7 PURCHASE COMMITMENT

7.1 CONTENT OF PURCHASE COMMITMENT

Lattice intends to purchase each month the number of New Facility Wafers (the "Purchase Commitment") equal to the Supply Commitment until (*) wafers have been purchased. Lattice will not be required to fulfill the Purchase Commitment in the event that Epson fails to fulfill the Supply Commitment in the manner specified in Article 6.4.1. Instead, subject to the terms of the Purchase Agreement, Lattice will be required to purchase those New Facility Wafers that Epson is able to fabricate up to the Purchase Commitment for each month. Lattice will not be required to fulfill the Purchase Commitment in the event of difficulties caused by both Epson and Lattice. Instead, the parties will mutually agree in writing upon a fair and equitable solution.

7.2 SALE OF UNUSED CAPACITY

In the event that Lattice is unable to fulfill the Purchase Commitment in any month for reasons not due to Epson, Epson will use its best efforts to sell unused capacity to other customers, or to allocate unused capacity for the fabrication of Epson products during such month. Further, the Supply Commitment for such month will be reduced to the same extent that Lattice is unable to fulfill the Purchase Commitment. When Lattice desires to increase its monthly purchases after Epson has sold or otherwise allocated unused capacity, then Epson will use its best efforts to increase capacity for Lattice to the Supply Commitment in an expeditious manner. The parties will mutually agree upon the specific rate at which Epson will be required to ramp up capacity to the Supply Commitment.

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

8 FREE WAFERS

As a consideration for Lattice's payment of APP, Epson shall provide Lattice with (*) free wafers of a Product ("Free Wafers") through SMOS pursuant to the Purchase Agreement for every (*) New Facility Wafers ordered by Lattice after the execution of this Agreement (*) until Epson has supplied (*) New Facility Wafers (excluding the Free Wafers).

9 FABRICATION, PURCHASE AND SALE

9.1 GENERAL TERMS AND CONDITIONS

The terms and conditions for the prototype wafer fabrication, wafer fabrication, order and acceptance, shipping, insurance and warranty for the Products will be set forth in the Purchase Agreements. The parties have agreed to certain order and forecast systems as described in Exhibit F, which will be incorporated in the Purchase Agreement. The parties acknowledge that a best estimation and target of defect densities as at the date of this Agreement is set forth in Exhibit H attached hereto, which will be reviewed and amended from time to time by the parties hereto, and will be incorporated into all Purchase Agreements.

9.2 START OF PRODUCTION

Qualification testing for the Products will be conducted in the manner specified in the Purchase Agreement. Once any Product has been qualified, Epson will begin mass production of such Product in the manner specified by the Purchase Agreement.

9.3 TURN AROUND TIME

The parties acknowledge that the lead time for shipment of New Facility Wafers, defined as the time from Lattice's purchase order release until delivery of New Facility Wafers, known as "turn around time", is of the essence, and agree that the parties shall set annual target turn around time and make their joint efforts to achieve such target in accordance with Exhibit I.

10 WAFER PRICING AND PAYMENT

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

10.1 DETERMINATION OF PRICE

The general method for determining the price of Products ("Price") shall be as set forth in Exhibit E. Epson agrees that at any time the Prices to Lattice (*). The Price herein shall be applicable until Lattice has completed the purchase of (*) New Facility Wafers under the terms of this Agreement.

10.2 SHIPPING, INSURANCE, TAXES, DUTIES AND OTHER FEES

Epson will deliver the Products on a C.I.F., San Jose basis, and SMOS will deliver such Products to Lattice on an F.O.B., San Jose basis. Bearing of sales, use, excise, ad valorem, withholding or other taxes or duties that may be applicable to purchase of the Products by Lattice shall be prescribed in the Purchase Agreement.

10.3 PAYMENT

Other than through offset of the APP, Lattice will not be required to pay for any New Facility Wafers delivered under this Agreement or any Purchase Agreement until the APP has been fully offset and reduced. Once the APP is fully offset and reduced, Lattice will be required to pay Epson in the manner specified in the Purchase Agreement based on the Price until Lattice has completed the purchase of (*) New Facility Wafers under the terms of this Agreement.

11 TECHNICAL COOPERATION AND SUPPORT

The parties desire to engage in various types of joint development and technical cooperation activities required to fabricate Products and to effectuate the terms and conditions of this Agreement. The parties, including SMOS, will discuss such joint development possibilities, and will conclude appropriate agreement(s).

12 INTELLECTUAL PROPERTY RIGHTS

All intellectual property rights clauses relating to (*) Process and the Products will be set forth in the Purchase Agreement. Lattice agrees that any indemnity or warranty that Lattice expressly provides to Epson or SMOS under the Purchase Agreement will be fully

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

enforceable by Epson even though Epson has not executed the Purchase Agreement. Furthermore, Epson agrees that any indemnity or warranty that Epson or SMOS purports to provide to Lattice under the Purchase Agreement will be fully enforceable by Lattice even though Epson has not executed the Purchase Agreement. In the event that any claims for intellectual property rights infringements described in the Purchase Agreement prevent the parties from fulfilling the Supply Commitment and the Purchase Commitment, the parties will mutually agree on a fair and equitable solution without affecting in any way the right of either party to terminate this Agreement for cause pursuant to Article 14.4 as a consequence of failure of the other party to fulfill this Agreement and the Purchase Agreement as the case may be. The parties acknowledge that the covenants contained in this Article 12 are an essential part of this Agreement.

13 CONFIDENTIAL INFORMATION

13.1 DEFINITIONS

"Confidential Information" means technical information, specifications, data, drawings, designs or know-how, prices, order volumes, forecasts, financial information, strategic plans, and other important business information disclosed between Epson and Lattice, or SMOS and Lattice in connection with this Agreement. Confidential Information includes information or material that is expressly covered by confidentiality provisions of Existing Agreements or the Purchase Agreement, it being understood that such provisions will apply.

13.2 MARKING

If Confidential Information is provided in a tangible form, it will be marked as confidential or proprietary. If Confidential Information is provided orally, it will be treated as confidential and proprietary if it is treated as confidential or proprietary at the time of disclosure by the disclosing party and described as such in a writing provided to the other party within thirty (30) days of the oral disclosure, which writing will be marked as confidential or proprietary. Material that is not marked as required by this Article 13.2 will not be deemed Confidential Information.

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

13.3 RESTRICTIONS ON USE

During the term of this Agreement and for a period of (*) years following disclosure of any Confidential Information, the receiving party will: (a) hold the Confidential Information in confidence using the same degree of care that it normally exercises to protect its own proprietary information but no less than a reasonable degree of care, (b) restrict disclosure and use of Confidential Information solely to those employees (including any contract employees or consultants) of such party on a need-to-know basis, and not disclose it to other employees or parties, and (c) restrict the number of copies of Confidential Information to the number required to carry out its obligations under this Agreement.

13.4 EXCEPTIONS TO CONFIDENTIALITY OBLIGATIONS

Neither party will use or disclose the other party's Confidential Information except as permitted by this Agreement. The receiving party, however, will have no obligations concerning the disclosing party's Confidential Information if the disclosing party's Confidential Information:

a) is made public before the disclosing party discloses it to the receiving party;

b) is made public after the disclosing party discloses it to the receiving party (unless its publication is a breach of this Agreement or any other agreement between Epson and Lattice);

c) is rightfully in the possession of the receiving party before the disclosing party discloses it to the receiving party;

d) is independently developed by the receiving party without the use of the Confidential Information, if such independent development is supported by documentary evidence; or

e) is rightfully obtained by the receiving party from a third party who is lawfully in possession of the information and not in violation of any contractual, legal or fiduciary obligation to the disclosing party with respect to the information.

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

Each party may disclose any Confidential Information to the extent that such party has been advised by counsel that such disclosure is necessary to comply with laws or regulations provided that such party shall give the other party reasonable advance notice of such proposed disclosure, shall use its best efforts to secure confidential treatment of such Confidential Information, and shall advise the other party in writing of the manner of the disclosure.

13.5 RETURN OF CONFIDENTIAL INFORMATION

Upon termination of this Agreement, a party who has received Confidential Information from the other party pursuant to this Agreement will return, within fourteen (14) days of the disclosing party's request for return, all Confidential Information that was obtained or learned by the receiving party from the disclosing party, or delivered to the receiving party, together with all copies, excerpts and translations thereof.

14 TERM AND TERMINATION OF AGREEMENT

14.1 TERM

The term of this Agreement will extend from the date first written above until the latest of (a) Epson's completion of the supply of, and receipt and acceptance by Lattice of, (*) New Facility Wafers in total (*), (b) the completion of off-setting APP, or (c) (*), unless terminated earlier pursuant to Article 14.2, 14.3 or 14.4. After the expiration of this Agreement, Epson and Lattice shall continue to make efforts to supply and purchase a certain volume of wafers per month under fair and competitive prices to be determined between the parties.

14.2 TERMINATION

Either party may terminate or suspend this Agreement immediately and without liability (except for the terms provided in Articles 14.5 and 14.6) upon written notice to the other party if any one of the following events occurs;:

a) the other party files a voluntary petition in bankruptcy or otherwise seeks protection under any law for the

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

protection of debtors;

b) a proceeding is instituted against the other party under any provision of any bankruptcy laws which is not dismissed within ninety (90) days;

c) the other party is adjudged bankrupt;

d) a court assumes jurisdiction of all or a substantial portion of the assets of the other party under a reorganization law;

e) a trustee or receiver is appointed by a court for all or a substantial portion of the assets of the other party;

f) the other party becomes insolvent, ceases or suspends all or substantially all of its business;

g) the other party makes an assignment of the majority of its assets for the benefit of creditors; or

h) the other party fails to pay all or a substantial portion of its debts as they become due or admits in writing its inability to pay all or a substantial portion of its debts as they become due; or

i) force majeure, as prescribed in Article 15.14, becomes in effect and performance of the obligations under this Agreement will not be restored within six (6) months after such force majeure's occurrence.

14.3 TERMINATION DUE TO ACQUISITION OR SALE OF ASSETS

In the event that a direct competitor or one party acquires, through merger, consolidation, acquisition or otherwise, an interest in excess of fifty percent (50%) of the voting securities or assets of the other party, or such other party transfers all or substantially all of its business to which this Agreement relates to a direct competitor of such party, the non-aquiring or non-transferring party will be permitted, upon written notice to the other party, to require that the

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

transactions contemplated by this Agreement and the Purchase Agreements be phased out and terminated at a rate not to exceed, (*) of the business existing at the time of the acquistion or transfer according to the following schedule:

A	B
(*)	(*)
(*)	(*)
(*)	(*)
(*)	(*)

A- Time elapsed since acquisition or transfer of assets
B- Level to which business may be phased out measured as a percentage of business existing at the time of the acquisition or transfer of assets

Alternatively, the business may be phased out and terminated under this Article 14.3 in a manner otherwise agreed upon in writing by the parties.

14.4 TERMINATION FOR CAUSE

If either party fails to perform or violates any material obligation of this Agreement, then, sixty (60) days after providing written notice to the breaching party specifying the default (the "Default Notice"), the non-breaching party may terminate this Agreement, without liability, unless:

a) the breach specified in the Default Notice has been cured within the sixty (60) day period; or

b) the default reasonably required more than sixty (60) days to correct, and the defaulting party has begun substantial corrective action to remedy the default within such sixty (60) day period and diligently pursues such action, in which event, the non-breaching party may not terminate or suspend this Agreement unless one hundred twenty (120) days has expired from the date of the Default Notice without such corrective action being

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

completed and the default remedied.

14.5 TERMINATION BY EPSON

In the event that Epson terminates this Agreement pursuant to this Article 14, then, unless otherwise agreed upon in writing, Epson may offset and reduce the APP to cover all direct material and labor costs for work in process rendered unusable by termination and will ship such work in process to Lattice, at Lattice's expense, if requested to do so. Upon such termination, Epson shall refund the remaining portion of APP (reduced by the amount of any such offset and reduction to cover direct material and labor costs for work in process rendered unusable by the termination) no later than thirty (30) business days after the date of termination.

14.6 TERMINATION BY LATTICE

In the event that Lattice terminates this Agreement pursuant to this Article 14, then, unless otherwise agreed in writing, Lattice may either (a) request that Epson refund the remaining portion of APP (from which Epson may offset and reduce to cover all direct material and labor costs for work in process rendered unusable by the termination) and then Epson will refund the remaining portion of APP (as so offset and reduced) or (b) request Epson to complete all work in process and ship them under normal terms and conditions, and then Epson will refund the remaining portion of APP (excluding, without limitation, the costs and expenses which have arisen in connection with completing all work in process and shipping thereof), with in either such case such refund to be paid upon the earlier of:

(a) receipt of sufficient funding from a financial institition or other source for purposes of paying the refund, or
(b) thirty (30) days from the date of termination.

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

14.7 RETENTION OF RIGHTS AFTER TERMINATION

Notwithstanding anything contained in this Article 14 to the contrary, in the event that either party is entitled to terminate this Agreement pursuant to Articles 14.2 (f), (g) or (h) or either party is subject to a bankruptcy, reorganization or liquidation proceeding, the other party may elect to (a) retain its rights in this Agreement existing immediately prior to termination pursuant to Article 14.2 (f), (g) or (h) or the initiation of such proceeding or (b) treat any such proceeding or attempted rejection of this Agreement by a bankruptcy trustee as an event of termination. Unless otherwise provided, in the event of such termination, Epson shall refund the remaining portion of the APP in accordance with article 14.5 or 14.6 as applicable.

14.8 RECONCILIATION

In the event of termination that results in a refund of the APP balance pursuant to Article 14 (or would result in such a refund if the APP balance were increased by the net return material account balances, if any, under the Purchase Agreement), Epson shall cause SMOS to bring current the APP, Free Wafers and return material account balances as provided for in the Purchase Agreement in order to reconcile the account with Lattice, and to refund the mutually agreed net amount.

14.9 SURVIVAL OF OBLIGATIONS

The following Articles will survive any expiration, termination or cancellation of this Agreement and the parties will continue to be bound by the terms and conditions thereof: 12, 13, 14, and 15.

15 MISCELLANEOUS

15.1 ORDER OF PRECEDENCE

In the event of any conflicts between this Agreement and any Purchase Agreement, any purchase orders, acceptances, correspondence, memoranda, listing sheets or other documents forming part of an order for the Products placed by Lattice and accepted by SMOS (or Epson), priority will be given first to this Agreement, second to the Purchase Agreements, third to SMOS's or

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

Epson's acceptance, fourth to Lattice's order and then to any other documents. In no event, however, will either party's standard terms and conditions be applicable to the transactions between the Lattice and SMOS (or Epson), unless expressly accepted in writing by the other party.

15.2 GOVERNING LAW

This Agreement shall be governed by and construed in accordance with the laws of California, U.S.A. without reference to conflict of law principles.

15.3 DISPUTE RESOLUTION

15.3.1 MEETING OF EXECUTIVES

In the event that any dispute or disagreement between the parties as to any provision of this Agreement arises, prior to taking any other action, the matter will be referred to responsible executives of the parties for consideration and resolution. Any party may commence such proceedings by delivering a written request to the other party for a meeting of such responsible executives. The other party will be required to set a date for the meeting to be held within thirty (30) days after receipt of such request and the parties agree to exercise their best efforts to settle the matter amicably.

15.3.2 LOCATION OF MEETING

In the event that Epson initiates the proceedings described in Article 15.3.1, the first meeting will be held Hillsboro, Oregon and all subsequent meetings will alternate between Tokyo, Japan, and Hillsboro, Oregon. In the event that Lattice initiates the proceedings described in Article 15.3.1, the first meeting will be held in Tokyo, Japan and all subsequent meetings will alternate between Hillsboro, Oregon and Tokyo, Japan.

15.3.3 DEMAND FOR ARBITRATION

Any dispute relating to and/or arising out of this Agreement will be decided exclusively by binding arbitration under procedures which ensure efficient and speedy resolution.

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

Such an arbitration may be commenced by either party involved in the dispute (i) after the expiration of a sixty (60) day period following the written request to resolve the dispute, and/or (ii) at such earlier time as any party involved repudiates and/or refuses to continue with its obligations to negotiate in good faith. The arbitration hearing will be conducted in the State of Hawaii, and will be in the English language (with translators and interpretations as reasonable for the presentation of evidence and/or conduct of the arbitration). Notwithstanding anything to the contrary, any party may apply to any court of competent jurisdiction for interim injunctive relief as may be allowed under applicable law with respect to irreparable harm which cannot be avoided and/or compensated by such arbitration proceedings, without breach of this Article 15.3.3 and without any abridgement of the powers of the arbitrators.

The arbitration will be conducted under the Rules of the Asia Pacific Arbitration Center. Notwithstanding anything to the contrary, (i) the arbitrators will have the power to order discovery to the extent they find such discovery necessary to achieve a fair and equitable result and (ii) the arbitrators shall require pre-hearing exchange of documentary evidence to be relied upon by each of the respective parties in their respective cases in chief, and pre-hearing exchange of briefs, witness lists,and summaries of expected testimony.

The arbitrators will make their decision in writing.

15.3.4 ARBITRATORS
The arbitration will be conducted by three (3) arbitrators. No person with a beneficial interest in the dispute under arbitration may be an arbitrator. The parties will make reasonable efforts to select arbitrators with experience in the field of computers and law.

15.3.5 BINDING EFFECT
The decision or award rendered or made in connection with

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

such arbitration will be binding upon the parties and judgment thereon may be entered in any court having jurisdiction and/or application may be made to such court for enforcement of such decision or award. However, the arbitrators will not have the authority to create any licenses. They will only be permitted to enforce licenses which the parties have otherwise agreed to in the Agreement or the Existing Agreements.

15.3.6 EXPENSES

The expenses of the arbitrators will be shared equally by the parties; each party will otherwise be responsible for the costs and attorney's fees incurred by it; provided, however, if the arbitrators appointed in Article 15.3.4 find that the position of the non-prevailing party or parties in such arbitration was without substantial justification or was frivolous, the arbitrators may assess all of the costs and expenses together with reasonable attorney's fees against the non-prevailing party or parties.

15.4 CONSEQUENTIAL DAMAGES

IN NO EVENT WILL EITHER PARTY BE LIABLE TO THE OTHER PARTY FOR ANY INDIRECT, SPECIAL, CONSEQUENTIAL OR INCIDENTAL DAMAGES (INCLUDING LOST PROFITS) WHETHER BASED ON WARRANTY, CONTRACT, TORT OR ANY OTHER LEGAL THEORY REGARDLESS OF WHETHER SUCH PARTY HAD ACTUAL OR CONSTRUCTIVE NOTICE OF SUCH DAMAGES; PROVIDED, HOWEVER, THIS LIMITATION WILL NOT APPLY IF THE DAMAGES OCCUR AS A RESULT OF GROSS NEGLIGENCE OR WILLFUL MISCONDUCT OF EITHER PARTY IN THE PERFORMANCE OF THEIR RESPONSIBILITIES UNDER THIS AGREEMENT.

15.5 ASSIGNMENT

Neither party will assign, transfer or otherwise dispose of this Agreement in whole or in part without the prior consent of the other party in writing, and such consent will not be unreasonably withheld. Except in the case set forth in Article 14.3, above, this Agreement may be assigned to any Subsidiary or to a successor who has acquired a majority of the business or assets of the assigning party.

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

15.6 PUBLIC ANNOUNCEMENTS

Neither party will publicly announce the execution or existence of this Agreement or disclose the terms and conditions of this Agreement without first submitting the text of such announcement to the other party and receiving the approval of the other party of such text, which approval, unless public disclosure is required by a court or a government agency, may be withheld for any reason. However, Lattice may disclose the existence and the terms of this Agreement in any document legitimately required to be filed with the Securities and Exchange Commission (and may file a copy of this Agreement required legitimately with such filing) or in accordance with generally accepted accounting procedures under the rules of the Securities and Exchange Commission or the National Association of Securities Dealers Automated Quotations stock market.

15.7 NOTICE AND COMMUNICATIONS

Any notices required or permitted to be given hereunder will be in English and be sent by (i) registered airmail or (ii) cable, facsimile or telex to be confirmed by registered airmail, addressed to:

To Epson:

281 Fujimi, Fujimi-machi, Suwa-gun
Nagano-ken 399-02, Japan
Attn: Nobuo Hashizume,
Director and Corporate General Manager
Semiconductor Operations Division
Tel: 81-266-61-1211
Fax: 81-266-61-1270

To SMOS:

150 River Oaks Parkway, San Jose, CA 95134-1951
U.S.A.
Attn: Tadakatsu Hayashi, President and CEO
Tel: 1-408-922-0200
Fax: 1-408-922-0238

To Lattice:

5555 N.E. Moore Ct., Hillsboro, Oregon,

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

97124-6421, U.S.A.
Attn: Cyrus Tsui
Chairman, President and Chief Executive Officer
Tel: 1-503-681-0118
Fax: 1-503-681-3077

Any such notice will be deemed given at the time of its receipt by the addressee.

15.8 RELATIONSHIP OF THE PARTIES

Epson and Lattice are independent contractors and neither of them will be nor represent themselves to be the legal agent, partner or employee of the other party for any purpose. Neither party will have the authority to make any warranty or representation on behalf of the other party nor to execute any contract or otherwise assume any obligation or responsibility in the name of or on behalf of the other party. In addition, neither party will be bound by, nor liable to, any third person for any act or any obligations or debt incurred by the other party, except to the extent specifically agreed to in writing by the parties.

15.9 WAIVER AND AMENDMENT

Failure by either party, at any time, to require performance by the other party or to claim a breach of any provision of this Agreement will not be construed as a waiver of any right accruing under this Agreement, nor will it affect any subsequent breach or the effectiveness of this Agreement or any part hereof, or prejudice either party with respect to any subsequent action. A waiver of any right accruing to either party pursuant to this Agreement will not be effective unless given in writing.

15.10 SEVERABILITY

In the event that any provision of this Agreement will be unlawful or otherwise unenforceable, such provision will be severed, and the entire agreement will not fail on account thereof, the balance continuing in full force and effect, and the parties will endeavor to replace the severed provision with a similar provision that is not unlawful or otherwise unenforceable.

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

15.11 RIGHTS AND REMEDIES CUMULATIVE
The rights and remedies provided herein will be cumulative and not exclusive of any other rights or remedies provided by law or otherwise.

15.12 HEADINGS
The Article headings in this Agreement are for convenience only and will not be considered a part of, or affect the interpretation of, any provision of this Agreement.

15.13 GOVERNING LANGUAGE
This Agreement and all communications pursuant to it will be in the English language. If there is any conflict between the English version and any translated version of this Agreement, the English version will govern.

15.14 FORCE MAJEURE
Except as otherwise expressly provided for herein, no party will be liable in any manner for failure or delay in fulfillment of all or part of this Agreement directly or indirectly owing to any causes or circumstances beyond its control, including, but not limited to, acts of God, governmental order or restrictions, war, war-like conditions, hostilities, sanctions, revolutions, riot, looting, strike, lockout, plague or other epidemics, fire and flood.

15.15 COUNTERPARTS
This Agreement may be executed in any number of counterparts, and all such counterparts will together constitute but one Agreement.

15.16 INTEGRATION
This Agreement sets forth the entire agreement and understanding between the parties as to its subject matter and supersedes all prior agreements, understandings and memoranda between the parties, except for the Existing Agreements. No amendments or supplements to this Agreement will be effective for any purpose except by a written agreement signed by the parties.

15.7 GOVERNMENT APPROVALS; EXPORT CONTROL LAWS
Epson will file all reports and notifications that may be

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

required to be filed with any agency of the Government of Japan in order to allow the performance of this agreement according to its terms. Lattice will file all reports and notifications that may be required to be filed with any agency of the Government of U.S.A. in order to allow the performance of this Agreement according to its terms. Neither party will transmit indirectly or directly any Products or technical information contained in the Confidential Information except in accordance with applicable Japanese and United States export control laws, regulations and procedures.

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

IN WITNESS WHEREOF, the parties have signed this Agreement as of the date first above written.

LATTICE SEMICONDUCTOR CORPORATION

By: /s/ CYRUS TSUI

Name: Cyrus Tsui
Title: Chairman, President and Chief Executive Officer

SEIKO EPSON CORPORATION

By: /s/ NOBUO HASHIZUME

Name: Nobuo Hashizume
Title: Director and Corporate General Manager
Semiconductor Operations Division

S MOS Systems, Inc.

By: /s/ TADAKATSU HAYASHI

Name: Tadakatsu Hayashi
Title: President and CEO

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

EXHIBIT A

"Projected Completion Schedule"

EXHIBIT B

"Process Road Map for Lattice"

EXHIBIT C

"Payment Schedule"

EXHIBIT D

"New Facility Production Capacity and Supply/Purchase Commitment"

EXHIBIT E

Price Determination Procedure"

"APP Offset Procedure"

"(*)"

EXHIBIT F

"Forecast System"

EXHIBIT G

"Epson's (*) Technology Road Map and (*) Process"

EXHIBIT H

"Defect Density Goal"

EXHIBIT I

"Turn Around Time"

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

EXHIBIT A
PROJECTED COMPLETION SCHEDULE
(*)

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

EXHIBIT B
PROCESS ROAD MAP FOR LATTICE
(*)

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

EXHIBIT C
PAYMENT SCHEDULE
(*)

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

EXHIBIT D
NEW FACILITY PRODUCTION CAPACITY PLAN
AND SUPPLY/PURCHASE COMMITMENT
(*)

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

EXHIBIT E
PRICE DETERMINATION PROCEDURE
(*)
APP OFFSET PROCEDURE
(*)
(*)
(*)

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

EXHIBIT F
FORECAST SYSTEM
(*)

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

EXHIBIT G
EPSON'S (*) TECHNOLOGY ROAD MAP AND (*) PROCESS
(*)

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

EXHIBIT H
DEFECT DENSITY GOAL
(*)

* Omitted and filed separately with the SEC pursuant to a confidential treatment request.

EXHIBIT I
TURN AROUND TIME
(*)

EXHIBIT 11.1

LATTICE SEMICONDUCTOR CORPORATION

COMPUTATION OF NET INCOME PER SHARE
(In thousands, except per share data)

	YEAR ENDED		
	MARCH 29, 1997	MARCH 30, 1996	APRIL 1, 1995
Net income	$45,005	$41,784	$26,966
Weighted average common stock and common stock equivalents:			
Common	22,460	20,327	18,627
Options and warrants	513	652	537
	22,973	20,979	19,164
Net income per share	$ 1.96	$ 1.99	$ 1.41

FINANCIAL HIGHLIGHTS

(IN THOUSANDS, EXCEPT PER SHARE DATA)	YEAR ENDED MARCH 29, 1997	MARCH 30, 1996	APRIL 1, 1995
Revenue	$204,089	$198,167	$144,083
Net income	$45,005	$41,784	$26,966
Net income per share	$1.96	$1.99	$1.41
Cash and short-term investments	$228,647	$215,170	$88,810
Total assets	$403,462	$342,935	$192,917
Stockholders' equity	$360,491	$298,768	$157,797

CORPORATE PROFILE

Lattice Semiconductor Corporation designs, develops and markets high performance programmable logic devices ("PLDs") and related development system software. Lattice is the inventor and world's leading supplier of in-system programmable ("ISP-TM-") logic devices. ISP devices have emerged as the next standard in the high-density PLD market. PLDs are standard semiconductor components that can be configured by the end customer as specific logic functions, enabling shorter design cycle times and reduced development costs. Lattice's end customers are primarily original equipment manufacturers ("OEMs") in the fields of communications, computing, computer peripherals, instrumentation, industrial controls and military systems. Nearly one-half of Lattice's revenue is derived from international sales, mainly in Europe and Asia. Lattice offers products that range in complexity from about 200 to 25,000 gates. Products are offered in 20 to 304 pin packages in a variety of speed, power and temperature grades.

MANAGEMENT'S DISCUSSION AND ANALYSIS OF FINANCIAL CONDITION AND RESULTS OF OPERATIONS

This report contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934. Actual results could differ materially from those projected in the forward-looking statements as a result of the factors set forth in the section entitled "Factors Affecting Future Results" and elsewhere in this report.

Lattice Semiconductor Corporation (the "Company"), founded in 1983 and based in Hillsboro, Oregon, designs, develops and markets high performance programmable logic devices ("PLDs") and related development system software. The Company is the inventor and world's leading supplier of in-system programmable ("ISP-TM-") logic devices. PLDs are standard semiconductor components that can be configured by the end customer as specific logic functions, enabling shorter design cycle times and reduced development costs. The Company's end customers are primarily original equipment manufacturers ("OEMs") in the fields of communications, computing, computer peripherals, instrumentation, industrial controls and military systems. Nearly one-half of the Company's revenue is derived from international sales, mainly in Europe and Asia.

RESULTS OF OPERATIONS

The following table sets forth, for the periods indicated, the percentage of revenue represented by selected items reflected in the Company's consolidated statement of operations.

	YEAR ENDED		
	MAR. 29, 1997	MAR. 30, 1996	APR. 1, 1995
Revenue	100%	100%	100%
Costs and expenses:			
Cost of products sold	41	41	41
Research and development	14	14	16
Selling, general and administrative	16	16	17
	71	71	74
Income from operations	29	29	26
Interest and other income (net)	4	3	2
Income before provision for income taxes	33	32	28
Provision for income taxes	11	11	9
Net income	22%	21%	19%

REVENUE Revenue was $204.1 million in fiscal 1997, an increase of 3% over fiscal 1996. Fiscal 1996 revenue of $198.2 million represented an increase of 38% from the $144.1 million recorded in fiscal 1995. The majority of the Company's revenue in fiscal 1997 was derived from the sale of products that address the high-density segment of the programmable logic market. The majority of the Company's revenue growth for the periods presented resulted from the sales of new products, primarily high-density products. Increases in the sales of the Company's high-density products have been significant and have grown consistently as a percentage of the Company's overall revenue for the fiscal periods presented.

Revenue from international sales was approximately 49%, 48% and 47% of total revenue for fiscal 1997, 1996 and 1995, respectively. The Company expects export sales to continue to represent a significant portion of revenue. See "Factors Affecting Future Results."

Overall average selling prices, while remaining relatively constant during the fiscal 1995 period, increased during fiscal 1996 and again during fiscal 1997. This was due primarily to a higher proportion of high-density products in the revenue mix. Although selling prices of mature products generally decline over time, this decline is at times offset by higher selling prices of new products. The Company's ability to maintain its recent trend of revenue growth is in large part dependent on the continued development, introduction and market acceptance of new products.

GROSS MARGIN The Company's gross margin as a percentage of revenue was 59% for all three fiscal years presented. Profit margins on older products tend to decrease over time as selling prices decline, but the Company's strategy has been to offset these decreases by introducing new products with higher margins.

RESEARCH AND DEVELOPMENT Research and development expense was $27.8 million, $26.8 million and $22.9 million in fiscal 1997, 1996 and 1995, respectively. Spending increases were related primarily to the development of new technologies and new products, including the Company's high-density product families and related software development tools. The Company believes that a continued commitment to research and development is essential in order to maintain product leadership in its existing product families and to provide innovative new product offerings, and therefore expects to continue to make significant investments in research and development in the future.

SELLING, GENERAL AND ADMINISTRATIVE Selling, general and administrative expense was $33.6 million, $31.3 million and $25.0 million in fiscal 1997, 1996 and 1995, respectively. Spending increases were primarily due to expansion of the Company's sales force, the addition of field applications

engineers to provide enhanced customer assistance, and higher sales commissions associated with higher revenue levels. Selling, general and administrative expense as a percentage of revenue was 16% in fiscal 1997 and 1996, a slight decrease from 17% in fiscal 1995.

INCOME FROM OPERATIONS Income from operations increased 2%, from $57.8 million to $59.0 million, from fiscal 1996 to fiscal 1997, and increased 55%, from $37.3 million, between fiscal 1995 and fiscal 1996. Income from operations increased as a percentage of revenue, from 26% in fiscal 1995 to 29% in fiscal 1996 and fiscal 1997.

INTEREST AND OTHER INCOME Interest and other income (net of expense) increased by approximately $3.3 million from fiscal 1996 to fiscal 1997, and by approximately $2.1 million from fiscal 1995 to fiscal 1996. The increase in both fiscal years was due to higher cash and investment balances resulting from the Company's follow-on public offering of common stock in November 1995, cash generated from operations and common stock issuance from employee stock option exercises.

PROVISION FOR INCOME TAXES The Company's effective tax rate was 33.5% for fiscal 1997 as compared to 33.9% and 33.6% recorded in fiscal 1996 and 1995, respectively. The fiscal 1997 decrease was primarily due to increased benefit from tax-exempt investment income. The fiscal 1996 increase was due to the absence of tax credit carryforwards available in prior years, although this increase was offset somewhat by lower state taxes.

Deferred tax asset valuation allowances are recorded to offset deferred tax assets that can only be realized by earning taxable income in distant future years. Management established the valuation allowances because it cannot determine if it is more likely than not that such income will be earned.

NET INCOME Net income increased 8%, from $41.8 million to $45.0 million, from fiscal 1996 to fiscal 1997, and increased 55%, from $27.0 million, between fiscal 1995 and fiscal 1996. Net income increased as a percentage of revenue each fiscal year, from 19% in fiscal 1995 to 21% in fiscal 1996, and then to 22% in fiscal 1997.

FACTORS AFFECTING FUTURE RESULTS

Notwithstanding the objectives, projections, estimates and other forward-looking statements in this Annual Report, the Company's future operating results will continue to be subject to variations based on a wide variety of factors, including, but not limited to, the following: the Company's continued ability to obtain adequate wafer capacity supply commitments under competitive pricing terms, successful implementation of the Company's proprietary process technology, UltraMOS-Registered Trademark-, at its wafer manufacturers, successful development and implementation of future new advanced process technologies, attainment of acceptable wafer manufacturing yields, the ability to achieve volume production at Seiko Epson Corporation's ("Seiko Epson") new eight-inch facility or United Integrated Circuit Corporation ("UICC") and potential interruptions in supply from the Company's wafer manufacturers and assembly contractors as a result of work stoppages, political instability or natural or man-made disasters.

The Company's operating results also depend in large part on various factors outside the Company's control such as general economic conditions, the cyclical nature of both the semiconductor industry and the markets addressed by the Company's products, sudden price fluctuations, general price erosion, substantial adverse currency exchange movements and changes in effective tax rates. The semiconductor industry is highly cyclical and has been subject to significant downturns at various times that have been characterized by diminished product demand, production overcapacity and accelerated erosion of average selling prices. The Company's rate of growth in recent periods has been positively and negatively impacted by trends in the semiconductor industry. Any material imbalance in industry-wide production capacity relative to demand, shift in industry capacity toward products competitive with the Company's products, reduced demand or reduced growth in demand or other factors could result in a decline in the demand for or the prices of the Company's products and have a material adverse effect on the Company's operating results. The Company's operating results are also dependent upon international revenues which may be adversely affected by the imposition of government controls, export license requirements, trade restrictions, political instability, changes in tariffs and other factors outside the Company's control. Due to these and other factors, the Company's past results are a less useful predictor of future results than is the case in more mature and stable industries. The market price of the Company's common stock could be subject to significant fluctuations due to the inherent volatility of the semiconductor industry combined with the aforementioned and other factors, including variations in the Company's quarterly operating results and shortfalls in revenues or earnings from levels expected by securities analysts. In addition, the stock market can experience significant price fluctuations, which often are unrelated to the operating performance of the specific companies whose stocks are traded. Broad market fluctuations, as well as economic conditions generally and in the semiconductor industry specifically, may adversely affect the market price of the Company's common stock.

In addition, the Company's operating results are subject to variations based upon the following competitive factors: introduction of new products on a timely basis that meet market needs at competitive prices with acceptable margins, market acceptance of the Company's new and proprietary products and proprietary software development tools, variations in product mix, scheduling, rescheduling and cancellation of large orders, successful protection of the Company's intellectual property rights, potential litigation relating to competitive patents and intellectual property and the Company's ability to attract and retain highly qualified technical and management personnel.

For further explanation of the factors set forth above, see "Factors Affecting Future Results" in Item 1 of the Company's Annual Report on Form 10-K for the fiscal year ended March 29, 1997.

LIQUIDITY AND CAPITAL RESOURCES

As of March 29, 1997, the Company's principal source of liquidity was $228.6 million of cash and short-term investments, an increase of $13.5 million from the balance of $215.2 million at March 30, 1996. This increase was primarily the result of cash generated from operations and common stock issuance from employee stock option exercises in excess of cash required for foundry investments and

wafer supply advances made in fiscal 1997 as further described below. The Company also has available an unsecured $10 million demand bank credit facility with interest due on outstanding bal-

ances at a money market rate. This facility has not been used.

Accounts receivable and deferred income on sales to distributors increased $3.1 million and $1.4 million, or 13% and 8%, respectively, as compared to the balances at March 30, 1996. These increases were primarily due to higher revenue levels in the fiscal 1997 fourth quarter and the timing of billings to end customers and distributors. Inventories increased by $6.0 million, or 28%, versus amounts recorded at March 30, 1996 due to increased production in anticipation of future requirements. Prepaid expenses and other current assets decreased by $2.8 million, or 14%, as compared to the balance at March 30, 1996 due primarily to a decrease in the current portion of wafer supply advances. The $36.8 million increase in Foundry investments, advances and other assets was primarily due to the $25.8 million paid in January 1997 in the second of three planned payments representing the Company's investment in UICC. In March 1997, the Company paid approximately $17.0 million to Seiko Epson pursuant to a second advance payment purchase agreement. This advance offset the decline in wafer supply advances related to fiscal 1997 wafer deliveries. See below and Note 4 of Notes to Consolidated Financial Statements. Accrued payroll obligations increased $2.2 million, or 29%, as compared to the balance at March 30, 1996 due to higher variable compensation, increased headcount and timing of payments. Income taxes payable decreased $4.0 million, or 84%, as compared to the balance at March 30, 1996 due to the timing of tax deductions and payments.

Stockholders' equity increased by approximately $61.7 million, primarily due to net income of approximately $45.0 million for fiscal 1997 and net proceeds from common stock issuance.

Capital expenditures were approximately $10.6 million, $12.6 million and $6.3 million for fiscal years 1997, 1996 and 1995, respectively. These expenditures consisted primarily of manufacturing test equipment, lab equipment, engineering workstations, buildings and building improvements. The increase in fiscal 1997 and 1996 capital expenditures over fiscal 1995 was associated with higher production levels noted above and included increased investment in manufacturing test equipment to support the growth in revenue of high-density products.

The Company currently anticipates capital expenditures of approximately $20 million to $30 million for the fiscal year ending March 28, 1998. A significant portion of these expenditures is planned for improvements and expansions to the Company's facilities and manufacturing capacity.

The majority of the Company's silicon wafer purchases are denominated in Japanese yen. The Company maintains yen-denominated bank accounts and bills its Japanese customers in yen. The yen bank deposits utilized to hedge yen-denominated wafer purchases are accounted for as identifiable hedges against specific and firm wafer purchases.

The Company entered into a series of agreements with United Microelectronics Corporation ("UMC") in September 1995 pursuant to which the Company has agreed to join UMC and several other companies to form a separate Taiwanese Company, UICC, for the purpose of building and operating an advanced semiconductor manufacturing facility in Taiwan, Republic of China. Under the terms of the agreements, the Company will invest approximately $53 million, payable in three installments over two years, for an approximately 10% equity interest in UICC and the right to receive a percentage of the facility's wafer production at market prices. The timing of the payments is related to certain milestones in the development of the advanced semiconductor manufacturing facility. The first payment, in the amount of approximately $13.7 million, was paid in January 1996, the second payment, in the amount of approximately $25.8 million, was paid in January 1997, and the final payment is anticipated to be required within the six-month period ending December 1997.

In March 1997, the Company entered into a second advance payment production agreement with Seiko Epson and its affiliated U.S. distributor, S-MOS Systems Inc. ("SMOS") under which it agreed to advance approximately $90 million, payable over two years, to Seiko Epson to finance construction of an eight-inch sub-micron semiconductor wafer manufacturing facility. Under the terms of the agreement, the advance is to be repaid with semiconductor wafers over a multi-year period. The agreement calls for wafers to be supplied by Seiko Epson through SMOS pursuant to purchase agreements with SMOS. The Company also has an option under this agreement to advance Seiko Epson an additional $60 million for additional wafer supply under similar terms. The first payment pursuant to this agreement, approximately $17.0 million, was made during March 1997. As a result of the future payments to UICC and Seiko Epson, the Company's cash and short-term investments will be reduced by a minimum of approximately $86.5 million over the time period of the remaining payments.

The Company believes that its existing sources of liquidity and expected cash generated from operations will be adequate to fund the Company's anticipated cash needs for at least the next twelve months, including the anticipated required payments to UICC and Seiko Epson during this time period.

In an effort to secure additional wafer supply, the Company may from time to time consider various financial arrangements including joint ventures with, minority investments in, advance purchase payments to, loans to, or similar arrangements with independent wafer manufacturers in exchange for committed wafer capacity. To the extent that the Company pursues any such additional financial arrangements, additional debt or equity financing may be required. There can be no assurance that any such additional funding could be obtained when needed or, if available, on terms acceptable to the Company.

SELECTED FINANCIAL DATA

(IN THOUSANDS, EXCEPT PER SHARE DATA)	YEAR ENDED MARCH 29, 1997	MARCH 30, 1996	APRIL 1, 1995	APRIL 2, 1994	APRIL 3, 1993
STATEMENT OF OPERATIONS DATA:					
Revenue	$204,089	$198,167	$144,083	$126,241	$103,391
Costs and expenses:					
Cost of products sold	83,736	82,216	58,936	53,266	43,650
Research and development	27,829	26,825	22,859	20,636	16,530
Selling, general and administrative	33,558	31,323	25,020	22,299	20,465
	145,123	140,364	106,815	96,201	80,645
Income from operations	58,966	57,803	37,268	30,040	22,746
Interest and other income, net	8,712	5,442	3,349	2,566	2,470
Income before provision for income taxes	67,678	63,245	40,617	32,606	25,216
Provision for income taxes	22,673	21,461	13,651	10,116	7,817
Net income	$ 45,005	$ 41,784	$ 26,966	$ 22,490	$ 17,399
Net income per share	$ 1.96	$ 1.99	$ 1.41	$ 1.19	$ 0.94
Weighted average common and common equivalent shares outstanding	22,973	20,979	19,164	18,946	18,458
BALANCE SHEET DATA:					
Working capital	$267,669	$244,649	$106,021	$105,007	$ 79,878
Total assets	403,462	342,935	192,917	146,093	128,876
Stockholders' equity	360,491	298,768	157,797	125,068	98,481

	YEAR ENDED MARCH 29, 1997				YEAR ENDED MARCH 30, 1996			
	FOURTH QUARTER	THIRD QUARTER	SECOND QUARTER	FIRST QUARTER	FOURTH QUARTER	THIRD QUARTER	SECOND QUARTER	FIRST QUARTER
UNAUDITED QUARTERLY DATA:								
Revenue	$56,268	$51,015	$48,638	$48,168	$53,008	$51,538	$48,608	$45,013
Gross profit	$33,332	$30,048	$28,643	$28,330	$31,094	$30,195	$28,418	$26,244
Net income	$12,819	$11,278	$10,460	$10,448	$12,097	$11,063	$ 9,778	$ 8,846
Net income per share	$ 0.55	$ 0.49	$ 0.46	$ 0.46	$ 0.54	$ 0.52	$ 0.49	$ 0.45

ALL SHARE AND PER SHARE AMOUNTS HAVE BEEN ADJUSTED TO REFLECT THE THREE-FOR-TWO STOCK SPLIT EFFECTED IN THE FORM OF A STOCK DIVIDEND WHICH WAS PAID ON JULY 6, 1993.

CONSOLIDATED BALANCE SHEET

(IN THOUSANDS, EXCEPT SHARE AND PAR VALUE AMOUNTS)	MARCH 29, 1997	MARCH 30, 1996
ASSETS		
Current assets:		
Cash and cash equivalents	$ 53,949	$ 54,600
Short-term investments	174,698	160,570
Accounts receivable, net	25,940	22,884
Inventories (note 2)	27,809	21,761
Prepaid expenses and other current assets (note 9)	16,519	19,301
Deferred income taxes (note 7)	11,725	9,700
Total current assets	310,640	288,816
Foundry investments, advances and other assets (notes 4 and 9)	65,419	28,648
Property and equipment, less accumulated depreciation (note 3)	27,403	25,471
	$403,462	$342,935
LIABILITIES AND STOCKHOLDERS' EQUITY		
Current liabilities:		
Accounts payable and accrued expenses (note 9)	$ 14,276	$ 15,015
Accrued payroll obligations	9,648	7,456
Income taxes payable (note 7)	782	4,800
Deferred income	18,265	16,896
Total current liabilities	42,971	44,167
Commitments and contingencies (notes 4, 6, 9, 10 and 11)	--	--
Stockholders' equity (note 8):		
Preferred stock, $.01 par value, 10,000,000 shares authorized; none issued and outstanding	--	--
Common stock, $.01 par value, 100,000,000 shares authorized; 22,877,724 and 22,123,069 shares issued and outstanding	229	221
Paid-in capital	198,667	181,957
Retained earnings	161,595	116,590
	360,491	298,768
	$403,462	$342,935

THE ACCOMPANYING NOTES ARE AN INTEGRAL PART OF THIS STATEMENT.

CONSOLIDATED STATEMENT OF OPERATIONS

(IN THOUSANDS, EXCEPT PER SHARE DATA)	YEAR ENDED MARCH 29, 1997	MARCH 30, 1996	APRIL 1, 1995
Revenue	$204,089	$198,167	$144,083
Costs and expenses:			
Cost of products sold (note 9)	83,736	82,216	58,936
Research and development	27,829	26,825	22,859
Selling, general and administrative (note 12)	33,558	31,323	25,020
	145,123	140,364	106,815
Income from operations	58,966	57,803	37,268
Other income (expense):			
Interest income	8,886	5,570	3,437
Other expense, net	(174)	(128)	(88)
Income before provision for income taxes	67,678	63,245	40,617
Provision for income taxes (note 7)	22,673	21,461	13,651
Net income	$ 45,005	$ 41,784	$ 26,966
Net income per share	$ 1.96	$ 1.99	$ 1.41
Weighted average number of common and common equivalent shares outstanding	22,973	20,979	19,164

THE ACCOMPANYING NOTES ARE AN INTEGRAL PART OF THIS STATEMENT.

CONSOLIDATED STATEMENT OF CHANGES IN STOCKHOLDERS' EQUITY

(IN THOUSANDS, EXCEPT PAR VALUE)	COMMON STOCK ($.01 PAR VALUE) SHARES	AMOUNT	PAID-IN CAPITAL	RETAINED EARNINGS	TOTAL
Balances, April 2, 1994	18,411	$184	$ 77,044	$ 47,840	$125,068
Common stock issued	479	5	3,659	--	3,664
Tax benefit of option exercises	--	--	2,133	--	2,133
Other	--	--	(34)	--	(34)
Net income for fiscal 1995	--	--	--	26,966	26,966
Balances, April 1, 1995	18,890	189	82,802	74,806	157,797
Net proceeds from public offering	2,500	25	86,676	--	86,701
Other common stock issued	733	7	5,416	--	5,423
Tax benefit of option exercises	--	--	6,961	--	6,961
Other	--	--	102	--	102
Net income for fiscal 1996	--	--	--	41,784	41,784
Balances, March 30, 1996	22,123	221	181,957	116,590	298,768
Common stock issued	755	8	10,516	--	10,524
Tax benefit of option exercises	--	--	6,179	--	6,179
Other	--	--	15	--	15
Net income for fiscal 1997	--	--	--	45,005	45,005
Balances, March 29, 1997	22,878	$229	$198,667	$161,595	$360,491

THE ACCOMPANYING NOTES ARE AN INTEGRAL PART OF THIS STATEMENT.

CONSOLIDATED STATEMENT OF CASH FLOWS

(IN THOUSANDS)	YEAR ENDED MARCH 29, 1997	MARCH 30, 1996	APRIL 1, 1995
Cash flow from operating activities:			
Net income	$ 45,005	$ 41,784	$ 26,966
Adjustments to reconcile net income to net cash provided (used) by operating activities:			
Depreciation and amortization	8,629	7,137	6,007
Deferred income taxes	(2,025)	(2,398)	(1,781)
Changes in assets and liabilities:			
Accounts receivable	(3,056)	(4,737)	(6,486)
Inventories	(6,048)	(7,630)	(284)
Prepaid expenses and other current assets	(750)	(450)	(100)
Foundry investments, advances and other assets	(33,239)	(3,087)	(42,673)
Accounts payable and accrued expenses	(739)	2,241	6,516
Accrued payroll obligations	2,192	2,067	1,799
Income taxes payable	(4,018)	(406)	1,115
Deferred income	1,369	5,145	4,665
Net cash provided (used) by operating activities	7,320	39,666	(4,256)
Cash flow from investing activities:			
Purchase of short-term investments, net	(14,128)	(79,457)	(5,874)
Proceeds from sale of fixed assets	--	98	--
Capital expenditures	(10,561)	(12,591)	(6,299)
Net cash used by investing activities	(24,689)	(91,950)	(12,173)
Cash flow from financing activities:			
Net proceeds from issuance of common stock	16,718	99,187	5,763
Net cash provided by financing activities	16,718	99,187	5,763
Net (decrease) increase in cash and cash equivalents	(651)	46,903	(10,666)
Beginning cash and cash equivalents	54,600	7,697	18,363
Ending cash and cash equivalents	$ 53,949	$ 54,600	$ 7,697

THE ACCOMPANYING NOTES ARE AN INTEGRAL PART OF THIS STATEMENT.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS

NOTE 1. NATURE OF OPERATIONS AND SIGNIFICANT ACCOUNTING POLICIES

NATURE OF OPERATIONS Lattice Semiconductor Corporation (the "Company"), founded in 1983 and based in Hillsboro, Oregon, designs, develops and markets high performance programmable logic devices ("PLDs") and related development system software. The Company is the inventor and world's leading supplier of in-system programmable ("ISP-TM-") logic devices. PLDs are standard semiconductor components that can be configured by the end customer as specific logic functions, enabling shorter design cycle times and reduced development costs. The Company's end customers are primarily original equipment manufacturers ("OEMs") in the fields of communications, computing, computer peripherals, instrumentation, industrial controls and military systems. Nearly one-half of the Company's revenue is derived from international sales, mainly in Europe and Asia.

FISCAL REPORTING PERIOD AND PRINCIPLES OF CONSOLIDATION The Company reports on a 52- or 53-week fiscal year, which ends on the Saturday closest to March 31. The accompanying consolidated financial statements include the accounts of Lattice Semiconductor Corporation and its wholly owned foreign subsidiaries, Lattice GmbH, Lattice Semiconducteurs SARL, Lattice Semiconductor KK, Lattice Semiconductor Shanghai Co., Ltd., Lattice Semiconductor Asia Ltd., Lattice Semiconductor International Ltd., Lattice Semiconductor UK Ltd. and Lattice Semiconductor AB. The assets, liabilities, and results of operations of these entities were not material for any of the years presented in the consolidated financial statements and all intercompany accounts and transactions have been eliminated.

CASH EQUIVALENTS AND SHORT-TERM INVESTMENTS The Company considers all highly liquid investments, which are readily convertible into cash and have original maturities of three months or less, to be cash equivalents. Short-term investments, which have maturities greater than three months and less than one year, are composed of money market preferred stocks ($109.0 million), government obligations ($57.8 million), commercial paper ($4.3 million) and time deposits ($3.6 million) at March 29, 1997.

Effective beginning in fiscal 1995, the Company adopted Statement of Financial Accounting Standards No. 115, "Accounting for Certain Investments in Debt and Equity Securities" (SFAS No. 115), which creates certain classification categories for such investments based on the nature of the securities and intent of the Company. SFAS No. 115 was adopted on a prospective basis, and the cumulative effect of adoption was not material. Pursuant to adoption, the Company has categorized its investments as held-to-maturity. Securities classified as held-to-maturity are stated at amortized cost with corresponding premiums or discounts amortized over the life of the investment to interest income. Amortized cost approximates market value at March 29, 1997.

FINANCIAL INSTRUMENTS All of the Company's significant financial assets and liabilities are recognized in the Consolidated Balance Sheet as of March 29, 1997 and March 30, 1996. The value reflected in the Consolidated Balance Sheet (carrying value) approximates fair value for the Company's financial assets and liabilities. The Company estimates the fair value of its cash and cash equivalents, short-term investments, accounts receivable, other current assets and current liabilities based upon existing interest rates related to such assets and liabilities compared to the current market rates of interest for instruments of similar nature and degree of risk.

DERIVATIVE FINANCIAL INSTRUMENTS Effective beginning in the first quarter of fiscal 1995, the Company adopted Statement of Financial Accounting Standards No. 119, "Disclosures about Derivative Financial Instruments and Fair Value of Financial Instruments" (SFAS 119). In order to minimize exposure to foreign exchange risk with respect to its long-term investments made with foreign currencies as further described in note 4 of notes to consolidated financial statements, the Company has at times entered into foreign forward exchange contracts in order to hedge these transactions. These contracts are accounted for as identifiable hedges against firm Company commitments. Realized gain or loss with respect to these contracts for the fiscal periods presented was not material. As of March 29, 1997, the Company had no open foreign exchange contracts for the purchase or sale of foreign currencies.

The Company does not enter into derivative financial instruments for trading purposes.

FOREIGN EXCHANGE The majority of the Company's silicon wafer purchases are denominated in Japanese yen. The Company maintains yen-denominated bank accounts and bills its Japanese customers in yen. The yen bank deposits utilized to hedge yen-denominated wafer purchases are accounted for as identifiable hedges against specific and firm wafer purchases. Gains or losses from foreign exchange rate fluctuations on unhedged balances denominated in foreign currencies are reflected in other income. Realized and unrealized gains or losses were not significant for the fiscal periods presented.

CONCENTRATIONS OF CREDIT RISK Financial instruments which potentially expose the Company to concentrations of credit risk consist primarily of short-term investments and trade receivables. The Company places its investments through several financial institutions and mitigates the concentration of credit risk by placing percentage limits on the maximum portion of the investment portfolio which may be invested in any one investment instrument. Investments consist primarily of A1 and P1 or better rated U.S. commercial paper, U.S. government agency obligations and other money market instruments, "AA" or better rated municipal obligations, money market preferred stocks and other time deposits. Concentrations of credit risk with respect to trade receivables are mitigated by a geographically diverse customer base and the Company's credit and collection process. The

Company performs credit evaluations for all customers and secures transactions with letters of credit or advance payments where necessary. Write-offs for uncollected trade receivables have not been significant to date.

REVENUE RECOGNITION AND ACCOUNTS RECEIVABLE Revenue from sales to OEM customers is recognized upon shipment. Certain of the Company's sales are made to distributors under agreements providing price protection and right of return on unsold merchandise. Revenue and cost relating to such distributor sales are deferred until the product is sold by the distributor and related revenue and costs are then reflected in income. Accounts receivable are shown net of allowance for doubtful accounts of $874,000 and $800,000 at March 29, 1997 and March 30, 1996, respectively.

No individual customer or distributor accounted for more than 10% of revenue in fiscal 1997. Revenue from one distributor was $21.1 million for fiscal 1996. Revenue from two distributors was $17.3 and $16.1 million for fiscal 1995. Export revenue was approximately $99.8 million, $95.1 million and $68.4 million for fiscal 1997, 1996 and 1995, respectively. Sales to Europe were approximately $39.9 million, $37.9 million and $24.5 million, and to Asia $52.6 million, $52.4 million and $40.6 million in fiscal 1997, 1996 and 1995, respectively.

INVENTORIES Inventories are stated at the lower of first-in, first-out cost or market.

LONG-LIVED ASSETS During the fiscal year ended March 29, 1997, the Company adopted the Financial Accounting Standards Board Statement No. 121 (SFAS 121), "Accounting for the Impairment of Long-Lived Assets and for Long-Lived Assets to be Disposed of", which requires the Company to review the impairment of long-lived assets whenever events or changes in circumstances indicate that the carrying amount of an asset may not be recoverable. The adoption of SFAS 121 did not have a material impact on the Company's financial condition or results of operations.

PROPERTY AND EQUIPMENT Property and equipment are stated at cost. Depreciation is computed using the straight-line method for financial reporting purposes over the estimated useful lives of the related assets, generally three to five years for equipment and thirty years for buildings. Accelerated methods of computing depreciation are generally used for income tax purposes.

TRANSLATION OF FOREIGN CURRENCIES The Company translates accounts denominated in foreign currencies in accordance with Statement of Financial Accounting Standards No. 52, "Foreign Currency Translation." Translation adjustments related to the consolidation of foreign subsidiary financial statements have not been significant to date.

RESEARCH AND DEVELOPMENT Research and development costs are expensed as incurred.

INCOME TAXES Income taxes are calculated in accordance with SFAS No. 109, "Accounting for Income Taxes," which the Company adopted on a prospective basis in the first quarter of fiscal 1994. The cumulative effect of the adoption of SFAS 109 was not material.

STOCK-BASED COMPENSATION The Company accounts for its employee and director stock options and employee stock purchase plan in accordance with provisions of the Accounting Principles Board Opinion No. 25 (APB 25), "Accounting for Stock Issued to Employees." During 1995, the Financial Accounting Standards Board issued Statement of Financial Accounting Standards No. 123 (SFAS 123), "Accounting for Stock-Based Compensation." SFAS 123, effective for fiscal years beginning after December 31, 1995, provides an alternative to APB 25, but allows companies to account for employee and director stock-based compensation under the current intrinsic value method as prescribed by APB 25. The Company has continued to account for its employee and director stock plans in accordance with APB 25. Additional pro forma disclosures as required under SFAS 123 are presented in note 8 of notes to consolidated financial statements.

NET INCOME PER SHARE Net income per share is computed based on the weighted average number of shares of common stock and common stock equivalents assumed to be outstanding during the period (using the treasury stock method). Common stock equivalents consist of stock options and warrants to purchase common stock. All share and per share amounts presented in the accompanying consolidated financial statements and notes thereto have been adjusted to reflect the three-for-two stock split effected in the form of a stock dividend which was paid on July 6, 1993.

In February 1997, the Financial Accounting Standards Board issued Statement of Financial Accounting Standards No. 128 (SFAS 128), "Earnings Per Share." In accordance with this pronouncement, the Company will adopt the new standard for periods ending after December 15, 1997.

STATEMENT OF CASH FLOWS Income taxes paid approximated $22.6 million, $17.3 million and $11.9 million in fiscal 1997, 1996, and 1995, respectively. Interest paid does not differ materially from interest expense, which aggregated approximately $152,000, $42,000 and $28,000 in fiscal 1997, 1996 and 1995, respectively.

USE OF ESTIMATES The preparation of financial statements in conformity with generally accepted accounting principles requires management to make estimates and assumptions that affect the reported amounts of assets and liabilities and disclosure of contingent assets and liabilities at the date of the financial statements and the reported amounts of revenues and expenses during the fiscal periods presented. Actual results could differ from those estimates.

FINANCIAL PRESENTATION Certain prior year amounts in the consolidated financial statements have been reclassified to conform to the fiscal 1997 presentation.

NOTE 2. INVENTORIES

(IN THOUSANDS)	MARCH 29, 1997	MARCH 30, 1996
Work in progress	$20,286	$13,174
Finished goods	7,523	8,587
	$27,809	$21,761

NOTE 3. PROPERTY AND EQUIPMENT

(IN THOUSANDS)	MARCH 29, 1997	MARCH 30, 1996
Land	$ 2,098	$ 1,455
Buildings	7,132	5,892
Computer and test equipment	52,204	44,333
Office furniture and equipment	2,881	2,712
Leasehold and building improvements	2,501	2,465
	66,816	56,857
Accumulated depreciation and amortization	(39,413)	(31,386)
	$ 27,403	$ 25,471

NOTE 4. FOUNDRY INVESTMENTS, ADVANCES AND OTHER ASSETS

(IN THOUSANDS)	MARCH 29, 1997	MARCH 30, 1996
Foundry investments and other assets	$48,399	$14,141
Wafer supply advances	17,020	14,507
	$65,419	$28,648

The Company entered into a series of agreements with United Microelectronics Corporation ("UMC") in September 1995 pursuant to which the Company agreed to join UMC and several other companies to form a separate Taiwanese corporation, United Integrated Circuit Corporation ("UICC"), for the purpose of building and operating an advanced semiconductor manufacturing facility in Taiwan, Republic of China. Under the terms of the agreements, the Company will invest approximately $53 million, payable in three installments over two years, for an approximately 10% equity interest in the corporation and the right to receive a percentage of the facility's wafer production at market prices. This investment is accounted for at cost. The timing of the payments is related to certain milestones in the development of the advanced semiconductor manufacturing facility. The first payment, in the amount of approximately $13.7 million, was paid in January 1996, the second payment, in the amount of approximately $25.8 million, was paid during January 1997, and the final payment is anticipated to be required within the six-month period ending December 1997.

In July 1994, the Company signed an agreement with Seiko Epson Corporation ("Seiko Epson") and its affiliated U.S. distributor, S-MOS Systems Inc. ("SMOS"), under which it advanced $44 million to be used to finance additional sub-micron wafer manufacturing capacity and technological development. The advance is being repaid in the form of semiconductor wafers over a multi-year period. No interest income is recorded. Total wafer receipts under this agreement aggregated approximately $18,042,000, $10,713,000 and $1,430,000 during fiscal 1997, 1996 and 1995, respectively. The balance sheet caption "Prepaid expenses and other current assets" at March 29, 1997 includes the remaining amount of such wafers to be received under this agreement, aggregating $13,729,000.

In March 1997, the Company entered into a second advance payment production agreement with Seiko Epson and SMOS under which it agreed to advance approximately $90 million, payable over two years, to Seiko Epson to finance construction of an eight-inch sub-micron semiconductor wafer manufacturing facility. Under the terms of the agreement, the advance is to be repaid with semiconductor wafers over a multi-year period. No interest income is recorded. The agreement calls for wafers to be supplied by Seiko Epson through SMOS pursuant to purchase agreements with SMOS. The Company also has an option under the agreement to advance Seiko Epson an additional $60 million for additional wafer supply under similar terms. The first payment pursuant to this agreement, approximately $17.0 million, was made during March 1997.

NOTE 5. CREDIT FACILITIES

The Company has available an unsecured $10 million demand bank credit facility with interest due on outstanding balances at a money market rate. This facility has not been used.

NOTE 6. LEASE OBLIGATIONS

Certain facilities and equipment of the Company are leased under operating leases, which expire at various times through fiscal 2000. Rental expense under the operating leases was approximately $984,000, $993,000 and $815,000 for fiscal 1997, 1996 and 1995, respectively.

Future minimum lease commitments at March 29, 1997 are as follows:

FISCAL YEAR	(IN THOUSANDS)
1998	$ 691
1999	271
2000	45
	$1,007

NOTE 7. INCOME TAXES

The components of the provision for income taxes for fiscal 1997, 1996 and 1995 are presented in the following table:

	YEAR ENDED		
(IN THOUSANDS)	MARCH 29, 1997	MARCH 30, 1996	APRIL 1, 1995
Current:			
Federal	$22,308	$21,550	$13,849
State	2,390	2,309	1,583
	24,698	23,859	15,432
Deferred:			
Federal	(1,829)	(2,166)	(1,598)
State	(196)	(232)	(183)
	(2,025)	(2,398)	(1,781)
	$22,673	$21,461	$13,651

Foreign income taxes were not significant for the fiscal years presented.

The provision for income taxes differs from the amount of income tax determined by applying the applicable U.S. statutory federal income tax rate to pretax income as a result of the following differences:

	YEAR ENDED		
(IN THOUSANDS)	MARCH 29, 1997	MARCH 30, 1996	APRIL 1, 1995
Computed income tax expense at the statutory rate	$23,687	$22,136	$14,216
Adjustments for tax effects of:			
State taxes, net	2,048	1,636	1,625
Research and development credits, current	(62)	(196)	(193)
Research and development and investment tax credit carryforwards	--	--	(243)
Nontaxable investment income	(2,579)	(1,506)	(1,020)
Other	(421)	(609)	(734)
	$22,673	$21,461	$13,651

The components of the Company's net deferred tax asset under SFAS No. 109 were as follows:

(IN THOUSANDS)	MARCH 29, 1997	MARCH 30, 1996
Deferred income	$7,102	$6,343
Expenses and allowances not currently deductible	6,619	5,693
Total deferred tax assets	13,721	12,036
Valuation allowance	(1,996)	(2,336)
	$11,725	$9,700

The valuation allowances are recorded to offset deferred tax assets which can only be realized by earning taxable income in distant future years. Management established the valuation allowances because it cannot determine if it is more likely than not that such income will be earned.

NOTE 8. STOCKHOLDERS' EQUITY

COMMON STOCK In November 1995, the Company completed its third public offering, consisting of 2,500,000 shares of common stock at $36.63 per share. Net proceeds to the Company were approximately $86.7 million after underwriting discount and offering expenses.

STOCK WARRANTS The Company has issued to a vendor warrants to purchase 464,125 shares of common stock. Of this amount, 402,000 warrants were issued and 295,500 exercised prior to fiscal 1995. During fiscal 1995, the Company issued an additional 62,125 shares at $17.38 per share. During fiscal 1996, the vendor exercised warrants for 45,000 shares, at an exercise price of $20.17 per share. The rights to the remaining 123,625 warrants were forfeited in exchange for the issuance of a warrant to purchase 67,419 shares of common stock which were earned ratably from March 1996 through February 1997.

STOCK OPTION PLANS As of March 29, 1997, the Company had reserved 2,000,000 and 5,775,000 shares of common stock for issuance to officers and key employees under the 1996 Stock Option Plan and 1988 Stock Option Plan, respectively. The 1996 Plan options generally vest over four years in increments as determined by the Board of Directors and may have terms up to ten years. The 1988 Plan options are exercisable immediately and expire five years from the date of grant. The transfer of certain shares of common stock acquired through the exercise of 1988 Plan stock options is restricted under stock vesting agreements that grant the Company the right to repurchase

unvested shares at the exercise price if employment is terminated. Generally, the Company's repurchase rights lapse quarterly over four years.

The 1993 Directors Stock Option Plan provides for the issuance of stock options to members of the Company's Board of Directors who are not employees of the Company; 225,000 shares of the Company's common stock are reserved for issuance thereunder. These options are granted at fair market value at the date of grant and generally become exercisable quarterly over a four-year period beginning on the date of grant and expire five years from the date of grant.

The following table summarizes the Company's stock option activity and related information for the past three years:

	YEAR ENDED					
	MARCH 29, 1997		MARCH 30, 1996		APRIL 1, 1995	
(NUMBER OF SHARES IN THOUSANDS)	NUMBER OF SHARES UNDER OPTION	WEIGHTED-AVERAGE EXERCISE PRICE	NUMBER OF SHARES UNDER OPTION	WEIGHTED-AVERAGE EXERCISE PRICE	NUMBER OF SHARES UNDER OPTION	WEIGHTED-AVERAGE EXERCISE PRICE
Options outstanding at beginning of fiscal year	2,330	$22.20	2,340	$14.15	2,322	$11.92
Options granted	827	30.82	807	33.37	548	18.54
Options canceled	(176)	28.31	(196)	14.90	(127)	16.77
Options exercised	(691)	13.31	(621)	8.79	(403)	6.33
Options outstanding at end of fiscal year	2,290	27.50	2,330	22.20	2,340	14.15

The following table summarizes information about stock options outstanding at March 29, 1997:

	OPTIONS OUTSTANDING			OPTIONS EXERCISABLE	
RANGE OF EXERCISE PRICES	NUMBER OF SHARES	WEIGHTED-AVERAGE REMAINING CONTRACT LIFE (IN YEARS)	WEIGHTED-AVERAGE EXERCISE PRICE	NUMBER OF SHARES	WEIGHTED-AVERAGE EXERCISE PRICE
(NUMBER OF SHARES IN THOUSANDS)					
$10.17 - $15.00	86	0.07	$12.31	82	$12.25
$16.37 - $23.50	439	1.27	18.38	275	18.38
$23.75 - $32.88	1,425	2.41	28.35	454	26.77
$34.00 - $51.88	340	2.96	39.76	70	36.50
	2,290	2.18	27.52	881	23.55

STOCK PURCHASE PLAN The Company's employee stock purchase plan was approved by the stockholders in August 1990, and became effective January 1, 1991. The plan permits eligible employees to purchase shares of common stock through payroll deductions, not to exceed 10% of the employee's compensation. The purchase price of the shares is the lower of 85% of the fair market value of the stock at the beginning of each six-month period or 85% of the fair market value at the end of such period, but in no event less than the book value per share at the mid-point of each offering period. Amounts accumulated through payroll deductions during the offering period are used to purchase shares on the last day of the offering period. Of the 450,000 shares authorized to be issued under the plan, 57,421, 54,239 and 70,973 shares were issued during fiscal 1997, 1996 and 1995, respectively, and 57,809 shares were available for issuance at March 29, 1997.

PRO FORMA DISCLOSURES The Company accounts for its stock options and employee stock purchase plan in conformity with APB 25 and has adopted the additional proforma disclosure provisions of SFAS 123.

The fair value, as defined by SFAS 123, for stock options and employee stock plan purchase rights was estimated on the date of grant using the Black-Scholes option pricing model with the following assumptions:

	GRANTS FOR YEARS ENDED	
	MARCH 29, 1997	MARCH 30, 1996
Stock options:		
Expected volatility	46.4%	46.4%
Risk-free interest rate	6.1%	5.9%
Expected term	3 years	3 years
Dividend yield	0%	0%
Stock purchase rights:		
Expected volatility	36.7%	36.7%
Risk-free interest rate	5.3%	6.2%
Expected term	6 months	6 months
Dividend yield	0%	0%

The Black-Scholes option pricing model was developed for use in estimating the fair value of freely tradable, fully transferable options without vesting restrictions. The Company's stock options have characteristics which significantly differ from those of freely tradable, fully transferable options. The Black-Scholes option pricing model also requires highly subjective assumptions, including expected stock price volatility and expected stock option term which greatly affect the calculated fair value of an option. The Company's actual stock price volatility and option term may be materially different from the assumptions used herein.

The resultant grant date weighted-average fair values calculated using the Black-Scholes option pricing model and the noted assumptions for stock options was $11.54 and $12.44, and for stock purchase rights $6.80 and $5.49, for fiscal 1997 and 1996, respectively.

For purposes of pro forma disclosures, the estimated fair value of the options is amortized to expense over the options' vesting period. The Company's pro forma information is as follows:

	YEAR ENDED	
	MARCH 29, 1997	MARCH 30, 1996
Pro forma net income	$40,681	$ 38,836
Pro forma earnings per share	$1.78	$ 1.86

Because the SFAS 123 pro forma disclosure applies only to options granted subsequent to April 1, 1995, its pro forma effect will not be fully reflected until subsequent years. The effects on pro forma disclosures of applying SFAS 123 are not likely to be representative of the effects on pro forma disclosures in future years.

SHAREHOLDER RIGHTS PLAN A shareholder rights plan approved on September 11, 1991 provides for the issuance of one right for each share of outstanding common stock. With certain exceptions, the rights will become exercisable only in the event that an acquiring party accumulates beneficial ownership of 20% or more of the Company's outstanding common stock or announces a tender or exchange offer, the consummation of which would result in ownership by that party of 20% or more of the Company's outstanding common stock. The rights expire on September 11, 2001 if not previously redeemed or exercised. Each right entitles the holder to purchase, for $60.00, a fraction of a share of the Company's Series A Participating Preferred Stock with economic terms similar to that of one share of the Company's common stock. The Company will generally be entitled to redeem the rights at $0.01 per right at any time on or prior to the tenth day after an acquiring person has acquired beneficial ownership of 20% or more of the Company's common stock. If, prior to the redemption or expiration of the rights, an acquiring person or group acquires beneficial ownership of 20% or more of the Company's outstanding common stock, each right not beneficially owned by the acquiring person or group will entitle its holder to purchase, at the rights' then current exercise price, that number of shares of common stock having a value equal to two times the exercise price.

NOTE 9. TRANSACTIONS WITH PRINCIPAL SUPPLIERS

The majority of the Company's silicon wafers are currently manufactured by Seiko Epson in Japan and are sold to the Company through Seiko Epson's affiliated U.S. distributor, SMOS. The Chairman of the Board of SMOS is a member of the Company's Board of Directors.

The Company has signed two advance payment production agreements with Seiko Epson and SMOS, in July 1994 and March 1997, respectively, under which it has advanced or will advance cash to be used in conjunction with the construction of additional wafer capacity, with the advances being repaid in the form of semiconductor wafers over a multi-year period. These transactions are more fully described in note 4 of notes to consolidated financial statements.

The Company continues to purchase a portion of its wafer supply from Seiko Epson for cash using commercial terms. Cash wafer purchases totaled $22.8 million, $34.7 million and $27.8 million for fiscal 1997, 1996 and 1995, respectively. Accounts payable and accrued expenses at March 29, 1997 and March 30, 1996 include $1.9 and $4.0 million, respectively, due this vendor. Open purchase commitments to this vendor approximated $8.8 million at March 29, 1997.

In connection with the series of agreements recently entered into with UMC as described in note 4 of notes to consolidated financial statements, the Company currently receives production wafers. A significant interruption in supply from Seiko Epson through SMOS, or from UMC, would have a material adverse effect on the Company's business.

NOTE 10. EMPLOYEE BENEFIT PLANS

PROFIT SHARING PLAN The Company initiated a profit sharing plan effective April 1, 1990. Under the provisions of this plan, as approved by the Board of Directors, a percentage of the operating income of the Company, as defined and calculated at the end of the second and fourth quarter of each fiscal year for each respective six-month period, is paid equally to qualified employees. In fiscal 1997, 1996 and 1995, approximately $2.4 million, $2.3 million and $1.4 million, respectively, were charged against operations in connection with the plan.

QUALIFIED INVESTMENT PLAN In 1990, the Company adopted a 401(k) plan, which provides participants with an opportunity to accumulate funds for retirement. Under the terms of the plan, eligible participants may contribute up to 15% of their eligible earnings to the plan Trust. The plan allows for discretionary matching contributions by the Company; no such contributions occurred through fiscal 1996. Beginning in fiscal 1997, the Company matched eligible employee contributions of up to 5% of base pay. Company contributions are discretionary and vest over four years.

NOTE 11. COMMITMENTS AND CONTINGENCIES

The Company is exposed to certain asserted and unasserted potential claims. Patent and other proprietary rights infringement claims are common in the semiconductor industry and the Company has received a letter from a semiconductor manufacturer stating that it believes certain patents held by it cover products previously sold by the Company. While this manufacturer has offered to license certain of such patents to the Company, there can be no assurance that, on this or any other claim which may be made against the Company, the Company could obtain a license on terms or under conditions that would not have a material adverse effect to the Company.

NOTE 12. RELATED PARTY

Larry W. Sonsini is a member of the Company's Board of Directors and is presently the Chairman of the Executive Committee of Wilson, Sonsini, Goodrich & Rosati, a law firm that provides corporate legal services to the Company. Legal services billed to the Company aggregated approximately $61,000, $177,000 and $46,000, respectively, for fiscal 1997, 1996 and 1995. Amounts payable to the law firm were not significant at March 29, 1997 or March 30, 1996.

REPORT OF INDEPENDENT ACCOUNTANTS

To the Board of Directors and Stockholders of
Lattice Semiconductor Corporation

In our opinion, the accompanying consolidated balance sheet and the related consolidated statements of operations, of changes in stockholders' equity and of cash flows present fairly, in all material respects, the financial position of Lattice Semiconductor Corporation and its subsidiaries at March 29, 1997 and March 30, 1996, and the results of their operations and their cash flows for each of the three years in the period ended March 29, 1997, in conformity with generally accepted accounting principles. These financial statements are the responsibility of the company's management; our responsibility is to express an opinion on these financial statements based on our audits. We conducted our audits of these statements in accordance with generally accepted auditing standards which require that we plan and perform the audit to obtain reasonable assurance about whether the financial statements are free of material misstatement. An audit includes examining, on a test basis, evidence supporting the amounts and disclosures in the financial statements, assessing the accounting principles used and significant estimates made by management, and evaluating the overall financial statement presentation. We believe that our audits provide a reasonable basis for the opinion expressed above.

/s/ PRICE WATERHOUSE LLP

Portland, Oregon
April 16, 1997

CORPORATE DIRECTORY

BOARD OF DIRECTORS
Cyrus Y. Tsui
Chairman of the Board, President and Chief Executive Officer

Mark O. Hatfield
Former U.S. Senator

Daniel S. Hauer(1)
Chairman of the Board,
S-MOS Systems Inc.

Harry A. Merlo (1), (2)
President,
Merlo Corporation

Douglas C. Strain(2)
Vice Chairman and Founder,
Electro Scientific Industries, Inc.

Larry W. Sonsini
Partner and Chairman of the Executive Committee,
Wilson, Sonsini, Goodrich & Rosati

OFFICERS
Cyrus Y. Tsui
Chairman of the Board, President and Chief Executive Officer

Steven A. Laub
Senior Vice President and Chief Operating Officer

Stephen A. Skaggs
Senior Vice President, Chief Financial Officer and Secretary

Jonathan K. Yu
Corporate Vice President, Business Development

Martin R. Baker
Vice President and General Counsel

Randy D. Baker
Vice President, Manufacturing

Albert L. Chan
Vice President, California Product Development

Stephen M. Donovan
Vice President, International Sales

Paul T. Kollar
Vice President, Sales

Rodney F. Sloss
Vice President, Finance

Kenneth K. Yu
Vice President and Managing Director, Lattice Asia

Technology Advisor to the Office of the President

CORPORATE HEADQUARTERS
Lattice Semiconductor Corporation
5555 N.E. Moore Court
Hillsboro, Oregon 97124-6421
Telephone: 503/681-0118
Facsimile: 503/681-0347

LEGAL COUNSEL
Wilson, Sonsini, Goodrich & Rosati
Palo Alto, California

INDEPENDENT ACCOUNTANTS
Price Waterhouse LLP
Portland, Oregon

REGISTRAR AND TRANSFER AGENT
ChaseMellon Shareholder Services
520 Pike St., Suite 1220
Seattle, Washington 98101
800/522-6645

ANNUAL MEETING
The annual meeting of stockholders for Lattice Semiconductor Corporation will be held at the Portland Hilton Hotel, 921 S.W. Sixth Avenue, Portland, Oregon 97204 on Monday, August 11, 1997, at 1:00 pm.

Form 10-K
Financial information, including the Company's Annual Report on Form 10-K, as filed with the Securities and Exchange Commission, and quarterly operating

results is available by accessing http://www.lscc.com or by written or telephone request to the Lattice shareholder relations department.

COMMON STOCK

Lattice Semiconductor Corporation's common stock is traded on the Nasdaq National Market System under the symbol "LSCC."

STOCK PRICE HISTORY

The following table sets forth the low and high sale prices of the Company's common stock for the last two fiscal years.

	LOW	HIGH
Fiscal 1996:		
First Quarter	23	37 1/8
Second Quarter	28 7/8	43
Third Quarter	27 5/8	42 1/8
Fourth Quarter	26 3/8	37 3/8
Fiscal 1997:		
First Quarter	21 5/8	36 1/4
Second Quarter	19 3/4	31 1/2
Third Quarter	27 1/2	47
Fourth Quarter	39 3/4	54 7/8

(1) MEMBER OF THE AUDIT COMMITTEE
(2) MEMBER OF THE COMPENSATION COMMITTEE

EXHIBIT 21.1

LATTICE SEMICONDUCTOR CORPORATION

SUBSIDIARIES OF THE REGISTRANT

	Name	Jurisdiction of Incorporation
1.	Lattice GmbH	Germany
2.	Lattice Semiconducteurs SARL	France
3.	Lattice Semiconductor AB	Sweden
4.	Lattice Semiconductor Asia Limited	Hong Kong
5.	Lattice Semiconductor International Limited	Jamaica
6.	Lattice Semiconductor KK	Japan
7.	Lattice Semiconductor (Shanghai) Co. Ltd.	China
8.	Lattice UK Limited	United Kingdom

CONSENT OF INDEPENDENT ACCOUNTANTS

We hereby consent to the incorporation by reference in the Registration Statement on Form S-8 (No. 33-33933, No. 33-35259, No. 33-38521, No. 33-76358, No. 33-51232 and No. 33-69496) of Lattice Semiconductor Corporation of our report dated April 16, 1997 appearing in the Annual Report to Stockholders which is incorporated in this Annual Report on Form 10-K. We also consent to the incorporation by reference of our report on the Financial Statement Schedule.

/s/ Price Waterhouse LLP

PRICE WATERHOUSE LLP

Portland, Oregon
June 24, 1997

5
1,000

YEAR	
	MAR-29-1997
	MAR-31-1996
	MAR-29-1997
	53,949
	174,698
	25,940
	874
	27,809
	310,640
	66,816
	39,413
	403,462
	42,971
	0
	0
	0
	229
	360,262
403,462	
	204,089
	204,089
	83,736
	145,123
	0
	18
	(8,712)
	67,678
	22,673
	45,005
	0
	0
	0
	45,005
	1.96
	1.96